June 1996

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About this Data Book

June 1996

This data book provides comprehensive information about Altera's FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, Classic, and Configuration EPROM device families, MAX+PLUS II development tools, and programming hardware.

How to Contact Altera

For additional information about Altera products, consult the sources shown in Table 1.

Table 1. How to Contact Altera

Information Type	Access	US & Canada	All Other Locations
Literature	Altera Express	(800) 5-ALTERA	(408) 894-7850
	Altera Literature Services	(408) 894-7144 *(1)*	(408) 894-7144 *(1)*
Non-technical customer service	Telephone hotline	(800) SOS-EPLD	(408) 894-7000
	Fax	(408) 954-8186	(408) 954-8186
Technical Support	Telephone hotline (8:00 a.m. to 5 p.m. Pacific Standard Time)	(800) 800-EPLD	(408) 894-7000 *(1)*
	Fax	(408) 954-0348	(408) 954-0348 *(1)*
	Bulletin board service	(408) 954-0104	(408) 954-0104
	Electronic mail	sos@altera.com	sos@altera.com
	FTP site	ftp.altera.com	ftp.altera.com
	CompuServe	go altera	go altera
General product information	Telephone	(408) 894-7104	(408) 894-7104 *(1)*
	World-wide web	http://www.altera.com	http://www.altera.com

Note:

(1) You can also contact your local Altera sales office or sales representative. See *Sales Offices, Distributors & Representatives* in this data book.

Typographic Conventions

The *1996 Data Book* uses the typographic conventions shown in Table 2.

Table 2. 1996 Data Book Conventions

Visual Cue	Meaning
Bold Initial Capitals	Dialog box titles are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold. Examples: $\mathbf{f_{MAX}}$, **\maxplus2** directory, **d:** drive, **chiptrip.gdf** file.
Bold italics	Book titles are shown in bold italics, initial capital letters. Example: ***1996 Data Book***.
Italic Initial Capitals	Application note and data sheet names, checkbox options, and options in dialog boxes are shown in italics with initial capital letters. Examples: *AN 52 (Implementing RAM Functions in FLEX 10K Devices)*, the *Check Outputs* option, the *Directories* box in the **Open** dialog box.
italics	Internal timing parameters and variables are shown in italics. Examples: t_{PIA}, $n + 1$. Variables are enclosed in angle brackets (< >) and shown in italics. Example: *<filename>*, *<project name>*.**pof** file.
Initial Capitals	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	Subheadings within a data book section and titles of MAX+PLUS II Help topics are shown in quotation marks. Example: "Configuring a FLEX 10K or FLEX 8000 Device with the BitBlaster."
`Courier font`	Reserved signal and port names are shown in uppercase Courier. Examples: `DATA1`, `TDI`, `INPUT`. User-defined signal and port names are shown in lowercase Courier. Examples: `my_data`, `ram_input`. Anything that must be typed exactly as it appears is shown in Courier. For example: `c:\max2work\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c.,...	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

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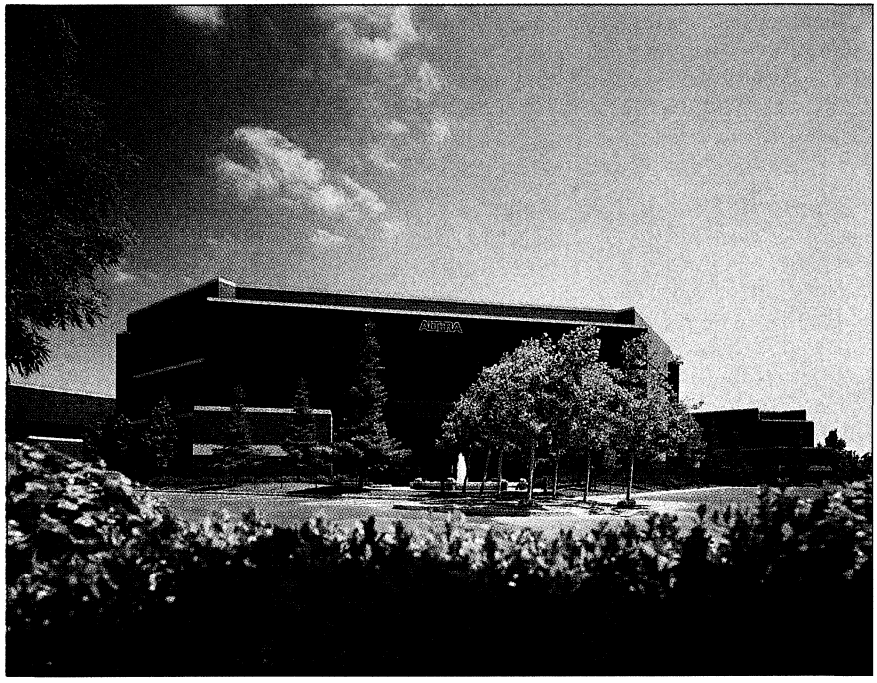
ALTRA

Introduction

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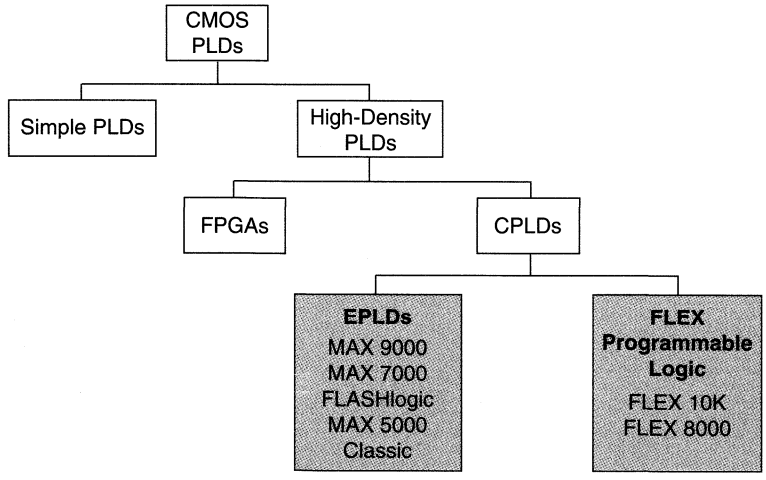
Programmable logic devices (PLDs) are digital, user-configurable integrated circuits (ICs) used to implement custom logic functions. PLDs can implement any Boolean expression or registered function with built-in logic structures. In contrast, off-the-shelf logic ICs, such as TTL devices, provide a specific logic function and cannot be modified to meet individual circuit design requirements. PLDs were once viewed as an alternative to discrete logic and custom or semi-custom devices such as ASICs; in recent years, however, PLDs have become the preferred choice. As PLD costs have decreased through high-volume manufacturing and the use of aggressive process technologies, PLD manufacturers have been able to offer devices with higher integration, higher performance, and lower cost per function than discrete devices.

The PLD Market

Programmable logic encompasses all digital logic circuits configured by the end user, including simple, low-density, 20-pin PAL/GAL devices, field-programmable gate arrays (FPGAs), and complex PLDs (CPLDs). PLDs are offered in different architectures, and a variety of memory elements are available for configuring the devices. Figure 1 shows the relative position of Altera general-purpose devices in the CMOS PLD market.

Figure 1. Altera General-Purpose Logic Devices



CPLDs and FPGAs have different interconnect structures. The segmented interconnect structure of FPGAs uses multiple metal lines of varying lengths connected by pass transistors or anti-fuses to connect logic cells. In contrast, the continuous interconnect structure of CPLDs uses continuous metal lines to provide logic cell-to-logic cell connectivity. The continuous interconnect structure eliminates the unpredictable timing associated with a segmented interconnect structure, and provides fast, fixed delay paths between logic cells. The continuous interconnect structure makes it easier to implement a design, and thus shortens the development cycle.

Advantages of Altera PLDs

Designers generally develop a logic circuit with one of three distinctly different implementation options: discrete logic (TTL, CMOS, etc.), custom or semi-custom devices (ASICs), or PLDs. The best option is one that can meet the largest number of design requirements. Table 1 lists a number of important requirements and rates the three options according to their effectiveness in meeting these requirements.

Table 1. Device Options Rating *Note (1)*

Requirement	PLD	Discrete Logic	ASIC
Speed	●	○	●
Density	●	○	●
Cost	●	○	● *(2)*
Development time	●	◗	○
Prototyping & simulation time	●	○	○
Manufacturing time	●	◗	○
Ease of use	●	◗	○
Future modification	●	◗	○
Inventory risk	●	●	○
Development tool support	●	○	●

Notes:
(1) ● Very effective
◗ Adequate
○ Poor
(2) Cost-effective only in high-volume production.

Altera PLDs offer the general benefits of PLD technology, and can offer the following advantages based on innovative architectures, advanced process technologies, state-of-the-art development tools, and a wide selection of megafunctions:

- Higher performance
- High-density logic integration
- Greater cost-effectiveness
- Shorter development cycles with MAX+PLUS II software
- Shorter development cycles with megafunctions

Higher Performance

Performance is a function of technology and architecture. Because Altera devices are manufactured on state-of-the-art CMOS technology, they offer the fastest possible performance. In addition, continuous interconnect structures provide fast, consistent signal delays throughout the device, and innovations such as specialized on-chip circuitry further enhance system performance.

High-Density Logic Integration

Designers often seek the highest possible logic integration for their new designs, usually to reduce board space and cost. Also, existing designs frequently undergo secondary development cycles in the attempt to reduce cost by integrating more logic into fewer devices. In both cases, PLDs with high logic integration capability offer an excellent solution. Altera devices—which range in density from 300 to 100,000 usable gates—can easily integrate existing logic, whether it be a small or large number of discrete logic devices, PLDs, FPGAs, or custom devices. The high integration capability of PLDs provides higher system performance, greater reliability, and lower system cost.

Greater Cost-Effectiveness

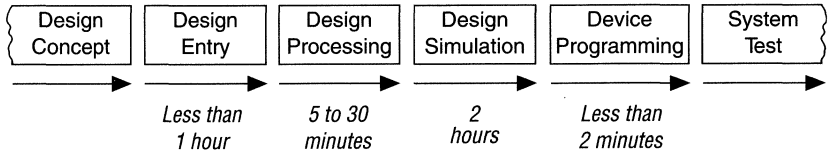
Altera continually strives to refine product development and manufacturing processes. The expertise accumulated in more than a decade of industry leadership has made both process technologies and manufacturing flow highly efficient, enabling Altera to offer the most cost-effective, highest-performance programmable logic available.

Shorter Development Cycles with MAX+PLUS II Software

Time is the most precious resource for many design engineers. Large sums of money are lost on projects that are not completed on schedule, thereby missing a window of opportunity in the market. Consequently, designers seek to achieve the shortest development cycle times as possible. Altera's fast, intuitive, and easy-to-use MAX+PLUS II software can dramatically shorten the development cycle. With MAX+PLUS II, design entry, processing, verification, and device programming together require only a few hours, potentially allowing several complete design iterations in one day. Altera also works closely with EDA manufacturers to link MAX+PLUS II with other industry-standard design-entry, synthesis, and verification tools such as those provided by Cadence, Mentor Graphics, Synopsys, and Viewlogic. Figure 2 illustrates a typical PLD development cycle in the MAX+PLUS II development environment.

Figure 2. Altera PLD Development Cycle in MAX+PLUS II

The times shown are representative of a relatively sophisticated 10,000-gate logic design.



Shorter Development Cycles with Megafunctions

With PLD densities reaching as high as 100,000-gates, it is now possible to implement entire digital sub-systems within a single programmable device. To facilitate this high level of integration and to further reduce design cycles, Altera provides megafunctions in the form of MegaCore functions and megafunctions created through the Altera Megafunction Partners Program (AMPP). Megafunctions are off-the-shelf building blocks that implement useful functions such as processors, digital signal processing (DSP) functions, bus controllers, and interfaces. Megafunctions provide a higher degree of flexibility and performance not attainable in fixed-function devices (e.g., high-speed FIR filters), and are targeted to a variety of applications, including:

- Digital signal processing (DSP)
- Image processing
- High-speed networking, including asynchronous transfer mode (ATM)
- Bus protocols, including peripheral component interconnect (PCI)
- Microprocessors and microperipherals

The Altera MegaCore functions range from standard building blocks, such as universal asynchronous receivers/transmitters (UARTs) and controllers, to innovative design examples that exploit the features of PLDs. Altera devices and development tools support both Altera-supplied MegaCore functions and functions created through AMPP.

Altera Device Families

Altera offers seven families of general-purpose PLDs: FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices. See Table 2. The Flexible Logic Element MatriX (FLEX) architecture uses look-up tables (LUTs) to implement logic functions, whereas the Multiple Array MatriX (MAX), FLASHlogic, and Classic architectures use a programmable-AND/fixed-OR product-term architecture. Each device family offers unique features as well as distinct speed and utilization advantages for implementing particular applications.

Table 2. Altera Device Architectures

Device Family	Logic Cell Structure	Interconnect Structure	Reconfigurable Element
FLEX 10K	Look-up table	Continuous	SRAM
FLEX 8000	Look-up table	Continuous	SRAM
MAX 9000	Product term	Continuous	EEPROM
MAX 7000	Product term	Continuous	EEPROM
FLASHlogic	Product term	Continuous	SRAM & FLASH
MAX 5000	Product term	Continuous	EPROM
Classic	Product term	Continuous	EPROM

Figure 3 compares the pin count and density of each device family.

Figure 3. Pin Count & Density in Altera Device Families

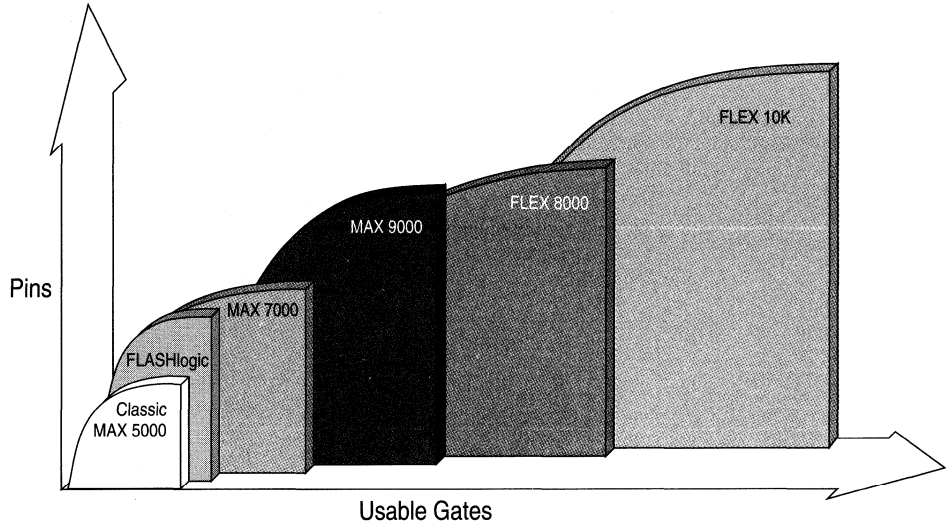
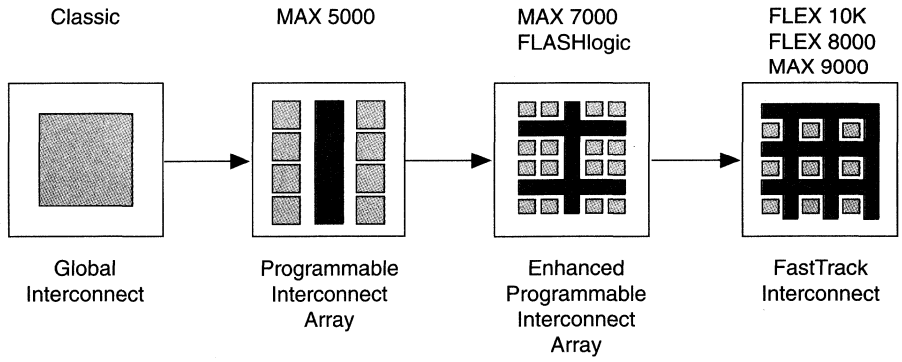


Figure 4 summarizes the architectures of Altera devices and illustrates how the interconnect structure has evolved to maintain high performance even at the highest densities.

Figure 4. Altera Architecture Evolution



All Altera device families are fabricated on CMOS processes, which provides lower power dissipation and greater reliability than bipolar processes. As part of Altera's commitment to continual improvement, products are transferred to advanced process technologies as soon as they become viable and can support reliable manufacturing. This transfer generally reduces manufacturing costs and enhances performance, producing faster, more cost-effective devices. The following descriptions summarize the key features and benefits of Altera's general-purpose PLD families.

FLEX 10K Device Family

The FLEX 10K device family features the first PLDs to contain embedded arrays and includes the industry's largest PLD (up to 100,000 gates). FLEX 10K devices can address the increasing levels of integration needed to accommodate system-on-a-chip designs because of their high density and ability to implement complex megafunctions and memories in designs. Each FLEX 10K device contains an embedded array, which gives designers the efficiency of embedded gate array megafunctions and the flexibility of programmable logic. The embedded array is composed of a series of embedded array blocks (EABs), which can be used to implement various memory and complex logic functions. Other architectural features, such as multiple low-skew clocks, ClockLock and ClockBoost phase-locked loop (PLL) circuitry, and internal tri-state buses, provide the performance and efficiency required for system-level integration. These features make FLEX 10K devices ideal for applications that have been traditionally reserved for gate arrays.

FLEX 8000 Device Family

The FLEX 8000 device family is ideal for applications that require a large number of registers and I/O pins. Devices in this family range in density from 2,500 to 16,000 usable gates, with 282 to 1,500 registers, and 78 to 208 user I/O pins. These features, along with its high-performance, predictable interconnect structure, make FLEX 8000 devices as easy to use as product-term-based devices. In addition, the SRAM-based FLEX 8000 devices provide low standby power and can be reconfigured in-circuit, making them ideal for such applications as PC add-on cards, battery-powered instruments, and multi-purpose telecommunication cards.

MAX 9000 Device Family

The MAX 9000 device family combines the efficient macrocell architecture of MAX 7000 devices with the high-performance, predictable FastTrack Interconnect of FLEX devices, resulting in a device family that is ideal for integrating multiple system-level functions. The EEPROM-based MAX 9000 device family ranges from 6,000 to 12,000 usable gates, 320 to 560 macrocells, and up to 216 user I/O pins. This level of density, combined with support for JTAG boundary-scan testing (BST) and in-system programmability (ISP), make the MAX 9000 device family an ideal choice for gate array designs that can use the benefits of PLDs and the flexibility of ISP.

MAX 7000 Device Family

The MAX 7000 device family is the fastest high-density programmable logic family in the industry. The MAX 7000 device family, which includes the MAX 7000E and MAX 7000S devices, ranges in density from 600 to 5,000 usable gates, 32 to 256 macrocells, and 36 to 164 user I/O pins. These EEPROM-based devices offer combinatorial propagation delays as fast as 5.0 ns and 16-bit counter frequencies of 178 MHz. Moreover, they provide very fast input register setup times, multiple system clocks, and a programmable speed/power control. The slew rate for I/O pins can be controlled, providing an extra level of switching noise control. MAX 7000E devices are the higher-density, feature-enhanced members of the MAX 7000 family. MAX 7000S devices provide the enhanced features of MAX 7000E devices as well as support for JTAG BST, ISP, and on-chip ClockBoost PLL circuitry.

FLASHlogic Device Family

The FLASHlogic device family features architectural innovations that are ideal for implementing logic designs that require internal RAM, in-circuit reconfigurability (ICR), ISP, or JTAG BST support. The FLASHlogic device family is SRAM-based, but also has built-in, nonvolatile FLASH cells, eliminating the need for an external data source. The family ranges in density from 1,600 to 3,200 usable gates, 80 to 160 macrocells, and 62 to 120 user I/O pins. These features, combined with combinatorial delays as fast as 10 ns, make the FLASHlogic device family ideal for microprocessor-based systems and bus interface applications.

MAX 5000 Device Family

The MAX 5000 device family provides a comprehensive, cost-effective solution for designs that require a high level of combinatorial logic. The MAX 5000 device family provides logic densities ranging from 600 to 3,750 usable gates, and pin counts ranging from 28 to 100 pins. The EPROM-based MAX 5000 devices are nonvolatile and erasable. Altera's continuing commitment to migrating existing families to newer, more aggressive technologies has yielded MAX 5000 devices that offer excellent cost-per-macrocell values, and which compare favorably to ASICs and gate arrays for high-volume production.

Classic Device Family

The Classic device family is Altera's original family of devices. The EPROM-based Classic devices feature densities of up to 900 usable gates and pin counts of up to 68 pins. Composed of single arrays of globally interconnected logic, the industry-standard Classic device family offers a low-cost solution for low-density applications. Classic devices offer a unique "zero-power" mode, allowing the devices to draw only microamps of current at standby, which makes them ideal for low-power applications.

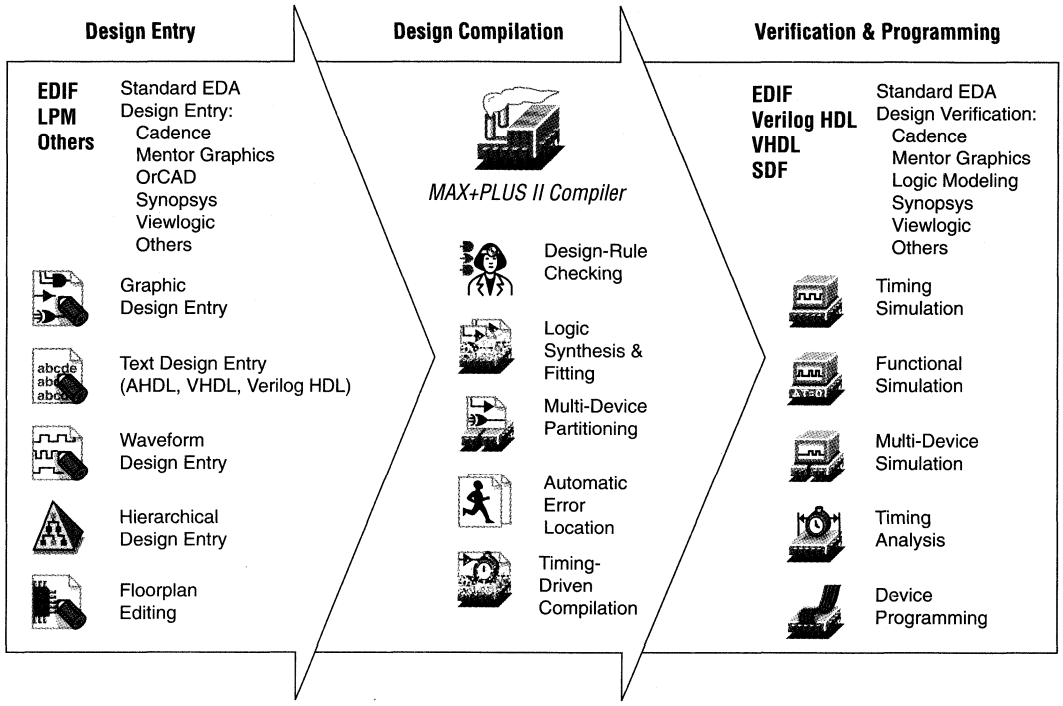
Solutions for High-Volume Production

For applications targeted for high-volume production, Altera offers Mask-Programmed Logic Devices (MPLDs) as low-cost alternatives to high-density PLDs. MPLDs, which are masked versions of PLDs, offer a unique turn-key approach that eliminates the engineering-intensive tasks required for custom and semi-custom devices. The quick turnaround for MPLD conversion ensures fast time-to-market.

MAX+PLUS II Development Tools

Altera achieves maximum device performance and density with advanced process technologies, innovative logic architectures, and state-of-the-art design tools. The MAX+PLUS II programmable logic development system provides an architecture-independent design environment and ensures easy design entry, fast compilation, and uncomplicated device programming. See Figure 5. MAX+PLUS II supports designs for Altera's FLEX, MAX, and Classic device families. In addition, Altera's PLDshell Plus software supports designs for the FLASHlogic device family.

Figure 5. MAX+PLUS II Design Environment



With MAX+PLUS II, designers no longer need to master the complexities of device architectures. MAX+PLUS II translates designs—created with familiar design entry tools such as schematic capture tools or high-level behavioral languages—into the format required by the target architecture.

The extensive architectural knowledge built into Altera development tools minimizes the need for designers to manually optimize their designs, which allows designers to complete their designs more quickly. With MAX+PLUS II, users can take a logic circuit from design entry to device programming in a matter of hours. Design compilation is typically completed in minutes, allowing several complete design iterations in a single day.

Design Entry, Compilation, Verification & Device Programming

MAX+PLUS II offers a full spectrum of logic design capabilities. Designers are free to combine text, graphic, and waveform design entry methods while creating hierarchical single- or multi-device designs. The MAX+PLUS II Compiler performs minimization and logic synthesis, fits the design into one or more devices, and generates programming data. Design verification with functional and timing simulation and delay prediction for speed-critical paths are available, as well as multi-device simulation across multiple device families. Altera and a number of programming hardware manufacturers offer hardware for programming the devices.

Access to Various Platforms & Other EDA Tools

Altera is committed to supporting the logic development environments that are most familiar to circuit designers. MAX+PLUS II provides interfaces to a wide variety of other EDA tools—from companies such as Cadence, Mentor Graphics, OrCAD, Synopsys, VeriBest, and Viewlogic. MAX+PLUS II and these EDA tools share information via EDIF, library of parameterized modules (LPM), Verilog HDL, and VHDL. The MAX+PLUS II Compiler runs on PC and various workstation platforms, making MAX+PLUS II the industry's only platform-independent, architecture-independent programmable logic design environment. The ACCESS alliance, which Altera has formed with industry-leading EDA tool vendors, ensures smooth interfaces between Altera products and ACCESS partner products, and timely support of Altera devices with these tools.

Conclusion

The advanced architectures and process technologies used in Altera devices provide the greatest performance, highest density, and greatest flexibility available in the programmable logic market. Regardless of an application's requirements, Altera devices provide an efficient solution with high levels of integration, high I/O capabilities, and the fastest speeds available.

The sophisticated, highly integrated MAX+PLUS II development system completes Altera's total solution. MAX+PLUS II gives designers the ability to take full advantage of all the features offered in Altera's FLEX, MAX, and Classic devices. MAX+PLUS II can target a project to the FLEX, MAX, and Classic device families, thus offering designers architecture-independent design capabilities, regardless of their preferred design flow. Together, Altera devices and development tools are the logical choice for high-density designs that require fast development cycles and cost-effective devices.

Notes:

Component Selection Guide

June 1996, ver. 3 Data Sheet

Introduction

This selection guide lists the available system-level features and devices from Altera:

- System-level features
- FLEX 10K devices
- FLEX 8000 devices
- Configuration EPROM devices
- MAX 9000 devices
- MAX 7000 devices
- FLASHlogic devices
- MAX 5000 devices
- Classic devices
- 3.3-V devices
- Devices with 3.3-V or 5.0-V I/O pins
- PCI-compliant devices

For detailed information on these products, refer to the appropriate sections in this data book. For information on Altera's programmable logic development system, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

The information in this selection guide is accurate as of the printing date. For the latest device information, contact your local Altera sales representative.

System-Level Features

Table 1 lists the system-level features available for each Altera device family.

Table 1. System-Level Features for Altera Devices

Device Family	3.3-V Device *(1)*	3.3-V or 5.0-V I/O Pins *(1)*	PLL *(2)*	PCI Compliance *(3)*	ISP *(4)*	ICR *(5)*	JTAG Boundary-Scan Testing	Embedded SRAM	Slew-Rate Control	Open-Drain Outputs
FLEX 10K	✓	✓	✓ *(6)*	✓ *(6)*		✓	✓	✓	✓	✓
FLEX 8000	✓ *(6)*	✓		✓ *(6)*		✓	✓ *(6)*		✓	
MAX 9000		✓		✓ *(6)*	✓		✓		✓	
MAX 7000	✓ *(6)*	✓		✓ *(6)*					✓	
MAX 7000S	✓ *(6)*	✓	✓ *(6)*	✓ *(6)*	✓		✓ *(6)*		✓	✓
FLASHlogic		✓		✓ *(6)*	✓	✓	✓	✓	✓	✓
MAX 5000										
Classic										

Notes:

(1) See "3.3-V Devices" on page 26 and "Devices with 3.3-V or 5.0-V I/O Pins" on page 26 in this data sheet for a list of specific devices that provide this feature.
(2) PLL represents the phase-locked loop feature.
(3) See "PCI-Compliant Devices" on page 27 in this data sheet for a list of specific devices that provide this feature.
(4) ISP represents in-system programmability.
(5) ICR represents in-circuit reconfigurability.
(6) Certain devices in this family provide this system-level feature. Consult the appropriate device family data sheet in this data book for more information.

FLEX 10K Devices

Altera's FLEX 10K devices are the first programmable logic devices (PLDs) to contain embedded arrays, offering up to 100,000 gates in a single programmable device. The revolutionary Flexible Logic Element MatriX (FLEX) device architecture in FLEX 10K devices offers system-level integration and megafunction support, making FLEX 10K devices ideal for gate array prototyping. See Table 2.

Table 2. FLEX 10K Devices *Note (1)*

Device	Typical Gates	Packages (2)	Temp. (3)	Speed Grade	Process	Logic Cells/ Registers	Ded. Inputs	I/O Pins	Number of Pins
EPF10K10	10,000	L, T, Q	C	-3	SRAM	576 / 720	6	59, 107, 134	84, 144, 208
	10,000	L, T, Q	C, I	-4	SRAM	576 / 720	6	59, 107, 134	84, 144, 208
EPF10K20	20,000	R	C	-3	SRAM	1,152 / 1,344	6	147, 189	208, 240
	20,000	R	C, I	-4	SRAM	1,152 / 1,344	6	147, 189	208, 240
EPF10K30	30,000	R, B	C	-3	SRAM	1,728 / 1,968	6	147, 189, 246	208, 240, 356
	30,000	R, B	C, I	-4	SRAM	1,728 / 1,968	6	147, 189, 246	208, 240, 356
EPF10K40	40,000	R	C	-3	SRAM	2,304 / 2,576	6	147, 189	208, 240
	40,000	R	C, I	-4	SRAM	2,304 / 2,576	6	147, 189	208, 240
EPF10K50	50,000	R, G, B	C	-3	SRAM	2,880 / 3,184	6	189, 274, 310	240, 356, 403
	50,000	R, G, B	C, I	-4	SRAM	2,880 / 3,184	6	189, 274, 310	240, 356, 403
	50,000	R, G, B	C, I	-5	SRAM	2,880 / 3,184	6	189, 274, 310	240, 356, 403
EPF10K70	70,000	R, G	C	-3	SRAM	3,744 / 4,096	6	189, 358	240, 503
	70,000	R, G	C, I	-4	SRAM	3,744 / 4,096	6	189, 358	240, 503
EPF10K100	100,000	G	C	-3	SRAM	4,992 / 5,392	6	406	503
	100,000	G	C, I	-4	SRAM	4,992 / 5,392	6	406	503

Notes:

(1) Preliminary information is shown for some devices. Consult the *FLEX 10K Embedded Programmable Logic Family Data Sheet* in this data book for more information, or contact Altera Customer Marketing for the most current device information.

(2) Package configurations (contact Altera Customer Marketing for information on device package availability):
- L: Plastic J-lead chip carrier (PLCC)
- T: Plastic thin quad flat pack (TQFP)
- Q: Plastic quad flat pack (PQFP)
- R: Power quad flat pack (RQFP)
- G: Ceramic pin-grid array (PGA)
- B: Ball-grid array (BGA)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)

FLEX 8000 Devices

Table 3 provides information on the FLEX 8000 device family of register-intensive, high-density PLDs. Low-cost FLEX 8000 devices are the ideal replacement for gate arrays with fewer than 20,000 gates. FLEX 8000 devices combine the fine-grained architecture and high register count of FPGAs with the high speed, predictable interconnect delays, and ease-of-use of EPLDs. FLEX 8000 devices are SRAM-based, fabricated on an advanced CMOS technology.

Table 3. FLEX 8000 Devices *Note (1)*

Device	Package *(2)*	Temp. *(3)*	Speed Grade	Process	Logic Cells/ Registers	Ded. Inputs	I/O Pins	Number of Pins
EPF8282A	L, T	C	A-2	SRAM	208 / 282	4	68, 78	84, 100
	L, T	C, I	A-3	SRAM	208 / 282	4	68, 78	84, 100
	L, T	C	A-4	SRAM	208 / 282	4	68, 78	84, 100
EPF8282AV	L, T	C	A-3	SRAM	208 / 282	4	68, 78	84, 100
Note (4)	L, T	C, I	A-4	SRAM	208 / 282	4	68, 78	84, 100
EPF8452A	L, T, Q, G	C	A-2	SRAM	336 / 452	4	68, 120	84, 100, 160
	L, T, Q, G	C, I	A-3	SRAM	336 / 452	4	68, 120	84, 100, 160
	L, T, Q, G	C	A-4	SRAM	336 / 452	4	68, 120	84, 100, 160
EPF8636A	L, Q, R, G	C	A-2	SRAM	504 / 636	4	68, 110, 136	84, 160, 192, 208
	L, Q, R, G	C, I	A-3	SRAM	504 / 636	4	68, 110, 136	84, 160, 192, 208
	L, Q, R, G	C	A-4	SRAM	504 / 636	4	68, 110, 136	84, 160, 192, 208
EPF8820A	T, Q, G, B	C	A-2	SRAM	672 / 820	4	120, 152	144, 160, 192, 208, 225
	T, Q, G, B	C, I	A-3	SRAM	672 / 820	4	120, 152	144, 160, 192, 208, 225
	T, Q, G, B	C	A-4	SRAM	672 / 820	4	120, 152	144, 160, 192, 208, 225
EPF81188A	Q, R, G	C	A-2	SRAM	1,008 / 1,188	4	148, 184	208, 232, 240
	Q, R, G	C, I	A-3	SRAM	1,008 / 1,188	4	148, 184	208, 232, 240
	Q, R, G	C	A-4	SRAM	1,008 / 1,188	4	148, 184	208, 232, 240
EPF81500A	R, G	C	A-2	SRAM	1,296 / 1,500	4	181, 208	240, 280, 304
	R, G	C, I	A-3	SRAM	1,296 / 1,500	4	181, 208	240, 280, 304
	R, G	C	A-4	SRAM	1,296 / 1,500	4	181, 208	240, 280, 304

Notes:
(1) Preliminary information is shown for some devices. Consult the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book for more information, or contact Altera Customer Marketing for the most current device information.
(2) Package configurations (contact Altera Customer Marketing for information on device package availability):
L: Plastic J-lead chip carrier (PLCC)
T: Plastic thin quad flat pack (TQFP)
Q: Plastic quad flat pack (PQFP)
R: Power quad flat pack (RQFP)
G: Ceramic pin-grid array (PGA)
B: Ball-grid array (BGA)
(3) Operating temperature:
C: Commercial (0° C to 70° C)
I: Industrial (–40° C to 85° C)
(4) The EPF8282AV is a 3.3-V version of the EPF8282A.

Configuration EPROM Devices

Table 4 provides information on Altera serial Configuration EPROMs, which can be used to configure FLEX devices.

Table 4. Configuration EPROMs for FLEX Devices *Note (1)*

Device	Package *(2)*	Temp. *(3)*	Process	Number of Pins	Description
EPC1064	P, L, T	C, I	EPROM	8, 20, 32	64K × 1-bit serial EPROM for configuring FLEX 8000 devices.
EPC1064V *Note (4)*	P, L, T	C, I	EPROM	8, 20, 32	64K × 1-bit serial EPROM for configuring FLEX 8000 devices.
EPC1213	P, L	C, I	EPROM	8, 20	213K × 1-bit serial EPROM for configuring FLEX 8000 devices.
EPC1	P, L, T	C, I	EPROM	8, 20, 32	1Mbyte × 1-bit serial EPROM for configuring FLEX 10K and FLEX 8000 devices.
EPC1V *Note (5)*	P, L, T	C	EPROM	8, 20, 32	1Mbyte × 1-bit serial EPROM for configuring FLEX 10K and FLEX 8000 devices.

Notes:
(1) Preliminary information is shown for some devices. Consult the *Configuration EPROMs for FLEX Devices Data Sheet* in this data book for more information, or contact Altera Customer Marketing for the most current device information.
(2) Package configurations (contact Altera Customer Marketing for information on device package availability):
P: Plastic dual in-line package (PDIP)
L: Plastic J-lead chip carrier (PLCC)
T: Plastic thin quad flat pack (TQFP)
(3) Operating temperature:
C: Commercial (0° C to 70° C)
I: Industrial (–40° C to 85° C)
(4) The EPC1064V is a 3.3-V version of the EPC1064.
(5) The EPC1V is a 3.3-V version of the EPC1.

MAX 9000 Devices

The MAX 9000 family of high-density PLDs is based on Altera's third-generation Multiple Array MatriX (MAX) architecture. Fabricated on an advanced CMOS technology, the EEPROM-based MAX 9000 family provides 6,000 to 12,000 usable gates, 320 to 560 macrocells, in-system programmability (ISP), and JTAG BST circuitry. See Table 5.

Table 5. MAX 9000 Devices *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	Process	Logic Cells/ Registers	Ded. Inputs	I/O Pins	Number of Pins
EPM9320	L, R, G	C	-12	EEPROM	320 / 484	4	60, 132, 168	84, 208, 280
	L, R, G	C	-15	EEPROM	320 / 484	4	60, 132, 168	84, 208, 280
	L, R, G	C, I	-20	EEPROM	320 / 484	4	60, 132, 168	84, 208, 280
EPM9400	L, R	C	-12	EEPROM	400 / 580	4	59, 139, 159	84, 208, 240
	L, R	C	-15	EEPROM	400 / 580	4	59, 139, 159	84, 208, 240
	L, R	C, I	-20	EEPROM	400 / 580	4	59, 139, 159	84, 208, 240
EPM9480	R	C	-15	EEPROM	480 / 616	4	146, 175	208, 240
	R	C, I	-20	EEPROM	480 / 616	4	146, 175	208, 240
EPM9560	R, G	C	-15	EEPROM	560 / 772	4	153, 191, 216	208, 240, 280, 304
	R, G	C, I	-20	EEPROM	560 / 772	4	153, 191, 216	208, 240, 280, 304

Notes:

(1) Preliminary information is shown for some devices. Consult the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book for more information, or contact Altera Customer Marketing for the most current device information.

(2) Package configurations (contact Altera Customer Marketing for information on device package availability):
- L: Plastic J-lead chip carrier (PLCC)
- R: Power quad flat pack (RQFP)
- G: Ceramic pin-grid array (PGA)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)

MAX 7000 Devices

Table 6 provides information on the MAX 7000 family of high-density, high-speed, I/O-intensive PLDs. These EEPROM-based devices range from fast 5-ns PAL/GAL integrators to high-speed, programmable gate array alternatives. MAX 7000 devices are fabricated on CMOS technology.

The higher-density members of the MAX 7000 family—called MAX 7000E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

ISP-capable versions of the MAX 7000 family—called MAX 7000S devices—have the enhanced features of MAX 7000E devices as well as system-level features such as ISP, JTAG BST circuitry in devices with 128 and greater macrocells, and an open-drain output option.

Table 6. MAX 7000 Devices (Part 1 of 2) *Note (1)*

Device	Package *(2)*	Temp. *(3)*	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Process	Logic Cells/ Registers	Ded. Inputs	I/O Pins	Number of Pins
EPM7032,	L, T	C	-5	5	176	EEPROM	32	4	36	44
EPM7032S	L, T	C	-6	6	150	EEPROM	32	4	36	44
	L, T	C	-7	7.5	125	EEPROM	32	4	36	44
	L, T	C, I	-10	10	100	EEPROM	32	4	36	44
	L, T	C, I	-12	12	90.9	EEPROM	32	4	36	44
	L, T	C, I	-15	15	76.9	EEPROM	32	4	36	44
EPM7032V	L, T	C	-12	12	90.9	EEPROM	32	4	36	44
Note (4)	L, T	C	-15	15	76.9	EEPROM	32	4	36	44
	L, T	C, I	-20	20	62.5	EEPROM	32	4	36	44
EPM7064,	L, T, Q	C	-5	5	176	EEPROM	64	4	36, 52, 68	44, 68, 84, 100
EPM7064S	L, T, Q	C	-6	6	150	EEPROM	64	4	36, 52, 68	44, 68, 84, 100
	L, T, Q	C	-7	7.5	125	EEPROM	64	4	36, 52, 68	44, 68, 84, 100
	L, T, Q	C, I	-10	10	100	EEPROM	64	4	36, 52, 68	44, 68, 84, 100
	L, T, Q	C	-12	12	90.9	EEPROM	64	4	36, 52, 68	44, 68, 84, 100
	L, T, Q	C, I	-15	15	76.9	EEPROM	64	4	36, 52, 68	44, 68, 84, 100
EPM7096,	L, T, Q	C	-6	6	150	EEPROM	96	4	52, 64, 76	68, 84, 100
EPM7096S	L, T, Q	C	-7	7.5	125	EEPROM	96	4	52, 64, 76	68, 84, 100
	L, Q	C, I	-10	10	100	EEPROM	96	4	52, 64, 76	68, 84, 100
	L, Q	C	-12	12	90.9	EEPROM	96	4	52, 64, 76	68, 84, 100
	L, Q	C, I	-15	15	76.9	EEPROM	96	4	52, 64, 76	68, 84, 100

Table 6. MAX 7000 Devices (Part 2 of 2) *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Process	Logic Cells/ Registers	Ded. Inputs	I/O Pins	Number of Pins
EPM7128E, EPM7128S *Notes (5), (6)*	L, T, Q	C	-6	6	150	EEPROM	128	4	68, 84, 100	84, 100, 160
	L, T, Q	C	-7	7.5	125	EEPROM	128	4	68, 84, 100	84, 100, 160
	L, T, Q	C, I	-10P	10	100	EEPROM	128	4	68, 84, 100	84, 100, 160
	L, T, Q	C, I	-10	10	100	EEPROM	128	4	68, 84, 100	84, 100, 160
	L, T, Q	C	-12	12	90.9	EEPROM	128	4	68, 84, 100	84, 100, 160
	L, T, Q	C, I	-15	15	76.9	EEPROM	128	4	68, 84, 100	84, 100, 160
	L, T, Q	C, I	-20	20	62.5	EEPROM	128	4	68, 84, 100	84, 100, 160
EPM7128SV	L, T, Q	C	-10	10	100	EEPROM	128	4	64, 84, 100	84, 100, 160
	L, T, Q	C	-15	15	76.9	EEPROM	128	4	64, 84, 100	84, 100, 160
EPM7160E, EPM7160S *Notes (5), (6)*	L, T, Q	C	-7	7.5	125	EEPROM	160	4	64, 84, 104	84, 100, 160
	L, T, Q	C, I	-10P	10	100	EEPROM	160	4	64, 84, 104	84, 100, 160
	L, T, Q	C, I	-10	10	100	EEPROM	160	4	64, 84, 104	84, 100, 160
	L, T, Q	C	-12	12	90.9	EEPROM	160	4	64, 84, 104	84, 100, 160
	L, T, Q	C, I	-15	15	76.9	EEPROM	160	4	64, 84, 104	84, 100, 160
	L, T, Q	C, I	-20	20	62.5	EEPROM	160	4	64, 84, 104	84, 100, 160
EPM7192E, EPM7192S *Notes (5), (6)*	Q, G	C	-7	7.5	125	EEPROM	192	4	124	160
	Q, G	C	-10	10	100	EEPROM	192	4	124	160
	Q, G	C	-12P	12	90.9	EEPROM	192	4	124	160
	Q, G	C	-12	12	90.9	EEPROM	192	4	124	160
	Q, G	C, I	-15	15	76.9	EEPROM	192	4	124	160
	Q, G	C, I	-20	20	62.5	EEPROM	192	4	124	160
EPM7256E, EPM7256S *Notes (5), (6)*	Q, R, G	C	-7	7.5	125	EEPROM	256	4	132, 164	160, 192, 208
	Q, R, G	C	-10	10	100	EEPROM	256	4	132, 164	160, 192, 208
	Q, R, G	C	-12P	12	90.9	EEPROM	256	4	132, 164	160, 192, 208
	Q, R, G	C	-12	12	90.9	EEPROM	256	4	132, 164	160, 192, 208
	Q, R, G	C, I	-15	15	76.9	EEPROM	256	4	132, 164	160, 192, 208
	Q, R, G	C, I	-20	20	62.5	EEPROM	256	4	132, 164	160, 192, 208

Notes:
(1) Preliminary information is shown for some devices. Consult the *MAX 7000 Programmable Logic Device Family Data Sheet* in this data book for more information, or contact Altera Customer Marketing for the most current device information.
(2) Package configurations (contact Altera Customer Marketing for information on device package availability):
L: Plastic J-lead chip carrier (PLCC)
T: Plastic thin quad flat pack (TQFP)
Q: Plastic quad flat pack (PQFP)
R: Power quad flat pack (RQFP)
G: Ceramic pin-grid array (PGA)
(3) Operating temperature:
C: Commercial (0° C to 70° C)
I: Industrial (–40° C to 85° C)
(4) The EPM7032V is a 3.3-V version of the EPM7032.
(5) The -12 and -12P speed grade versions are available for EPM7160E, EPM7192E, and EPM7256E devices only.
(6) The -20 speed grade version is available for EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices only.

FLASHlogic Devices

Table 7 provides information on the FLASHlogic family of medium-density, high-speed, feature-rich PLDs. These innovative devices are based on CMOS technology with SRAM process shadowed by FLASH processes. FLASHlogic devices feature in-circuit reconfigurability (ICR), ISP, and on-board RAM.

Table 7. FLASHlogic Devices *Note (1)*

Device	Package (2)	Temp. (3)	t_{PD1} (ns)	f_{CNT} (MHz)	Process	Logic Cells/ Registers	Max. On-Board RAM (Bits)	Ded. Inputs	I/O Pins	Number of Pins
EPX880	L, Q	C	10	80	SRAM, FLASH	80	10,240	24	60, 80	84, 132
	Q	I	12	64.5	SRAM, FLASH	80	10,240	24	80	132
EPX8160	Q	C	10	80	SRAM, FLASH	160	20,480	52	120	208
	Q	C, I	12	64.5	SRAM, FLASH	160	20,480	52	120	208

Notes:
(1) Consult the *FLASHlogic Programmable Logic Device Family Data Sheet* in this data book for more information, or contact Altera Customer Marketing for the most current device information.
(2) Package configurations (contact Altera Customer Marketing for information on device package availability):
L: Plastic J-lead chip carrier (PLCC)
Q: Plastic quad flat pack (PQFP)
(3) Operating temperature:
C: Commercial (0° C to 70° C)
I: Industrial (–40° C to 85° C)

MAX 5000 Devices

Table 8 provides information on the MAX 5000 family of low-cost PLDs, which are suitable for implementing functions ranging from 20-pin address decoders to 100-pin custom LSI peripherals. These devices combine the speed, ease-of-use, and familiarity of PAL devices with the density of programmable gate arrays. MAX 5000 devices are EPROM-based and fabricated on CMOS technology.

Table 8. MAX 5000 Devices *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Process	Logic Cells/ Registers	Ded. Inputs	I/O Pins	Number of Pins
EPM5032	D, P, S, J, L	C	-15	15	76.9	EPROM	32	8	16	28
	D, P, J, L	C	-20	20	62.5	EPROM	32	8	16	28
	P, L	C, I	-25	25	50.0	EPROM	32	8	16	28
EPM5064	J, L	C	-1	25	50.0	EPROM	64	8	28	44
	L	C	-2	30	40.0	EPROM	64	8	28	44
	L	C, I	*(4)*	35	33.3	EPROM	64	8	28	44
EPM5128	J, L, G	C	-1	25	50.0	EPROM	128	8	52	68
	L	C, I	-2	30	40.0	EPROM	128	8	52	68
	L, G	C, I	*(4)*	35	33.3	EPROM	128	8	52	68
EPM5130	J, L, Q, G	C	-1	25	50.0	EPROM	130	20	48, 64	84, 100
	J, L, Q, G	C	*(4)*	35	33.3	EPROM	130	20	48, 64	84, 100
EPM5192	J, L, G	C	-1	25	50.0	EPROM	192	8	64	84
	L, G	C, I	*(4)*	35	33.3	EPROM	192	8	64	84

Notes:

(1) Consult the *MAX 5000 Programmable Logic Device Family Data Sheet* in this data book for more information, or contact Altera Customer Marketing for the most current device information.

(2) Package configurations (contact Altera Customer Marketing for information on device package availability):
- D: Ceramic dual in-line package (CerDIP)
- P: Plastic dual in-line package (PDIP)
- S: Plastic small-outline integrated circuit (SOIC)
- J: Ceramic J-lead chip carrier (JLCC)
- L: Plastic J-lead chip carrier (PLCC)
- Q: Plastic quad flat pack (PQFP)
- G: Ceramic pin-grid array (PGA)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)

(4) The ordering code for this device does not have a speed grade suffix.

Classic Devices

Table 9 provides information on the industry-standard Classic family of PLDs. These EPROM-based devices provide propagation delays (t_{PD}) as low as 10 ns and counter rates as high as 100 MHz. Classic devices are fabricated on CMOS technology.

Table 9. Classic Devices *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Process	Logic Cells/ Registers	Ded. Inputs	I/O Pins	Number of Pins
EP610	P, S, L	C	-15	15	83.3	EPROM	16	4	16	24, 28
	P	C	-20	20	62.5	EPROM	16	4	16	24
	D, P, S, L	C	-25	25	40.0	EPROM	16	4	16	24, 28
	D, P	C, I	-30	30	33.3	EPROM	16	4	16	24
EP610I	D, P, L	C	-10	10	100	EPROM	16	4	16	24, 28
	P	C	-12	12	83	EPROM	16	4	16	28
	D	C	-15	15	66	EPROM	16	4	16	24
EP910	P, L	C	-30	30	33.3	EPROM	24	12	24	40
	D, P, L	C, I	-35	35	28.6	EPROM	24	12	24	40
EP910I	P, L	C, I	-12	12	77	EPROM	24	12	24	40
	D, L	C, I	-15	15	67	EPROM	24	12	24	40
	P	C	-25	25	40	EPROM	24	12	24	40
EP1810	L	C	-20	20	50.0	EPROM	48	16	48	68
	L	C, I	-25	25	40.0	EPROM	48	16	48	68
	L, G	C	-35	35	28.6	EPROM	48	16	48	68
	L	C, I	-45	45	22.2	EPROM	48	16	48	68

Notes:

(1) Consult the *Classic EPLD Family Data Sheet* in this data book for more information, or contact Altera Customer Marketing for the most current device information.

(2) Package configurations (contact Altera Customer Marketing for information on device package availability):
- D: Ceramic dual in-line package (CerDIP)
- P: Plastic dual in-line package (PDIP)
- S: Plastic small-outline integrated circuit (SOIC)
- J: Ceramic J-lead chip carrier (JLCC)
- L: Plastic J-lead chip carrier (PLCC)
- G: Ceramic pin-grid array (PGA)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)

3.3-V Devices

Table 10 provides information on Altera's general-purpose PLDs for 3.3-V applications. These devices are ideal for low-power systems, such as battery-operated instruments and notebook computers.

Table 10. 3.3-Volt Devices *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	Process	Logic Cells/ Registers	Ded. Inputs	I/O Pins	Number of Pins
EPF8282AV	L, T	C	A-3	SRAM	208 / 282	4	68, 78	84, 100
Note (4)	L, T	C, I	A-4	SRAM	208 / 282	4	68, 78	84, 100
EPM7032V	L, T	C	-12	EEPROM	32	4	36	44
Note (5)	L, T	C	-15	EEPROM	32	4	36	44
	L, T	C, I	-20	EEPROM	32	4	36	44
EPM7128SV	L, T, Q	C	-10	EEPROM	128	4	64, 84, 100	84, 100, 160
	L, T, Q	C	-15	EEPROM	128	4	64, 84, 100	84, 100, 160

Notes:
(1) Preliminary information is shown for some devices. Consult individual device data sheets in this data book for more information, or contact Altera Customer Marketing for the most current device information.
(2) Package configurations (contact Altera Customer Marketing for information on device package availability):
L: Plastic J-lead chip carrier (PLCC)
T: Plastic thin quad flat pack (TQFP)
(3) Operating temperature:
C: Commercial (0° C to 70° C)
I: Industrial (–40° C to 85° C)
(4) The EPF8282AV is a 3.3-V version of the EPF8282A.
(5) The EPM7032V is a 3.3-V version of the EPM7032.

Devices with 3.3-V or 5.0-V I/O Pins

Table 11 provides information on Altera devices with 3.3-V or 5.0-V I/O pins. These devices—ideal for 3.3-V, 5.0-V, and mixed-voltage systems—have two sets of V_{CC} pins: one for internal and input operation and another for I/O output drivers.

Table 11. Devices with 3.3-V/5.0-V I/O Pins

Device Family	Mixed-Voltage Devices
FLEX 10K	All devices
FLEX 8000	EPF8636A (except 84-pin PLCC packages), EPF8820A, EPF81188A, and EPF81500A
MAX 9000	All devices
MAX 7000	All devices except 44-pin packages
FLASHlogic	All devices

PCI-Compliant Devices

Altera offers devices that meet the 33-MHz peripheral component interconnect (PCI) bus standard. See Table 12. Refer to *Application Brief 140 (PCI Compliance of Altera Devices)* and *Application Note 41 (PCI Bus Applications in Altera Devices)* for more information.

Table 12. PCI-Compliant Devices (Part 1 of 2) *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	Process	Logic Cells/ Registers	Ded. Inputs	I/O Pins	Number of Pins
EPF10K10	L, T, Q	C	-3	SRAM	576 / 720	6	59, 107, 134	84, 144, 208
	L, T, Q	C, I	-4	SRAM	576 / 720	6	59, 107, 134	84, 144, 208
EPF10K20	R	C	-3	SRAM	1,152 / 1,344	6	147, 189	208, 240
	R	C, I	-4	SRAM	1,152 / 1,344	6	147, 189	208, 240
EPF10K30	R, B	C	-3	SRAM	1,728 / 1,968	6	147, 189, 246	208, 240, 356
	R, B	C, I	-4	SRAM	1,728 / 1,968	6	147, 189, 246	208, 240, 356
EPF10K40	R	C	-3	SRAM	2,304 / 2,576	6	147, 189	208, 240
	R	C, I	-4	SRAM	2,304 / 2,576	6	147, 189	208, 240
EPF10K50	R, G, B	C	-3	SRAM	2,880 / 3,184	6	189, 274, 310	240, 356, 403
	R, G, B	C, I	-4	SRAM	2,880 / 3,184	6	189, 274, 310	240, 356, 403
EPF10K70	R, G	C	-3	SRAM	3,744 / 4,096	6	189, 358	240, 503
	R, G	C, I	-4	SRAM	3,744 / 4,096	6	189, 358	240, 503
EPF10K100	G	C	-3	SRAM	4,992 / 5,392	6	406	503
	G	C, I	-4	SRAM	4,992 / 5,392	6	406	503
EPF8282A	L, T	C	A-2	SRAM	208 / 282	4	68, 78	84, 100
	L, T	C, I	A-3	SRAM	208 / 282	4	68, 78	84, 100
EPF8452A	L, T, Q, G	C	A-2	SRAM	336 / 452	4	68, 120	84, 100, 160
	L, T, Q, G	C, I	A-3	SRAM	336 / 452	4	68, 120	84, 100, 160
EPF8636A	L, Q, R, G	C	A-2	SRAM	504 / 636	4	68, 110, 136	84, 160, 192, 208
	L, Q, R, G	C, I	A-3	SRAM	504 / 636	4	68, 110, 136	84, 160, 192, 208
EPF8820A	T, Q, G, B	C	A-2	SRAM	672 / 820	4	120, 152	144, 160, 192, 208, 225
	T, Q, G, B	C, I	A-3	SRAM	672 / 820	4	120, 152	144, 160, 192, 208, 225
EPF81188A	Q, R, G	C	A-2	SRAM	1,008 / 1,188	4	148, 184	208, 232, 240
	Q, R, G	C, I	A-3	SRAM	1,008 / 1,188	4	148, 184	208, 232, 240
EPF81500A	R, G	C	A-2	SRAM	1,296 / 1,500	4	181, 208	240, 280, 304
	R, G	C, I	A-3	SRAM	1,296 / 1,500	4	181, 208	240, 280, 304
EPM9320	L, R, G	C	-12	EEPROM	320 / 484	4	60, 132, 168	84, 208, 280
EPM9400	L, R	C	-12	EEPROM	400 / 580	4	59, 139, 159	84, 208, 240
EPM7032,	L, T	C	-5	EEPROM	32	4	36	44
EPM7032S	L, T	C	-6	EEPROM	32	4	36	44
	L, T	C	-7	EEPROM	32	4	36	44
EPM7064,	L, T, Q	C	-6	EEPROM	64	4	36, 52, 68	44, 68, 84, 100
EPM7064S	L, T, Q	C	-7	EEPROM	64	4	36, 52, 68	44, 68, 84, 100

Table 12. PCI-Compliant Devices (Part 2 of 2) *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	Process	Logic Cells/ Registers	Ded. Inputs	I/O Pins	Number of Pins
EPM7096,	L, T, Q	C	-6	EEPROM	96	4	52, 64, 76	68, 84, 100
EPM7096S	L, T, Q	C	-7	EEPROM	96	4	52, 64, 76	68, 84, 100
EPM7128E,	L, T, Q	C	-7	EEPROM	128	4	68, 84, 100	84, 100, 160
EPM7128S	L, T, Q	C, I	-10P	EEPROM	128	4	68, 84, 100	84, 100, 160
Note (4)	L, T, Q	C, I	-10	EEPROM	128	4	68, 84, 100	84, 100, 160
EPM7160E	L, T, Q	C	-7	EEPROM	160	4	64, 84, 104	84, 100, 160
EPM7160S	L, T, Q	C, I	-10P	EEPROM	160	4	64, 84, 104	84, 100, 160
Note (4)	L, T, Q	C, I	-10	EEPROM	160	4	64, 84, 104	84, 100, 160
EPM7192E	Q, G	C	-10	EEPROM	192	4	124	160
EPM7192S	Q, G	C	-12P	EEPROM	192	4	124	160
Note (5)								
EPM7256E	Q, R, G	C	-10	EEPROM	256	4	132, 164	160, 192, 208
EPM7256S	Q, R, G	C	-12P	EEPROM	256	4	132, 164	160, 192, 208
Note (5)								
EPX880	L, Q	C	-10	SRAM, FLASH	80	24	60, 80	84, 132
EPX8160	Q	C	-10	SRAM, FLASH	160	52	120	208

Notes:

(1) Preliminary information is shown for some devices. Consult individual device data sheets in this data book for more information, or contact Altera Customer Marketing for the most current device information.

(2) Package configurations (contact Altera Customer Marketing for information on device package availability):
- T: Plastic thin quad flat pack (TQFP)
- Q: Plastic quad flat pack (PQFP)
- R: Power quad flat pack (RQFP)
- G: Ceramic pin-grid array (PGA)
- B: Ball-grid array (BGA)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)

(4) The -10P speed grade version is available for EPM7128E and EPM7160E devices only.
The -10 speed grade version is PCI-compliant for EPM7128S and EPM7160S devices only.

(5) The -12P speed grade version is available for EPM7192E and EPM7256E devices only.

June 1996

FLEX 10K Embedded Programmable Logic Family Data Sheet


ALTERA
FLEX
EPF10K20
EPF10K40
EPF10K10
EPF10K100
EPF10K30
EPF10K50
EPF10K70

FLEX 10K

Embedded Programmable Logic Family

June 1996, ver. 2 — Data Sheet

Features...

- The industry's first embedded programmable logic device (PLD) family, providing system integration in a single device
  - Embedded array for implementing megafunctions, such as efficient memory and specialized logic functions
  - Logic array for general logic functions
- High density
  - 10,000 to 100,000 typical gates (see Table 1)
  - 720 to 5,392 registers
  - 6,144 to 24,576 RAM bits, all of which can be used without reducing logic capacity
- System-level features
  - ClockLock and ClockBoost option for reduced clock delay/skew and clock multiplication
  - In-circuit reconfigurability (ICR) via external configuration EPROM, intelligent controller, or Joint Test Action Group (JTAG) port
  - Fully compliant with the peripheral component interconnect (PCI) standard
  - Built-in JTAG boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990
  - 3.3- or 5.0-V I/O pins on all devices in pin-grid array (PGA), ball-grid array (BGA), and 208-pin quad flat pack (QFP) packages
  - Able to bridge between 3.3-V and 5.0-V systems
  - Low power consumption (less than 1 mA in standby mode)

Preliminary Information

Table 1. FLEX 10K Device Features

Feature	EPF10K10	EPF10K20	EPF10K30	EPF10K40	EPF10K50	EPF10K70	EPF10K100
Typical gates (logic & RAM)	10,000	20,000	30,000	40,000	50,000	70,000	100,000
Usable gates	7,000 to 31,000	15,000 to 63,000	22,000 to 69,000	29,000 to 93,000	36,000 to 116,000	46,000 to 118,000	62,000 to 158,000
Logic elements	576	1,152	1,728	2,304	2,880	3,744	4,992
Logic array blocks	72	144	216	288	360	468	624
Embedded array blocks	3	6	6	8	10	9	12
Total RAM bits	6,144	12,288	12,288	16,384	20,480	18,432	24,576
Flipflops	720	1,344	1,968	2,576	3,184	4,096	5,392
Max. user I/O pins	134	189	246	189	310	358	406

...and More Features

- Flexible interconnect
  - FastTrack Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions
  - Tri-state emulation that implements internal tri-state nets
  - Up to six global clock signals and four global clear signals
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Open-drain option on each I/O pin
  - Programmable output slew-rate control to reduce switching noise
- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Flexible package options
  - Available in a variety of packages with 84 to 503 pins (see Table 2)
  - Pin-compatibility with other FLEX 10K devices in the same package
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS II development system for 486- and Pentium-based PCs and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, VeriBest, and Viewlogic

Table 2. FLEX 10K Package Options & I/O Count *Note (1)*

Device	84-Pin PLCC	144-Pin TQFP	208-Pin PQFP & RQFP	240-Pin RQFP	356-Pin BGA	403-Pin PGA	503-Pin PGA
EPF10K10	59	107	134				
EPF10K20			147	189			
EPF10K30			147	189	246		
EPF10K40			147	189			
EPF10K50				189	274	310	
EPF10K70				189			358
EPF10K100							406

Note:
(1) Contact Altera for up-to-date information on package availability.

General Description

Altera's FLEX 10K devices are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 100,000 gates, the FLEX 10K family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device. Table 3 shows FLEX 10K performance for typical applications, as well as the logic elements (LEs) and the embedded array blocks (EABs) required.

Table 3. FLEX 10K Performance

Application	Resources Used		Performance			Unit
	LEs	EABs	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade *Note (1)*	
16-bit loadable counter	16	0	104	97	67	MHz
16-bit accumulator	16	0	104	97	67	MHz
16-to-1 multiplexer, *Note (2)*	10	0	9.4	10.6	13.2	ns
4 × 4 multiplier, *Note (3)*	0	1	105	86	66	MHz
8 × 8 multiplier, *Note (3)*	25	4	30	24	18	MHz
256 × 8 RAM, *Note (3)*	0	1	105	86	66	MHz

Notes:
(1) The -5 speed grade is available for EPF10K50 devices only.
(2) This application uses combinatorial inputs and outputs.
(3) This application uses registered inputs and outputs.

The FLEX 10K architecture is similar to that of embedded gate arrays, the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional "sea-of-gates" architecture. In addition, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. However, the embedded megafunctions typically cannot be customized, limiting the designer's options. In contrast, FLEX 10K devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide data-path manipulation, and data transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10K devices are configured at system power-up with data stored in an Altera serial Configuration EPROM device or provided by a system controller. Altera offers the EPC1 Configuration EPROM, which configures FLEX 10K devices via a serial data stream. Configuration data can also be downloaded from system RAM or from Altera's BitBlaster serial download cable. After a FLEX 10K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 200 ms, real-time changes can be made during system operation.

FLEX 10K devices contain an optimized microprocessor interface that permits the microprocessor to configure FLEX 10K devices serially, in parallel, synchronously, or asynchronously. The interface also enables the microprocessor to treat a FLEX 10K device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.

Go to the *Configuration EPROMs for FLEX Devices Data Sheet* in this data book and *AN 59 (Configuring FLEX 10K Devices)* for more information.

FLEX 10K devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; full simulation and worst-case timing analysis; and device configuration. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

Go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book for more information.

Functional Description

Each FLEX 10K device contains an embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 2,048 bits, which can be used to create RAM, ROM, FIFO functions, or dual-port RAM. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

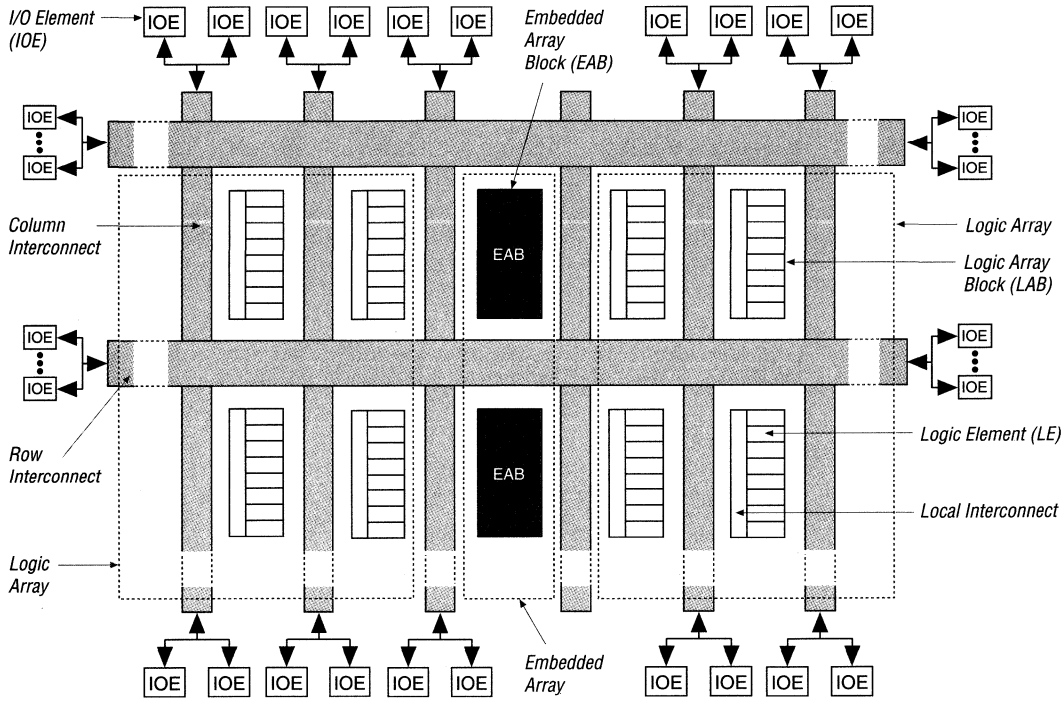
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10K devices, and to and from device pins, are provided by the FastTrack Interconnect, a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times of less than 8 ns and hold times of 0 ns; as outputs, these registers provide clock-to-output times of less than 8 ns. IOEs provide a variety of features, such as JTAG programming support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 1 shows a block diagram of the FLEX 10K architecture. Each group of LEs is combined into an LAB; LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each row and column of the FastTrack Interconnect.

Figure 1. FLEX 10K Device Block Diagram



FLEX 10K devices provide six dedicated inputs that drive the control inputs of the flipflops to ensure the efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

Embedded Array Block

The EAB facilitates the implementation of common gate array megafunctions. The EAB is a flexible block of RAM with registers on the input and output ports. However, the size and flexibility of the EAB make it suitable for more than memory, including functions such as multipliers, vector scalars, and error correction circuits. These functions can be combined in applications such as digital filters and microcontrollers.

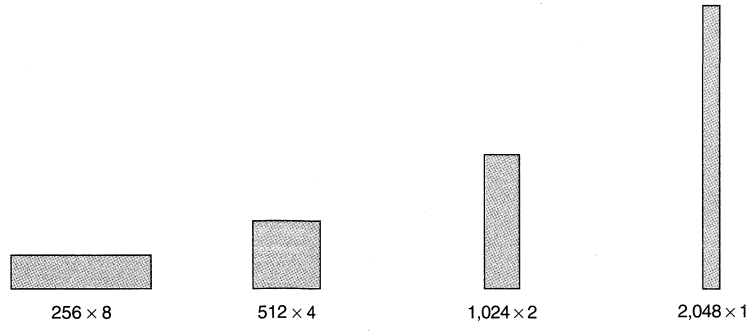
Logic functions are implemented by programming the EAB with a read-only pattern during configuration, creating a large LUT. In this LUT, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions is faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enable designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a 4 × 4 multiplier with eight inputs and eight outputs.

The EAB has advantages over FPGAs, which implement blocks of on-board RAM as arrays of small, distributed RAM blocks. These FPGA RAM blocks contain delays that are less predictable as the size of the RAM increases. In addition, FPGA RAM blocks are prone to routing problems because the small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns. Dedicated EABs are easy to use and provide fast, predictable delays.

The EAB can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the write enable (WE) signal of the RAM, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the EAB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. A circuit using the EAB's self-timed RAM need only meet the setup and hold time specifications of the global clock.

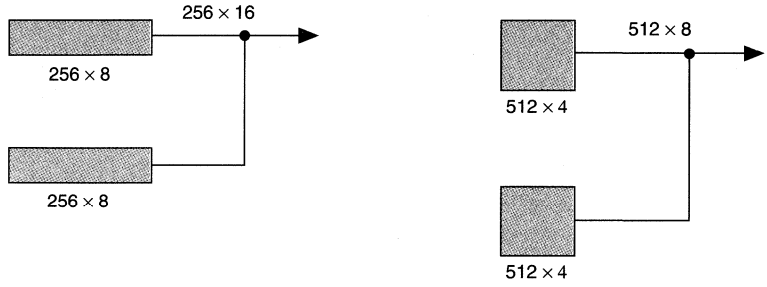
When used as RAM, each EAB can be configured in any of the following sizes: 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. See Figure 2.

Figure 2. EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 8 RAMs can be combined to form a 256 × 16 RAM; two 512 × 4 blocks of RAM can be combined to form a 512 × 8 RAM. If necessary, all EABs in a device can be cascaded to form a single RAM. EABs can be cascaded to form RAMs of up to 2,048 words without impacting timing. Altera's MAX+PLUS II software automatically combines EABs to implement a designer's RAM specifications. See Figure 3.

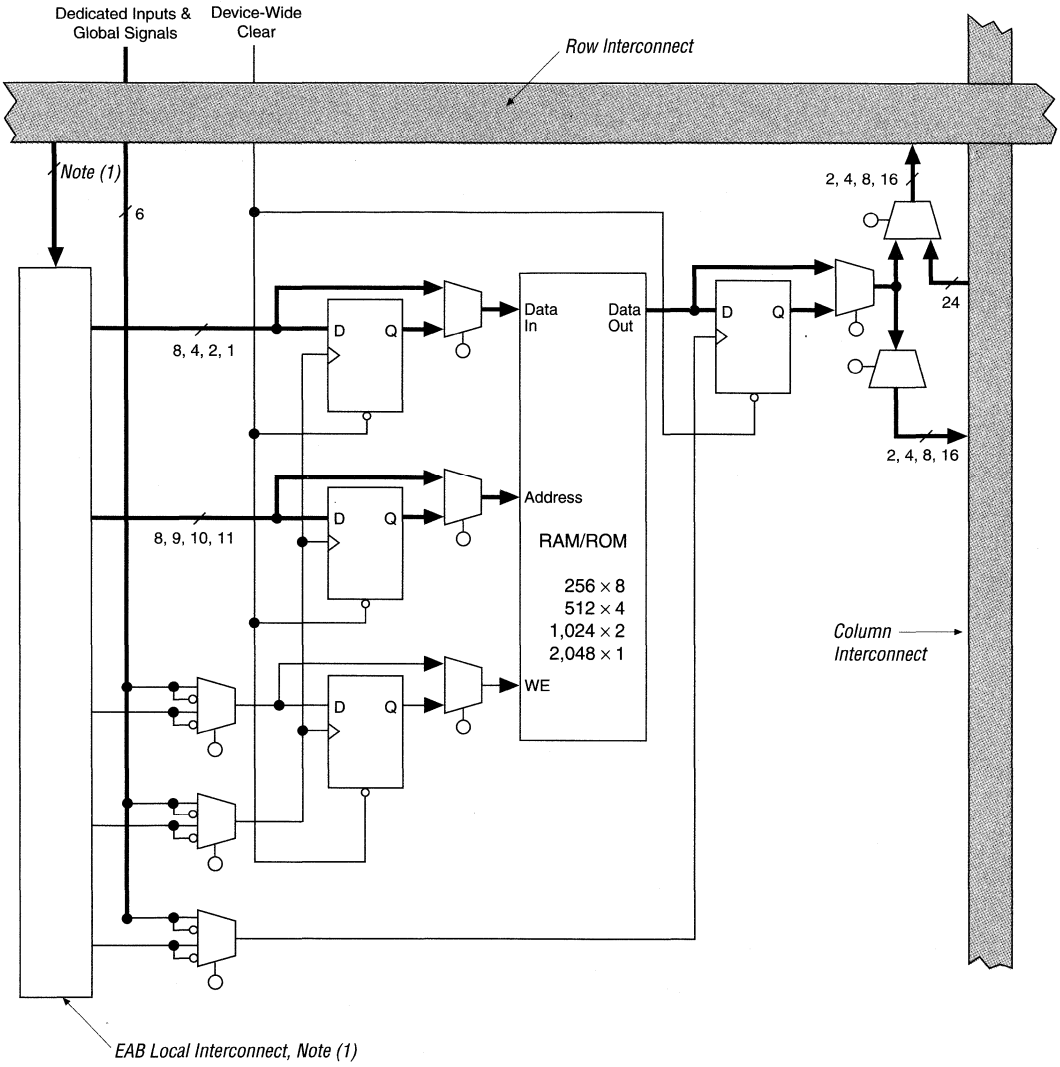
Figure 3. Examples of Combining EABs



The EAB provides flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and WE signals. The global signals and the EAB local interconnect can drive the WE signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the WE signal or the EAB clock signals.

Each EAB is fed by a row interconnect, and can drive out to row and column interconnects. Each EAB output can drive either of two row channels and either of two column channels; the unused row channel can be driven by a column channel. This feature increases the routing resources available for EAB outputs. See Figure 4.

Figure 4. FLEX 10K Embedded Array Block



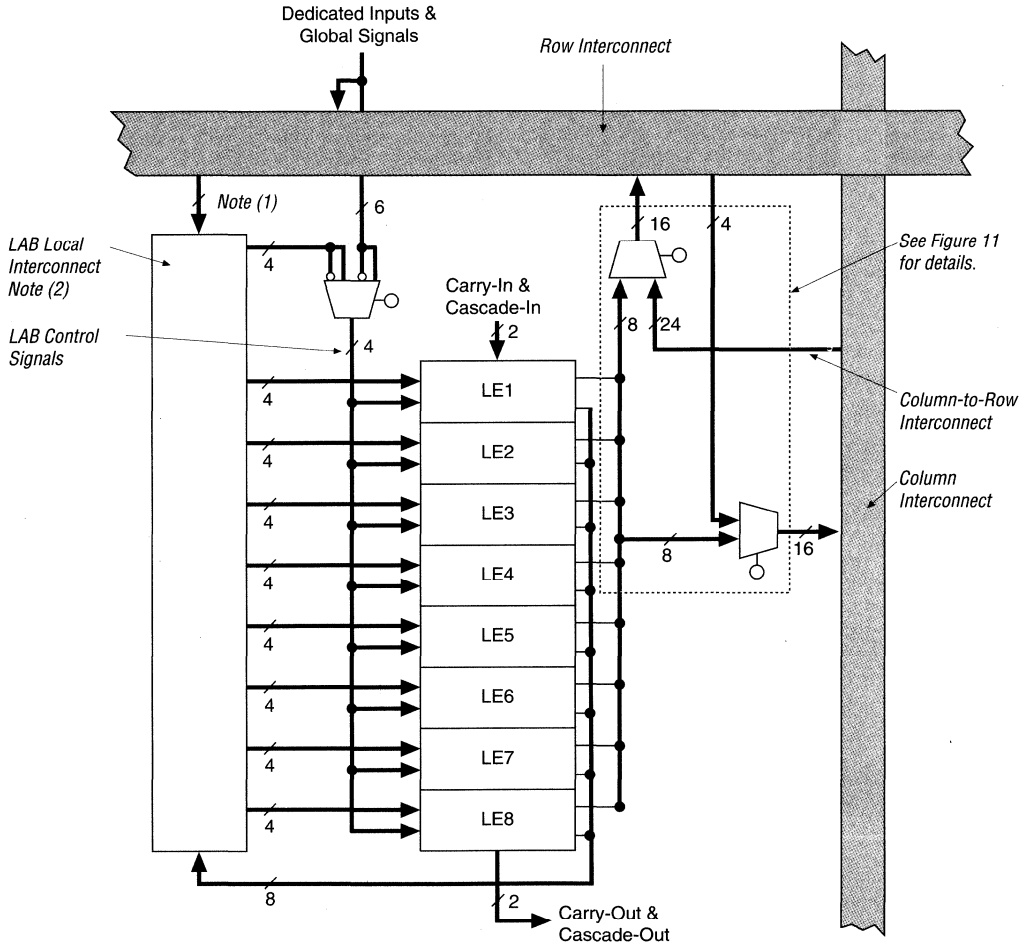
Note:

(1) EPF10K10, EPF10K20, EPF10K30, EPF10K40, and EPF10K50 devices have 22 EAB local interconnect channels; EPF10K70 and EPF10K100 devices have 26.

Logic Array Block

A LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10K architecture, facilitating efficient routing with optimum device utilization and high performance. See Figure 5.

Figure 5. FLEX 10K LAB



Notes:

(1) EPF10K10, EPF10K20, EPF10K30, EPF10K40, and EPF10K50 devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K70 and EPF10K100 devices have 26.

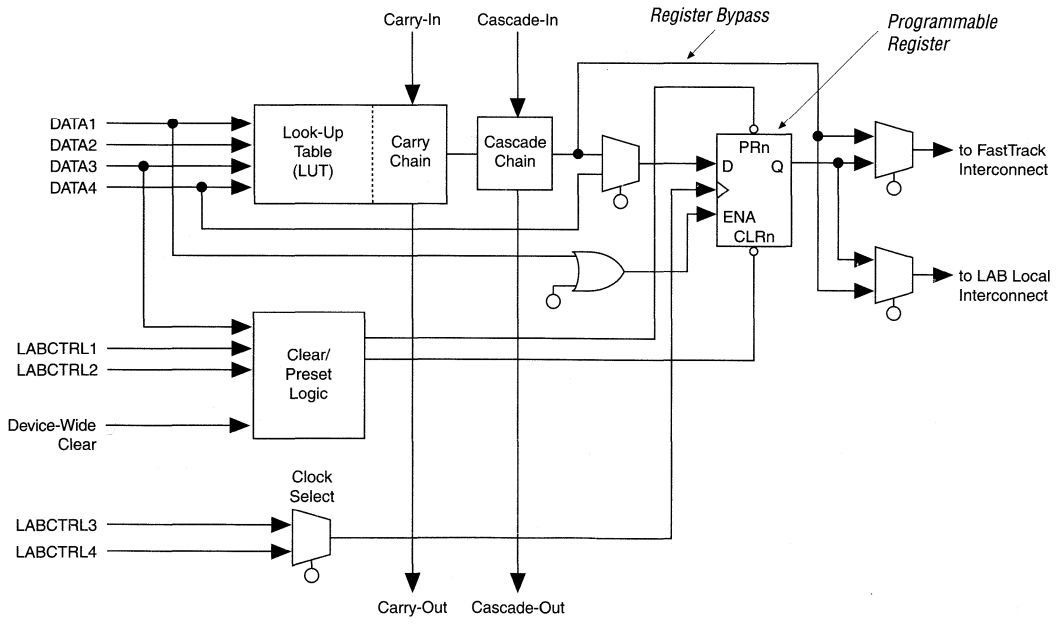
(2) EPF10K10, EPF10K20, EPF10K30, EPF10K40, and EPF10K50 devices have 30 LAB local interconnect channels; EPF10K70 and EPF10K100 devices have 34.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated using LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

Figure 6. FLEX 10K Logic Element



The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the output of the LE.

The LE has two outputs that drive the interconnect; one drives the local interconnect and the other drives either the row or column FastTrack Interconnect. The two outputs can be controlled independently; for example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The FLEX 10K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

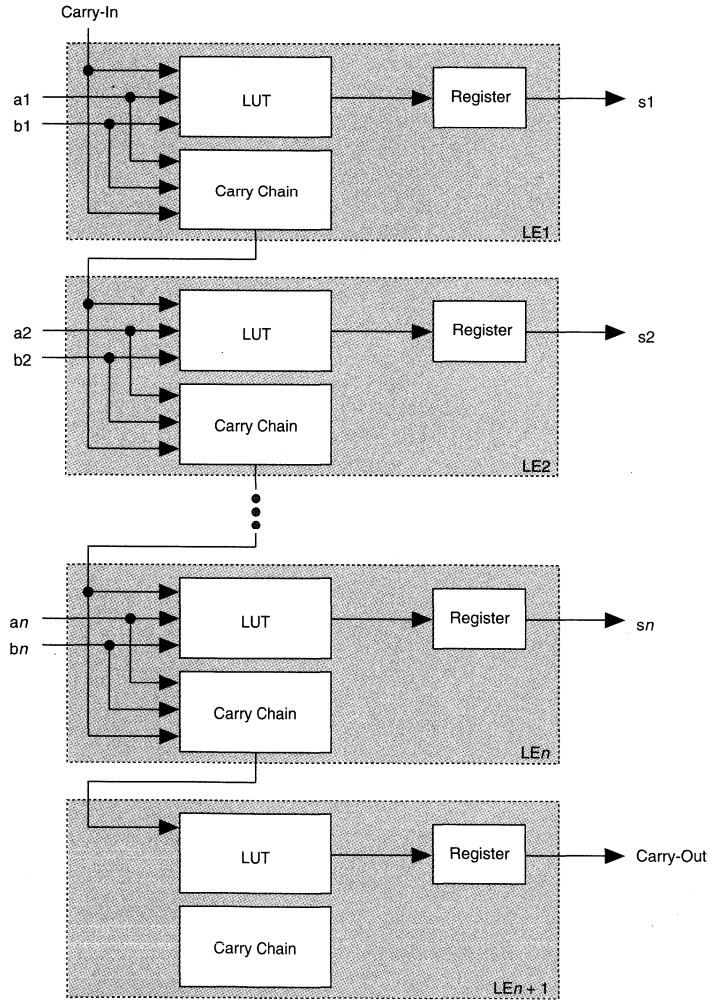
Carry Chain

The carry chain provides a very fast (less than 0.5 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 10K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the MAX+PLUS II Compiler during design processing, or manually by the designer during design entry.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. The last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For example, in the EPF10K50, the carry chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB.

Figure 7 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 7. Carry Chain Operation



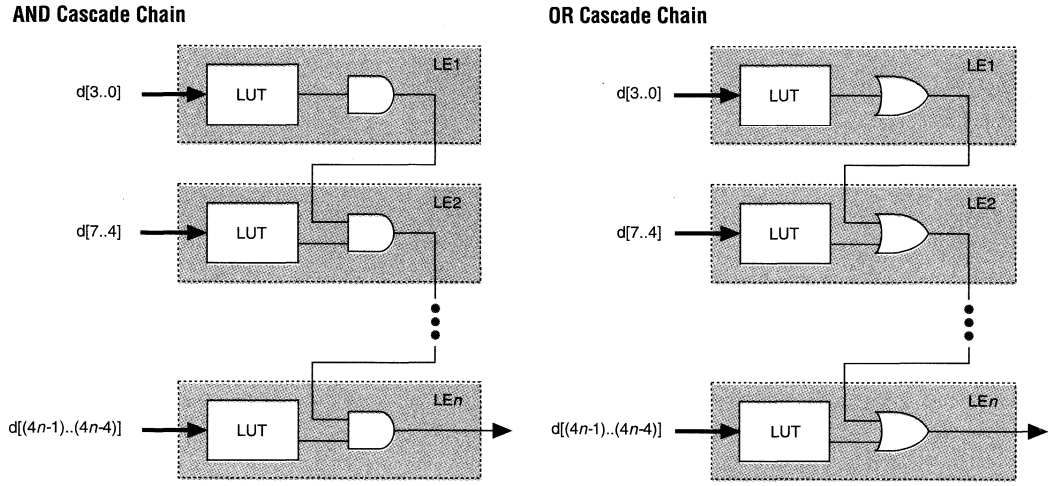
Cascade Chain

With the cascade chain, the FLEX 10K architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 1.1 ns per LE. Cascade chain logic can be created automatically by the MAX+PLUS II Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are automatically implemented by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. The last LE of the first LAB in a row cascades to the first LE of the third LAB. The cascade chain does not cross the center of the row. For example, in the EPF10K50, the cascade chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB. This break is due to the EAB's placement in the middle of the row.

Figure 8 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with n LEs. The LUT delay is approximately 3.0 ns; the cascade chain delay is 1.1 ns. With the cascade chain, 6.3 ns is needed to decode a 16-bit address.

Figure 8. Cascade Chain Operation



LE Operating Modes

The FLEX 10K LE can operate in one of the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

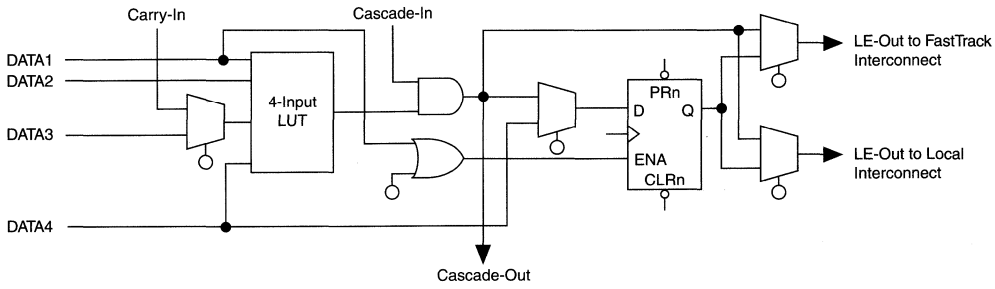
Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can be further enhanced by tailoring the design for the operating mode that supports the intended application.

The architecture provides a synchronous clock enable to the register in all four modes. `DATA1` can be set to synchronously enable the register, providing easy implementation of fully synchronous designs.

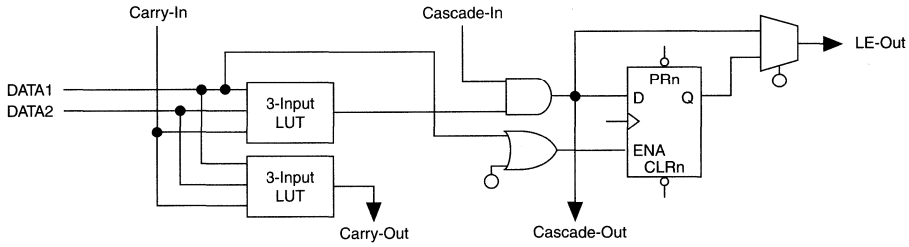
Figure 9 shows the LE operating modes.

Figure 9. FLEX 10K LE Operating Modes

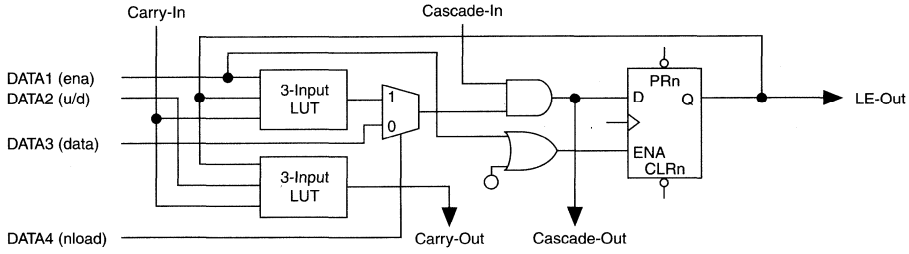
Normal Mode



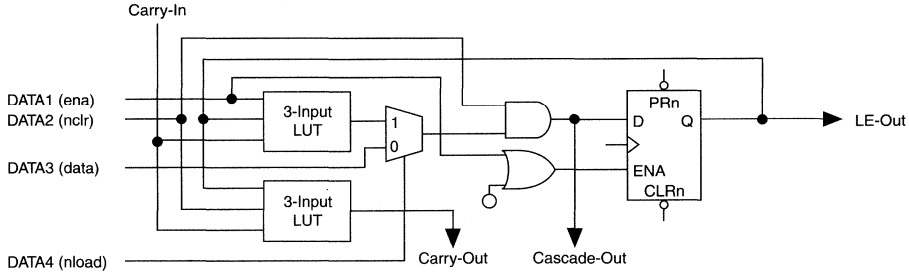
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. To support register packing, the LE has two outputs; one drives the local interconnect and the other drives the FastTrack Interconnect.

The LUT and the register in the LE can be used independently. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect at the same time. Alternatively, in a packed LE, the register can drive the FastTrack Interconnect while the LUT drives the local interconnect, or vice versa.

The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a 3-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a 4-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear and preset signals in the LE.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a 3-input function; the other generates a carry output. As shown in Figure 9 on page 46, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. MAX+PLUS II automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. The register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

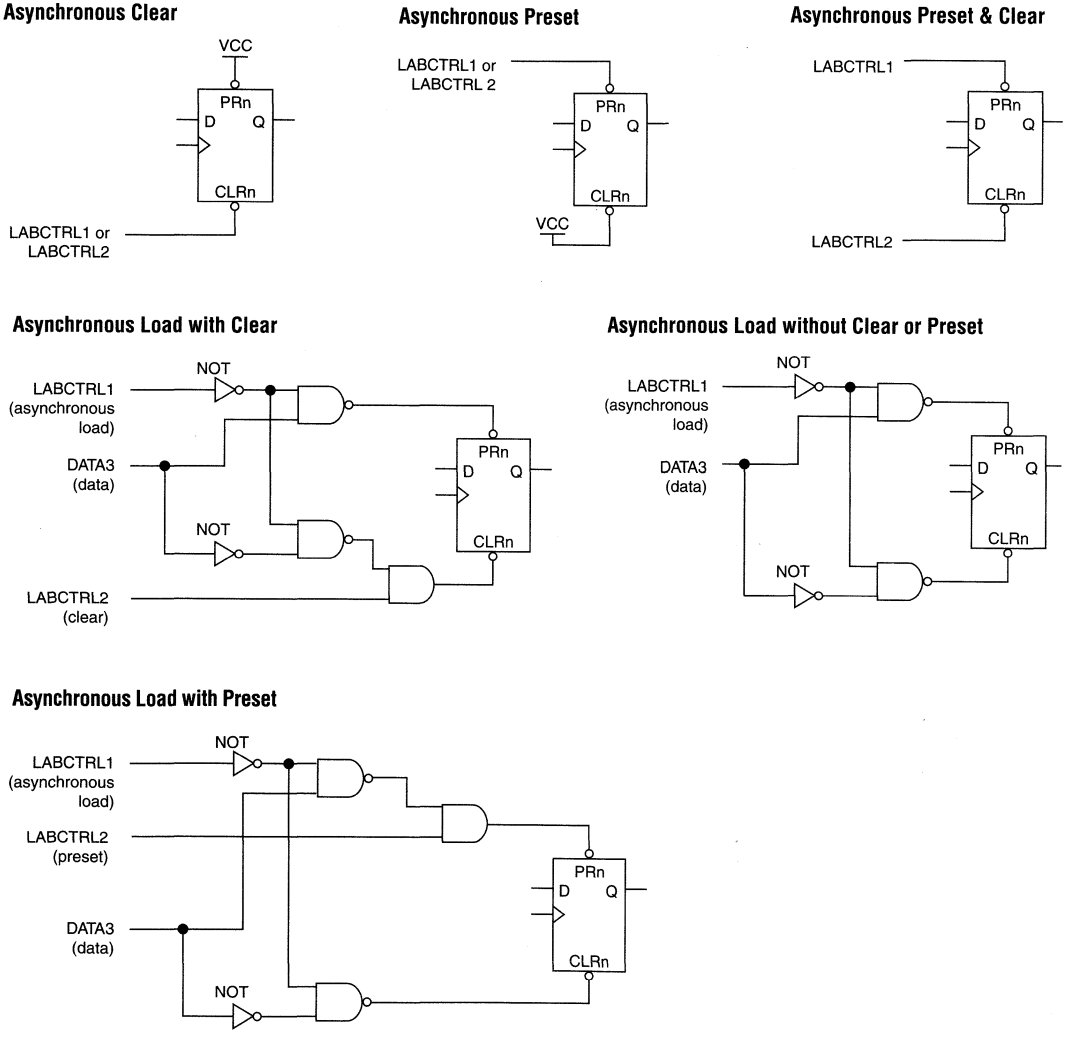
During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

In addition to the six clear and preset modes, FLEX 10K devices provide a device-wide clear pin that can reset all registers in the device. This pin is set during design entry. In any of the clear and preset modes, the device-wide clear overrides all other signals. See Figure 10.

Figure 10. LE Clear & Preset Modes



Asynchronous Clear

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, MAX+PLUS II can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to VCC, therefore, asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with the preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. MAX+PLUS II inverts the signal that drives DATA3 to account for the inversion of the register's output.

Asynchronous Load without Clear or Preset

When implementing an asynchronous load without the preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

FastTrack Interconnect

In the FLEX 10K architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

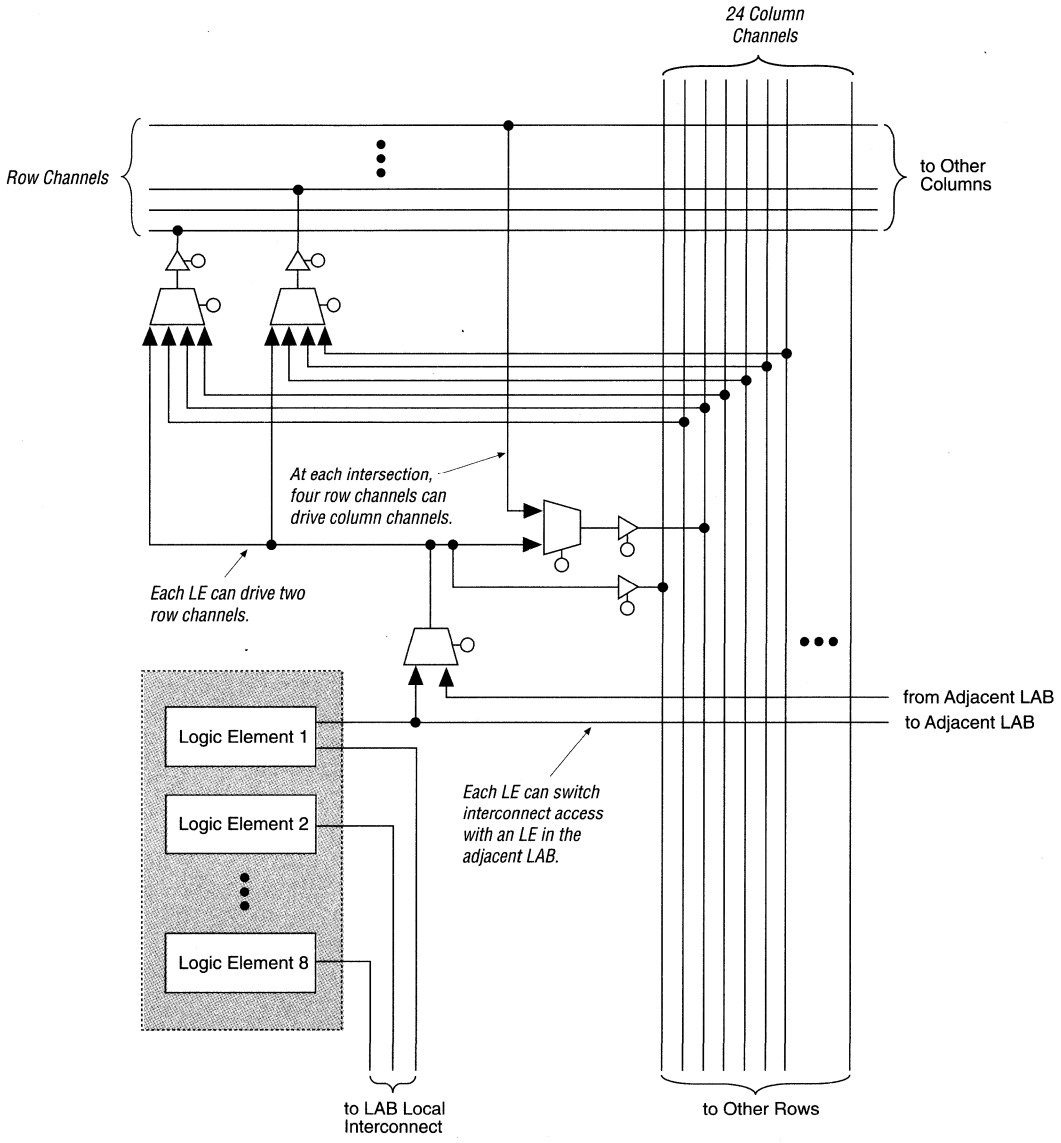
The FastTrack Interconnect consists of column and row interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the device. The column interconnect routes signals between rows and can drive I/O pins.

A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in an LAB drive the row interconnect.

Each column of LABs is served by a dedicated column interconnect. The column interconnect can then drive I/O pins or drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must be routed to the row interconnect before it can enter an LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, an LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This routing flexibility enables routing resources to be used more efficiently. See Figure 11.

Figure 11. LAB Connections to Row & Column Interconnect



For improved routability, the row interconnect is comprised of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in one-half of the row. The EAB can be driven by the half-channels in the left half of the row and by the full channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 4 summarizes the FastTrack Interconnect resources available in each FLEX 10K device.

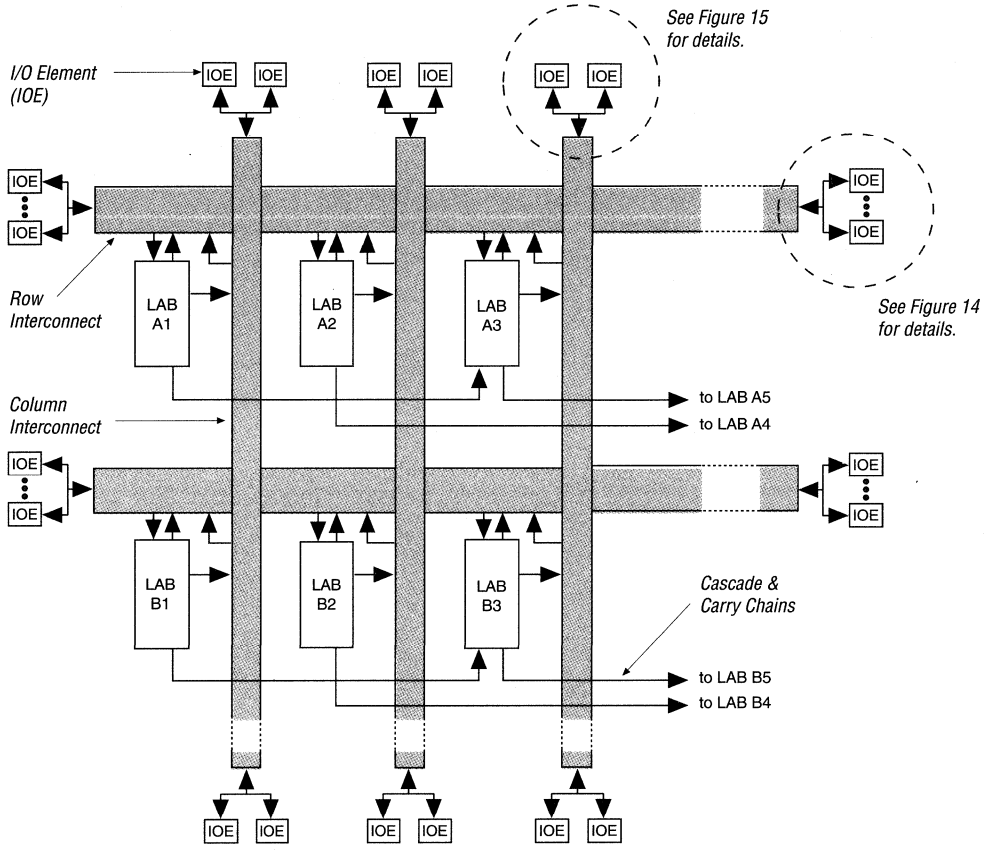
Table 4. FLEX 10K FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF10K10	3	144	24	24
EPF10K20	6	144	24	24
EPF10K30	6	216	36	24
EPF10K40	8	216	36	24
EPF10K50	10	216	36	24
EPF10K70	9	312	52	24
EPF10K100	12	312	52	24

In addition to general-purpose I/O pins, FLEX 10K devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. However, the use of dedicated inputs as data inputs can introduce additional delay into the control signal network.

Figure 12 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number representing the column. For example, LAB B3 is in row B, column 3.

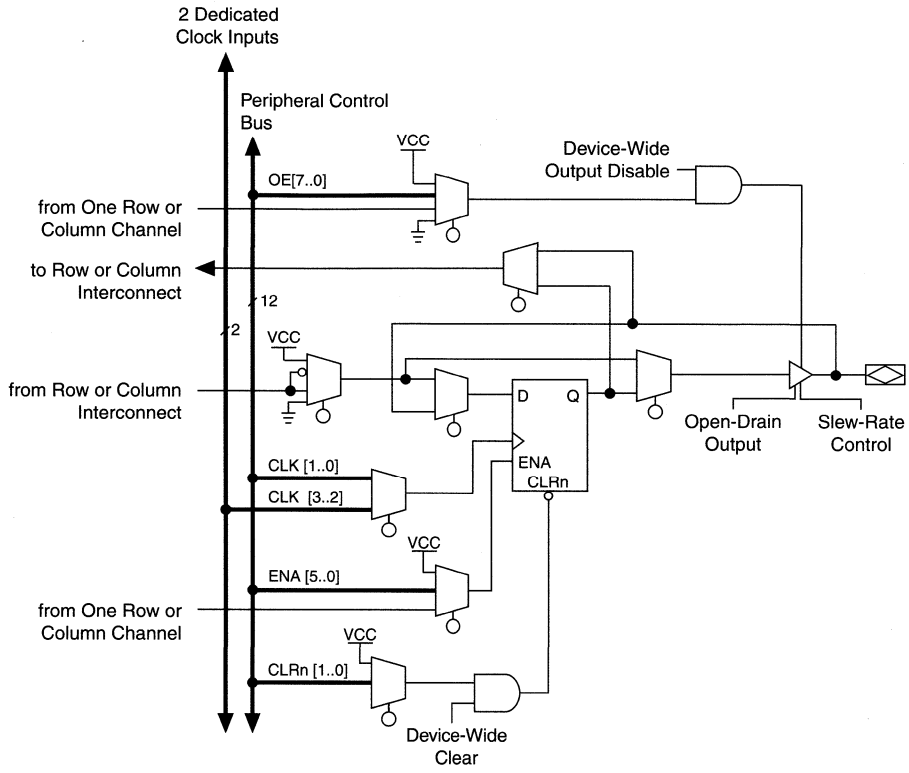
Figure 12. FLEX 10K Device Interconnect Resources



I/O Element

An I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect where appropriate. Figure 13 shows the IOE block diagram.

Figure 13. FLEX 10K Device I/O Element



The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4.5 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. Each pin can also be specified as open-drain on a pin-by-pin basis.

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by a specific LE. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, an LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal.

Table 5 lists the sources for each peripheral control signal, shows how the output enable, clock enable, clock, and clear signals share the 12 peripheral control signals, and the rows that can drive the global signals.

Table 5. Peripheral Bus Sources

Peripheral Control Signal	EPF10K10	EPF10K20	EPF10K30	EPF10K40	EPF10K50	EPF10K70	EPF10K100
OE0	Row A	Row A	Row A	Row A	Row A	Row A	Row A
OE1	Row A	Row B	Row B	Row C	Row B	Row B	Row C
OE2	Row B	Row C	Row C	Row D	Row D	Row D	Row E
OE3	Row B	Row D	Row D	Row E	Row F	Row I	Row G
OE4	Row C	Row E	Row E	Row F	Row H	Row G	Row I
OE5	Row C	Row F	Row F	Row G	Row J	Row H	Row K
CLKENA0/CLK0/ GLOBAL0	Row A	Row A	Row A	Row B	Row A	Row E	Row B
CLKENA1/OE6/ GLOBAL1	Row A	Row B	Row B	Row C	Row C	Row C	Row D
CLKENA2/CLR0	Row B	Row C	Row C	Row D	Row E	Row B	Row F
CLKENA3/OE7/ GLOBAL2	Row B	Row D	Row D	Row E	Row G	Row F	Row H
CLKENA4/CLR1	Row C	Row E	Row E	Row F	Row I	Row H	Row J
CLKENA5/CLK1/ GLOBAL3	Row C	Row F	Row F	Row H	Row J	Row E	Row L

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Table 5. The internally generated signal can drive the global signal, providing the same low-skew, low-delay characteristics for an internally generated signal as for a signal driven by an input. This feature is ideal for internally generated clear or clock signals with high fan-out.

A device-wide output disable pin is an active-low pin that can be used to tri-state all pins on the device. This option can be set in the design file. Additionally, the registers in the IOE can be reset by the device-wide clear pin.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Eight IOEs connect to each side of each row channel. See Figure 14.

Figure 14. FLEX 10K Row-to-IOE Connections

The values for m and n are provided in Table 6.

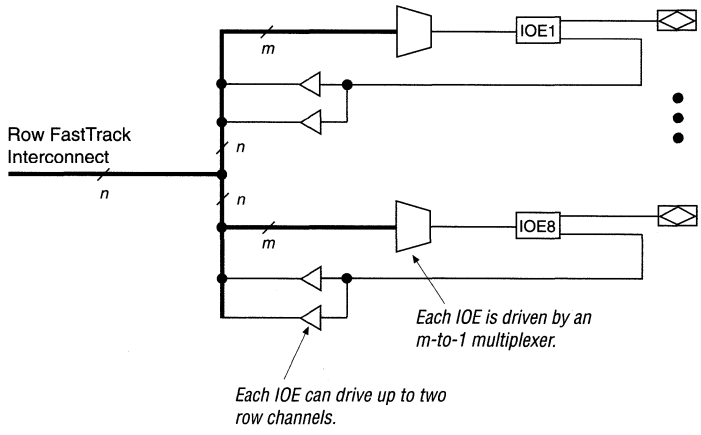


Table 6 lists the FLEX 10K row-to-IOE interconnect resources.

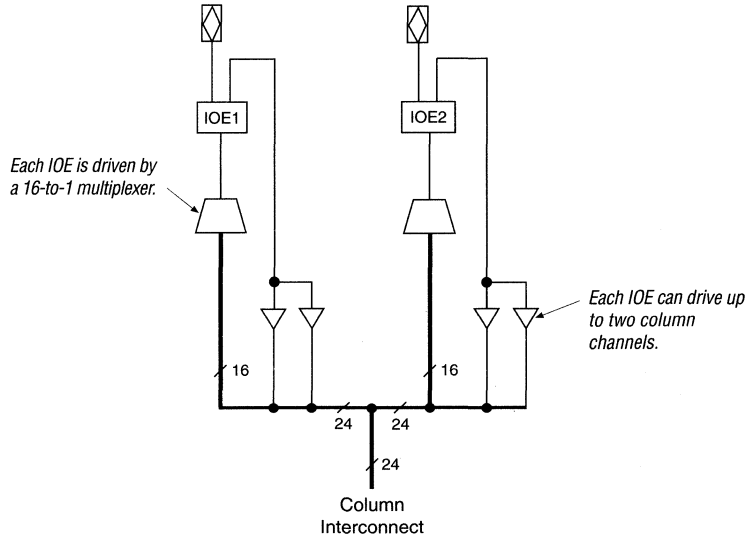
Table 6. FLEX 10K Row-to-IOE Interconnect Resources

Device	Channels per Row (*n*)	Row Channel per Pin (*m*)
EPF10K10	144	18
EPF10K20	144	18
EPF10K30	216	27
EPF10K40	216	27
EPF10K50	216	27
EPF10K70	312	39
EPF10K100	312	39

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be connected to 16 of the 24 column channels via a 16-to-1 multiplexer. The set of 16 column channels that each IOE can access is different for each IOE. See Figure 15.

Figure 15. FLEX 10K Column-to-IOE Connections



ClockLock & ClockBoost

To support high-speed designs, specially marked FLEX 10K devices offer optional ClockLock and ClockBoost circuitry. These circuits are phase-locked loops (PLLs) and can be used to increase design speed and reduce resource usage. The ClockLock circuitry is a synchronizing PLL that reduces the clock delay and skew within a device, improving setup and clock-to-output times. With the ClockBoost circuitry, which provides a clock multiplier, designers can easily implement time-domain-multiplexed logic to reduce resource usage in a design.

3.3- or 5.0-V I/O Pin Operation

Some FLEX 10K devices can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCINT} pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs. The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}.

Open-Drain Output Option

FLEX 10K devices provide an optional open-drain (electrically equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

JTAG Operation

All FLEX 10K devices provide JTAG BST circuits that comply with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG PROGRAM instruction.

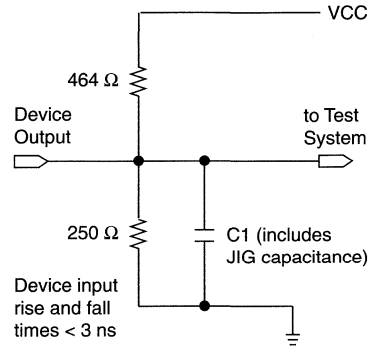
Go to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)* for more information.

Generic Testing

Each FLEX 10K device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 10K devices are made under conditions equivalent to those shown in Figure 16. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 16. FLEX 10K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



FLEX 10K Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		Plastic and power quad flat pack packages, under bias		135	° C

FLEX 10K Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	*Note (4)*	3.00	3.60	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 10K Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V, *Note (7)*	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V, *Note (7)*	2.4			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V, *Note (8)*			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V, *Note (8)*			0.45	V
I_I	Input pin leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load		500		µA

FLEX 10K Device Capacitance *Note (9)*

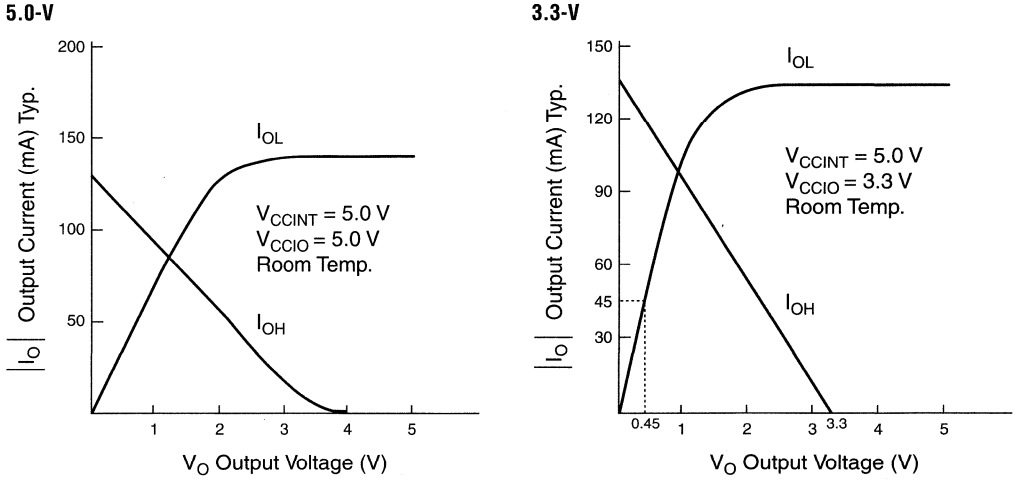
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range versions.
(4) Maximum V_{CC} rise time is 100 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) Operating conditions: V_{CCINT} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(7) The I_{OH} parameter refers to high-level TTL output current.
(8) The I_{OL} parameter refers to low-level TTL output current.
(9) Capacitance is sample-tested only.

Figure 17 shows the typical output drive characteristics of FLEX 10K devices with 5.0-V and 3.3V V_{CCIO}. The output driver is compatible with the *PCI Local Bus Specification,* version 2.0.

Figure 17. Output Drive Characteristics for Devices with 5.0-V V_{CCIO}



Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row could be calculated by adding the following parameters:

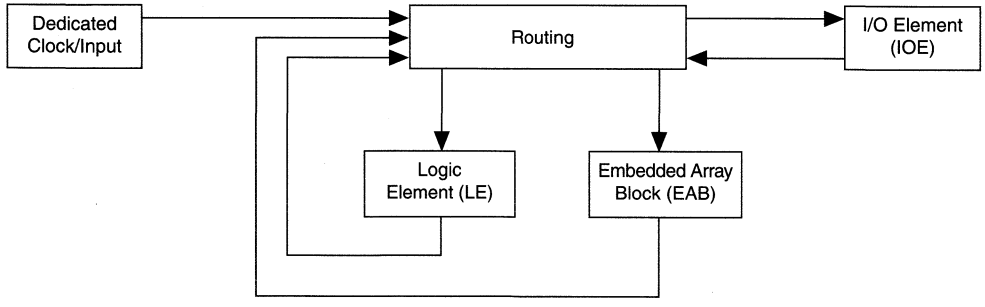
- LE register clock-to-output delay (t_{CO})
- Routing delay ($t_{SAMEROW}$)
- LE look-up table delay (t_{LUT})
- LE register setup time (t_{SU})

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 18 shows the overall timing model, which maps the possible routing paths to and from the various elements of the FLEX 10K device.

Figure 18. FLEX 10K Device Timing Model



Figures 19 through 21 show the delays that correspond to various paths and functions within the LE, IOE, and EAB timing models.

Figure 19. FLEX 10K Device LE Timing Model

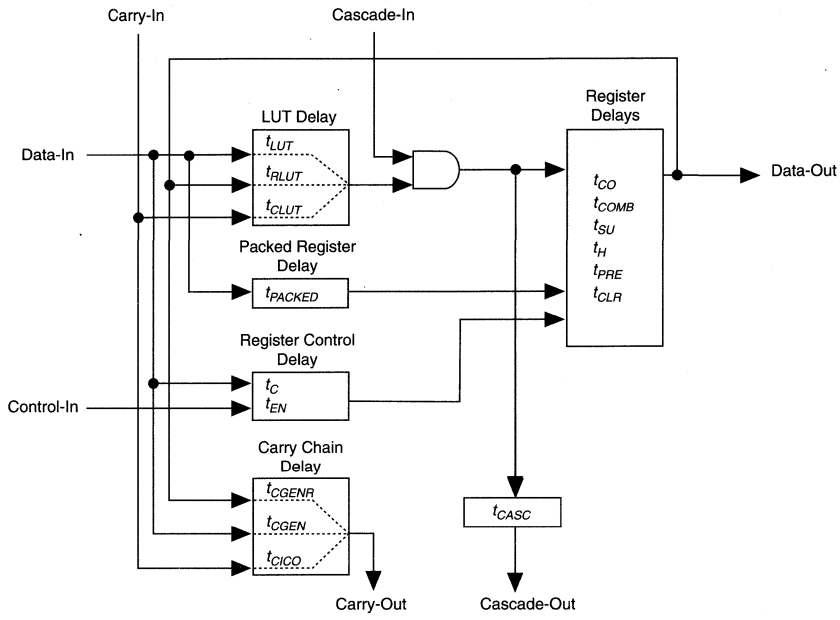


Figure 20. FLEX 10K Device IOE Timing Model

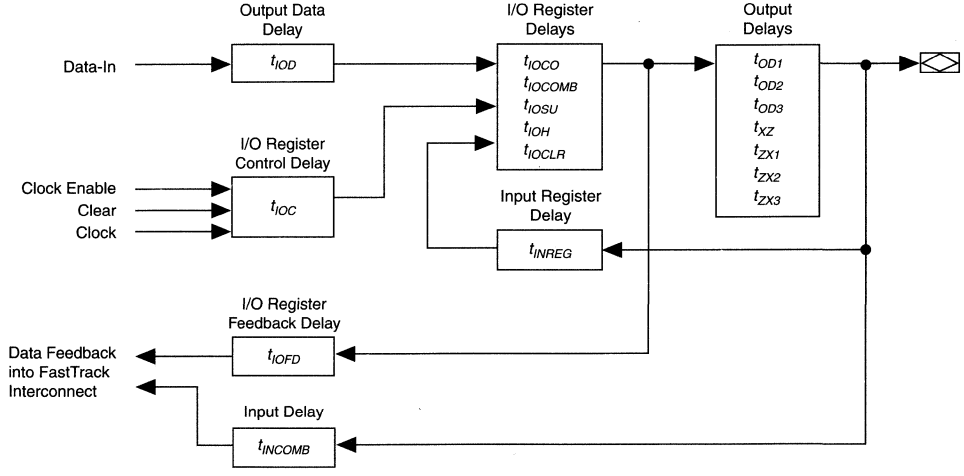
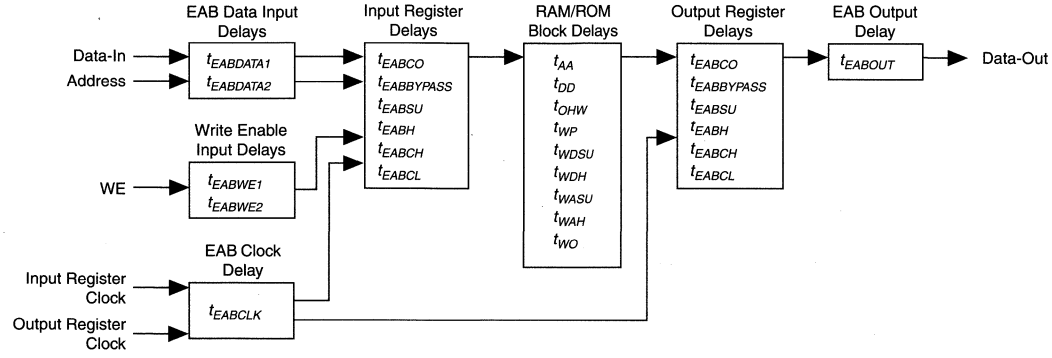


Figure 21. FLEX 10K Device EAB Timing Model



Tables 7 through 11 describe the FLEX 10K internal timing parameters. These internal timing parameters are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and timing analysis. Tables 12 and 13 describe FLEX 10K external timing parameters.

Table 7. LE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{LUT}	LUT delay for data-in	
t_{CLUT}	LUT delay for carry-in	
t_{RLUT}	LUT delay for LE register feedback	
t_{PACKED}	Data-in to packed register delay	
t_{EN}	LE register enable delay	
t_{CICO}	Carry-in to carry-out delay	
t_{CGEN}	Data-in to carry-out delay	
t_{CGENR}	LE register feedback to carry-out delay	
t_{CASC}	Cascade-in to cascade-out delay	
t_{C}	LE register control signal delay	
t_{CO}	LE register clock-to-output delay	
t_{COMB}	Combinatorial delay	
t_{SU}	LE register setup time before clock	
t_{H}	LE register hold time before clock	
t_{PRE}	LE register preset delay	
t_{CLR}	LE register clear delay	

Table 8. IOE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register data setup time before clock	
t_{IOH}	IOE register data hold time after clock	
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF *Note (2)*
t_{OD2}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *Note (3)*
t_{OD3}	Output buffer and pad delay, Slow slew rate = on	C1 = 35 pF *Note (4)*
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF *Note (2)*
t_{ZX2}	IOE output buffer enable delay, Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *Note (3)*
t_{ZX3}	IOE output buffer enable delay, Slow slew rate = off	C1 = 35 pF *Note (4)*
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{IOFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Table 9. EAB Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
t_{EABWE1}	Write enable delay to EAB for combinatorial input	
t_{EABWE2}	Write enable delay to EAB for registered input	
t_{EABCLK}	EAB register clock delay	
t_{EABCO}	EAB register clock-to-output delay	
$t_{EABBYPASS}$	Bypass register delay	
t_{EABSU}	EAB register setup time before clock	
t_{EABH}	EAB register hold time after clock	
t_{EABCH}	Clock high time	
t_{EABCL}	Clock low time	
t_{AA}	Address access delay	
t_{WP}	Write pulse width	
t_{WDSU}	Data setup time before falling edge of write pulse	*Note (5)*
t_{WDH}	Data hold time after falling edge of write pulse	*Note (5)*
t_{WASU}	Address setup time before rising edge of write pulse	*Note (5)*
t_{WAH}	Address hold time after falling edge of write pulse	*Note (5)*
t_{WO}	Write enable to data output valid delay	
t_{DD}	Data-in to data-out valid delay	
t_{EABOUT}	Data-out delay	

Table 10. EAB Timing Macroparameters (Part 1 of 2) *Note (6)*

Symbol	Parameter	Equation	Conditions
t_{EABAA}	EAB address access delay	$t_{EABDATA1} + t_{EABBYPASS} + t_{AA} + t_{EABBYPASS} + t_{EABOUT}$	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	$t_{EABDATA1} + t_{EABBYPASS} + t_{AA} + t_{EABBYPASS} + t_{EABOUT}$	
$t_{EABRCREG}$	EAB synchronous read cycle time	$t_{EABCO} + t_{AA} + t_{EABSU}$	
t_{EABWP}	EAB write pulse width	t_{WP}	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	$t_{WASU} + t_{WP} + t_{WAH}$	
$t_{EABWCREG}$	EAB synchronous write cycle time	$t_{EABCO} + t_{DD} + t_{EABSU}$	
t_{EABDD}	EAB data-in to data-out valid delay	$t_{EABDATA1} + t_{EABBYPASS} + t_{DD} + t_{EABBYPASS} + t_{EABOUT}$	

Table 10. EAB Timing Macroparameters (Part 2 of 2) *Note (6)*			
Symbol	**Parameter**	**Equation**	**Conditions**
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	$t_{EABCLK} + t_{EABCO} + t_{EABOUT}$	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	$t_{EABSU} + t_{EABDATA2} - t_{EABCLK}$	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	$t_{EABH} + t_{EABCLK} - t_{EABDATA2}$	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	$t_{EABSU} + t_{EABWE2} - t_{EABCLK}$	
t_{EABWEH}	EAB WE hold time after clock when using input register	$t_{EABH} + t_{EABCLK} - t_{EABWE2}$	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	$t_{WDSU} + (t_{EABDATA1} + t_{EABBYPASS}) - (t_{EABWE1} + t_{EABBYPASS})$	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	$t_{WDH} + (t_{EABWE1} + t_{EABBYPASS}) - (t_{EABDATA1} + t_{EABBYPASS})$	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	$t_{WASU} + (t_{EABDATA1} + t_{EABBYPASS}) - (t_{EABWE1} + t_{EABBYPASS})$	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	$t_{WAH} + (t_{EABWE1} + t_{EABBYPASS}) - (t_{EABDATA1} + t_{EABBYPASS})$	
t_{EABWO}	EAB write enable to data output valid delay	$t_{EABWE1} + t_{EABBYPASS} + t_{WO} + t_{EABBYPASS} + t_{EABOUT}$	

Table 11. Routing Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	*Note (7)*
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	*Note (7)*
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	*Note (7)*
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	*Note (7)*
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	*Note (7)*
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	*Note (7)*
t_{DIN2LE}	Delay from dedicated input pin to LE control input	*Note (7)*
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	*Note (7)*
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE clock	*Note (7)*

Table 12. External Reference Timing Parameters *Note (8)*

Symbol	Parameter	Conditions
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	*Note (9)*

Table 13. External Timing Parameters *Note (10)*

Symbol	Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (11)*

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2) Operating conditions: V_{CCIO} = 5.0 V ± 5% for commercial use.
V_{CCIO} = 5.0 V ± 10% for industrial use.
(3) Operating conditions: V_{CCIO} = 3.3 V ± 5% for commercial use.
V_{CCIO} = 3.3 V ± 10% for industrial use.
(4) Operating conditions: V_{CCIO} = 3.3 V or 5.0 V.
(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(8) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(9) Contact Altera Applications at (800) 800-EPLD for test circuit specifications and test conditions.
(10) These timing parameters are sample tested only.
(11) This parameter is a guideline that is sample-tested only and based on extensive device characterization. This parameter applies for both global and non-global clocking and for LE, EAB, and IOE registers.

Figures 22 and 23 show the asynchronous and synchronous timing waveforms, respectively, for the EAB macroparameters in Table 10.

Figure 22. EAB Asynchronous Timing Waveforms

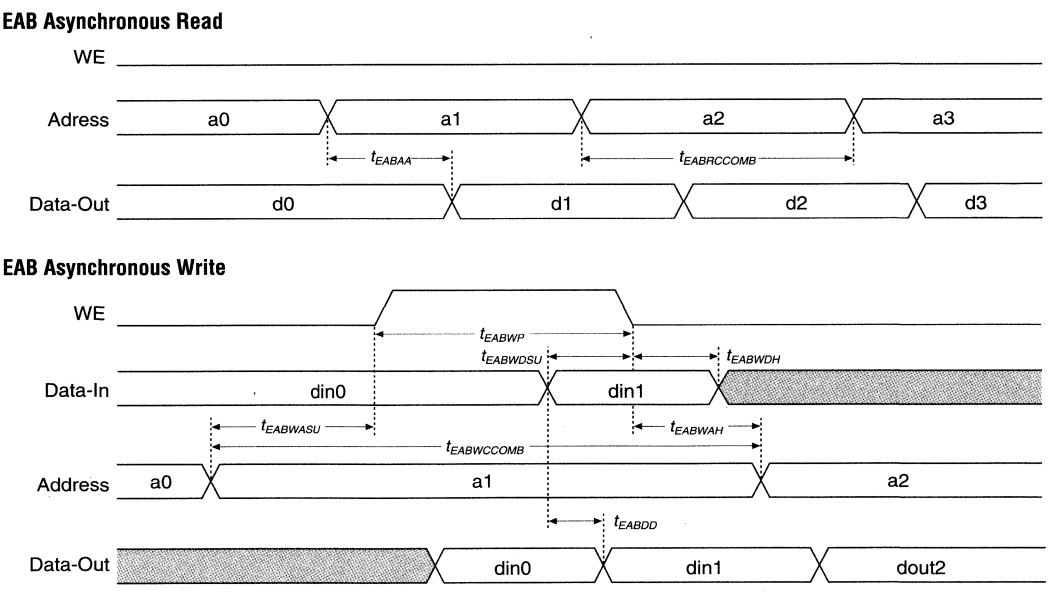
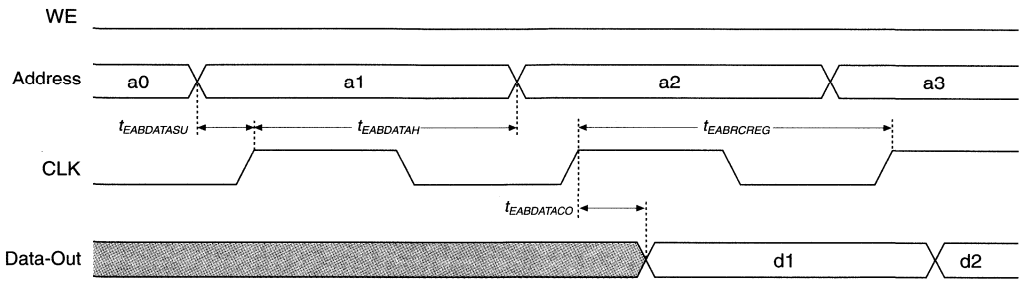
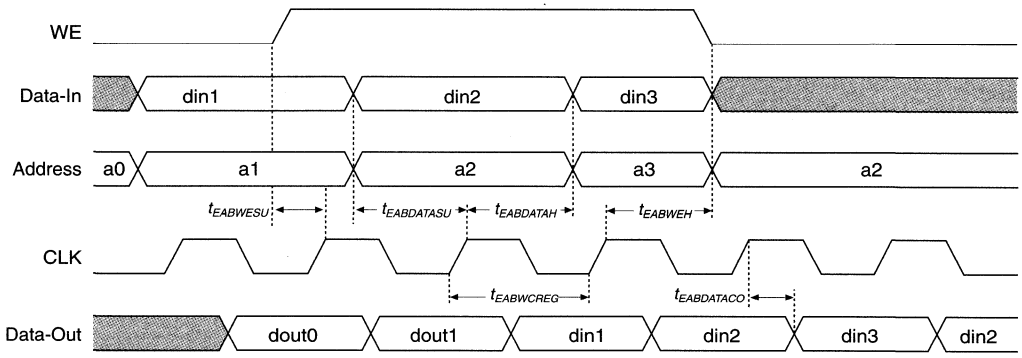


Figure 23. EAB Synchronous Timing Waveforms

EAB Synchronous Read



EAB Synchronous Write



FLEX 10K Device Internal Timing Parameters

LE Timing Microparameters *Note (1)*							
Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		1.5		1.9		2.5	ns
t_{CLUT}		0.8		1.0		1.4	ns
t_{RLUT}		1.3		1.5		2.2	ns
t_{PACKED}		0.7		0.8		1.1	ns
t_{EN}		0.7		0.8		1.1	ns
t_{CICO}		0.3		0.3		0.5	ns
t_{CGEN}		1.2		1.5		2.0	ns
t_{CGENR}		0.2		0.2		0.3	ns
t_{CASC}		1.1		1.2		1.5	ns
t_{C}		1.1		1.4		1.9	ns
t_{CO}		0.2		0.2		0.3	ns
t_{COMB}		0.6		0.7		0.9	ns
t_{SU}	2.2		2.7		3.7		ns
t_{H}	0.0		0.0		0.0		ns
t_{PRE}		1.2		1.4		1.9	ns
t_{CLR}		0.9		1.1		1.4	ns

FLEX 10K Device IOE Timing Microparameters *Note (1)*							
Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		1.3		1.6		2.0	ns
t_{IOC}		1.2		1.4		1.8	ns
t_{IOCO}		0.2		0.2		0.3	ns
t_{IOCOMB}		0.2		0.3		0.3	ns
t_{IOSU}	3.8		4.6		5.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.1		1.3		1.7	ns
t_{OD1}		6.1		6.2		6.4	ns
t_{OD2}		6.4		6.6		7.0	ns
t_{OD3}		8.7		9.5		10.5	ns
t_{XZ}		1.4		1.7		2.1	ns
t_{ZX1}		1.4		1.7		2.1	ns
t_{ZX2}		1.7		2.1		2.7	ns
t_{ZX3}		4.0		5.0		6.2	ns
t_{INREG}		4.9		5.9		7.4	ns
t_{IOFD}		1.0		1.1		1.2	ns
t_{INCOMB}		1.0		1.1		1.1	ns

FLEX 10K Device EAB Internal Microparameters							
Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		2.4		3.0		3.9	ns
$t_{EABDATA2}$		4.7		5.8		7.5	ns
t_{EABWE1}		2.4		3.0		3.9	ns
t_{EABWE2}		4.7		5.8		7.5	ns
t_{EABCLK}		0.9		1.1		1.4	ns
t_{EABCO}		0.6		0.7		0.9	ns
$t_{EABBYPASS}$		0.8		1.0		1.3	ns
t_{EABSU}	1.8		2.2		2.9		ns
t_{EABH}	0.0		0.0		0.0		ns
t_{EABCH}	4.3		5.3		6.9		ns
t_{EABCL}	1.6		1.9		2.5		ns
t_{AA}		7.1		8.7		11.3	ns
t_{WP}	4.7		5.8		7.5		ns
t_{WDSU}	5.9		7.3		9.5		ns
t_{WDH}	0.0		0.0		0.0		ns
t_{WASU}	2.4		3.0		3.8		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		7.1		8.7		11.3	ns
t_{DD}		7.1		8.7		11.3	ns
t_{EABOUT}		3.1		3.9		5.0	ns

FLEX 10K Device EAB Internal Timing Macroparameters *Note (2)*							
Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		14.2		17.6		22.8	ns
$t_{EABRCCOMB}$		14.2		17.6		22.8	ns
$t_{EABRCREG}$		9.5		11.6		15.1	ns
t_{EABWP}	4.7		5.8		7.5		ns
$t_{EABWCCOMB}$		7.1		8.8		11.3	ns
$t_{EABWCREG}$		9.5		11.6		15.1	ns
t_{EABDD}		14.2		17.6		22.8	ns
$t_{EABDATACO}$		4.6		5.7		7.3	ns
$t_{EABDATASU}$	5.6		6.9		9.0		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	5.6		6.9		9.0		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	5.9		7.3		9.5		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	2.4		3.0		3.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		14.2		17.6		22.8	ns

EPF10K10 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		5.2		5.7	ns
t_{DIN2LE}		3.1		3.2	ns
$t_{DCLK2IOE}$		2.0		2.2	ns
$t_{DCLK2LE}$		3.1		3.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		2.6		2.9	ns
$t_{SAMECOLUMN}$		3.5		3.9	ns
$t_{DIFFROW}$		6.1		6.7	ns
$t_{TWOROWS}$		8.7		9.6	ns
$t_{LEPERIPH}$		5.6		6.2	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

EPF10K20 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		5.2		5.7	ns
t_{DIN2LE}		3.1		3.2	ns
$t_{DCLK2IOE}$		2.0		2.2	ns
$t_{DCLK2LE}$		3.1		3.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		2.6		2.9	ns
$t_{SAMECOLUMN}$		4.0		4.4	ns
$t_{DIFFROW}$		6.6		7.3	ns
$t_{TWOROWS}$		9.2		10.1	ns
$t_{LEPERIPH}$		5.6		6.2	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

EPF10K30 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		6.0		6.6	ns
t_{DIN2LE}		3.1		3.2	ns
$t_{DCLK2IOE}$		2.5		2.7	ns
$t_{DCLK2LE}$		3.1		3.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		3.7		4.1	ns
$t_{SAMECOLUMN}$		5.5		6.1	ns
$t_{DIFFROW}$		9.2		10.1	ns
$t_{TWOROWS}$		12.9		14.2	ns
$t_{LEPERIPH}$		6.7		7.4	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

EPF10K40 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		6.0		6.6	ns
t_{DIN2LE}		3.1		3.2	ns
$t_{DCLK2IOE}$		2.5		2.7	ns
$t_{DCLK2LE}$		3.1		3.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		3.7		4.1	ns
$t_{SAMECOLUMN}$		6.0		6.6	ns
$t_{DIFFROW}$		9.7		10.7	ns
$t_{TWOROWS}$		13.4		14.7	ns
$t_{LEPERIPH}$		6.7		7.4	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

EPF10K50 Routing Timing Microparameters *Note (1)*						
Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade	**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		6.0		6.7		10.6	ns
t_{DIN2LE}		3.1		3.2		3.3	ns
$t_{DCLK2IOE}$		2.5		2.7		4.5	ns
$t_{DCLK2LE}$		3.1		3.2		3.3	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		3.7		4.1		5.4	ns
$t_{SAMECOLUMN}$		6.5		7.2		8.1	ns
$t_{DIFFROW}$		10.2		11.2		13.5	ns
$t_{TWOROWS}$		13.9		15.3		18.9	ns
$t_{LEPERIPH}$		6.7		7.4		8.0	ns
$t_{LABCARRY}$		2.0		2.0		2.3	ns
$t_{LABCASC}$		2.6		2.6		2.9	ns

EPF10K70 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		9.0		9.9	ns
t_{DIN2LE}		6.1		6.2	ns
$t_{DCLK2IOE}$		4.0		4.9	ns
$t_{DCLK2LE}$		6.1		6.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		5.0		5.5	ns
$t_{SAMECOLUMN}$		8.5		9.4	ns
$t_{DIFFROW}$		13.5		14.9	ns
$t_{TWOROWS}$		18.5		20.4	ns
$t_{LEPERIPH}$		8.0		8.8	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

EPF10K100 Routing Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		9.4		10.3	ns
t_{DIN2LE}		6.1		6.2	ns
$t_{DCLK2IOE}$		4.0		4.9	ns
$t_{DCLK2LE}$		6.1		6.2	ns
$t_{SAMELAB}$		0.4		0.4	ns
$t_{SAMEROW}$		5.0		5.5	ns
$t_{SAMECOLUMN}$		9.0		9.9	ns
$t_{DIFFROW}$		14.0		15.4	ns
$t_{TWOROWS}$		19.0		20.9	ns
$t_{LEPERIPH}$		8.0		8.8	ns
$t_{LABCARRY}$		2.0		2.0	ns
$t_{LABCASC}$		2.6		2.6	ns

External Timing Parameters

EPF10K10 & EPF10K20 Device External Timing Parameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{DRR}		16.1		20.0	ns
t_{INSU}, *Notes (2), (3)*	5.5		6.0		ns
t_{INH}, *Note (3)*	0.0		0.0		ns
t_{OUTCO}, *Note (3)*		8.5		8.9	ns
t_{ODH}, *Note (3)*	1.0		1.0		ns

EPF10K30 & EPF10K40 Device External Timing Parameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{DRR}		17.2		21.1	ns
t_{INSU}, *Notes (2), (3)*	6.5		7.0		ns
t_{INH}, *Note (3)*	0.0		0.0		ns
t_{OUTCO}, *Note (3)*		8.5		8.9	ns
t_{ODH}, *Note (3)*	1.0		1.0		ns

EPF10K50 Device External Timing Parameters *Note (1)*							
Symbol	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		17.2		21.1		27.0	ns
t_{INSU}, *Notes (2), (3)*	6.5		7.0		7.7		ns
t_{INH}, *Note (3)*	0.0		0.0		0.0		ns
t_{OUTCO}, *Note (3)*		8.5		8.9		9.6	ns
t_{ODH}, *Note (3)*	1.0		1.0		1.0		ns

EPF10K70 & EPF10K100 Device External Timing Parameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{DRR}		19.1		24.2	ns
t_{INSU}, *Notes (2), (3)*	7.0		7.7		ns
t_{INH}, *Note (3)*	0.0		0.0		ns
t_{OUTCO}, *Note (3)*		11.5		12.7	ns
t_{ODH}, *Note (3)*	1.0		1.0		ns

Notes to tables:
(1) All timing parameters are described in Tables 7 through 13 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is guaranteed by characterization.

Power Consumption

The supply power for FLEX 10K devices, P, can be calculated with the following equation:

$$P = P_{INT} + P_{IO}$$

$$= (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the "FLEX 10K Device DC Operating Conditions" table on page 61 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in this data book.

Relative to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CC_{ACTIVE}} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are as follows:

$\mathbf{f_{MAX}}$	=	Maximum operating frequency in MHz
N	=	Total number of logic cells used in the device
$\mathbf{tog_{LC}}$	=	Average percent of logic cells toggling at each clock (typically 12.5%)
K	=	Constant, shown in Table 14

Table 14. Values for Constant K

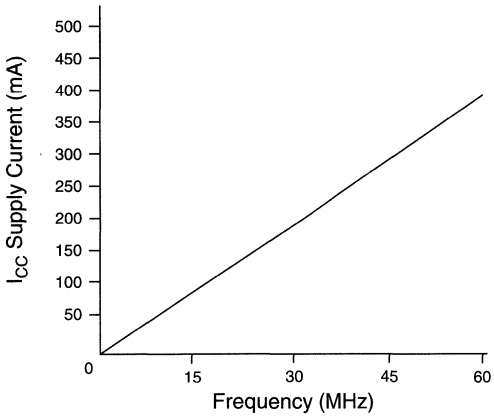
Device	K
EPF10K10	90
EPF10K20	98
EPF10K30	97
EPF10K40	101
EPF10K50	104
EPF10K70	93
EPF10K100	97

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

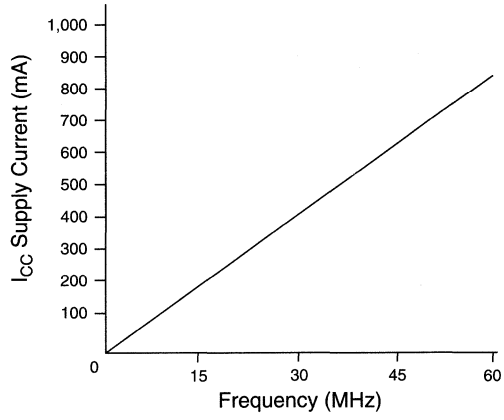
Figure 24 shows the relationship between the current and operating frequency of FLEX 10K devices.

Figure 24. $I_{CCACTIVE}$ vs. Operating Frequency (Part 1 of 2)

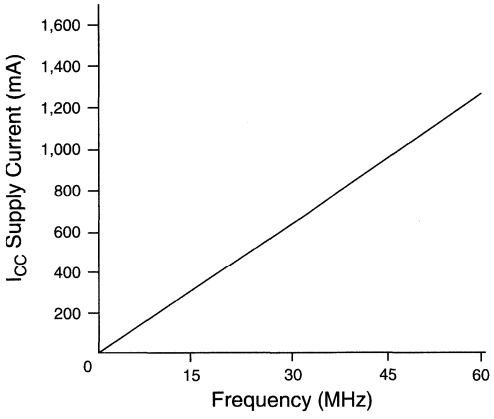
EPF10K10



EPF10K20



EPF10K30



EPF10K40

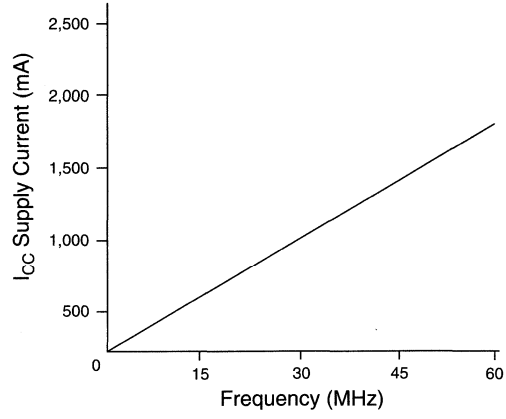
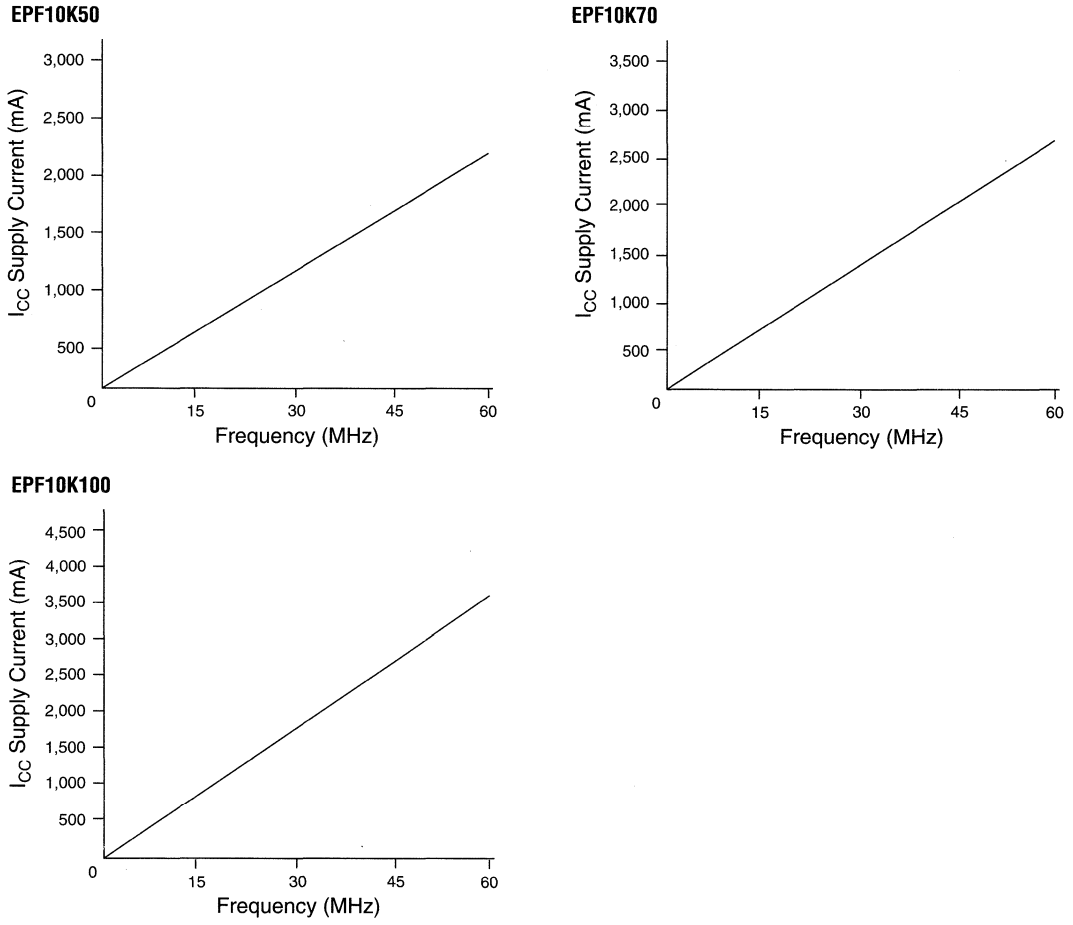


Figure 24. $I_{CCACTIVE}$ vs. Operating Frequency (Part 2 of 2)



Configuration & Operation

The FLEX 10K architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

Go to *Application Note 59 (Configuring FLEX 10K Devices)* for detailed descriptions of device configuration options; device configuration pins; and information on configuring FLEX 10K devices, including sample schematics, timing diagrams, and configuration parameters.

Operating Modes

The FLEX 10K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 10K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 200 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 10K device can be loaded with one of five configuration schemes (see Table 15), chosen on the basis of the target application. An EPC1 Configuration EPROM, intelligent controller, or JTAG port can be used to control the configuration of a FLEX 10K device, allowing automatic configuration on system power-up.

Multiple FLEX 10K devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 15. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration EPROM	EPC1 Configuration EPROM
Passive serial (PS)	BitBlaster, serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	JTAG controller, BitBlaster

Device Pin-Outs

Tables 16 through 18 show the pin names and numbers for the dedicated pins in each FLEX 10K device package.

Table 16. FLEX 10K Device Pin-Outs (Part 1 of 2) *Note (1)*

Pin Name	84-Pin PLCC EPF10K10	208-Pin PQFP EPF10K10	208-Pin RQFP EPF10K20 EPF10K30 EPF10K40	240-Pin RQFP EPF10K20 EPF10K30 EPF10K40 EPF10K50 EPF10K70
MSEL0 *(2)*	20	108	108	124
MSEL1 *(2)*	21	107	107	123
nSTATUS *(2)*	44	52	52	60
nCONFIG *(2)*	23	105	105	121
DCLK *(2)*	2	155	155	179
CONF_DONE *(2)*	65	2	2	2
INIT_DONE *(4)*	58	19	19	26
nCE *(2)*	3	154	154	178
nCEO *(2)*	64	3	3	3
nWS *(3)*	69	206	206	238
nRS *(3)*	70	204	204	236
nCS *(3)*	67	208	208	240
CS *(3)*	68	207	207	239
RDYnBSY *(3)*	59	16	16	23
CLKUSR *(3)*	62	10	10	11
DATA7 *(3)*	78	166	166	190
DATA6 *(3)*	79	164	164	188
DATA5 *(3)*	80	162	162	186
DATA4 *(3)*	81	161	161	185
DATA3 *(3)*	82	159	159	183
DATA2 *(3)*	83	158	158	182
DATA1 *(3)*	84	157	157	181
DATA0 *(2)*	1	156	156	180
TDI *(2)*	4	153	153	177
TDO *(2)*	63	4	4	4
TCK *(2)*	66	1	1	1
TMS *(2)*	46	50	50	58
nTRST *(2)*	45	51	51	59

Table 16. FLEX 10K Device Pin-Outs (Part 2 of 2) *Note (1)*

Pin Name	84-Pin PLCC EPF10K10	208-Pin PQFP EPF10K10	208-Pin RQFP EPF10K20 EPF10K30 EPF10K40	240-Pin RQFP EPF10K20 EPF10K30 EPF10K40 EPF10K50 EPF10K70
Dedicated Inputs	31, 33, 73, 75	78, 80, 182, 184	78, 80, 182, 184	90, 92, 210, 212
Dedicated Clock Pins	32,74	79, 183	79, 183	91, 211
DEV_CLRn *(4)*	76	180	180	209
DEV_OE *(4)*	72	186	186	213
VCCINT (5.0 V)	9, 22, 29, 34, 52, 77	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	5, 16, 27, 37, 47, 57, 77, 89, 96, 112, 122, 130, 140, 150, 160, 170, 189, 205, 224
VCCIO (5.0 V or 3.3 V)	–	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	–
GNDINT	15, 30, 35, 57, 71	21, 33, 49, 81, 82, 123, 129, 151, 185	21, 33, 49, 81, 82, 123, 129, 151, 185	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232
GNDIO	–	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	–
No Connect (N.C.) *Note (5)*	–	7, 8, 9, 14, 15, 36, 37, 113, 114, 125, 126, 139, 140	–	–
Total User I/O Pins	59	134	147	189

Table 17. EPF10K30 & EPF10K50 Pin-Outs (Part 1 of 2) *Note (1)*

Pin Name	356-Pin BGA EPF10K30	356-Pin BGA EPF10K50
MSEL0 *(2)*	D4	D4
MSEL1 *(2)*	D3	D3
nSTATUS *(2)*	D24	D24
nCONFIG *(2)*	D2	D2
DCLK *(2)*	AC5	AC5
CONF_DONE *(2)*	AC24	AC24
INIT_DONE *(4)*	T24	T24
nCE *(2)*	AC2	AC2
nCEO *(2)*	AC22	AC22
nWS *(3)*	AE24	AE24
nRS *(3)*	AE23	AE23
nCS *(3)*	AD24	AD24
CS *(3)*	AD23	AD23
RDYnBSY *(3)*	U22	U22
CLKUSR *(3)*	AA24	AA24
DATA7 *(3)*	AF4	AF4
DATA6 *(3)*	AD8	AD8
DATA5 *(3)*	AE5	AE5
DATA4 *(3)*	AD6	AD6
DATA3 *(3)*	AF2	AF2
DATA2 *(3)*	AD5	AD5
DATA1 *(3)*	AD4	AD4
DATA0 *(2)*	AD3	AD3
TDI *(2)*	AC3	AC3
TDO *(2)*	AC23	AC23
TCK *(2)*	AD25	AD25
TMS *(2)*	D22	D22
nTRST *(2)*	D23	D23
Dedicated Inputs	A13, B14, AF14, AE13,	A13, B14, AF14, AE13
Dedicated Clock Pins	A14, AF13	A14, AF13
DEV_CLRn *(4)*	AD13	AD13
DEV_OE *(4)*	AE14	AE14
VCCINT (5.0 V)	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26

Table 17. EPF10K30 & EPF10K50 Pin-Outs (Part 2 of 2) *Note (1)*

Pin Name	356-Pin BGA EPF10K30	356-Pin BGA EPF10K50
VCCIO (5.0 V or 3.3 V)	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16
GNDINT	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25
GNDIO	–	–
No Connect (N.C.) *Note (6)*	C1, D1, D26, E1, E2, G1, G5, G23, G26, H1, H25, H26, J25, K25, P24, R24, T23, U25, V1, V3, V4, V26, W2, W3, Y1, Y2, Y23, AC26	–
Total User I/O Pins	246	274

Table 18. EPF10K50, EPF10K70 & EPF10K100 Pin-Outs (Part 1 of 2)

Pin Name	403-Pin PGA EPF10K50	503-Pin PGA EPF10K70	503-Pin PGA EPF10K100
MSEL0 *(2)*	AN1	AT40	AT40
MSEL1 *(2)*	AR1	AV40	AV40
nSTATUS *(2)*	AU37	AY4	AY4
nCONFIG *(2)*	AU1	AY40	AY40
DCLK *(2)*	E1	H40	H40
CONF_DONE *(2)*	C37	F4	F4
INIT_DONE *(4)*	R35	V6	V6
nCE *(2)*	G1	K40	K40
nCEO *(2)*	E37	H4	H4
nWS *(3)*	E31	A3	A3
nRS *(3)*	A33	C5	C5
nCS *(3)*	A35	C1	C1
CS *(3)*	C33	C3	C3
RDYnBSY *(3)*	N35	T6	T6
CLKUSR *(3)*	G35	H6	H6
DATA7 *(3)*	C9	E29	E29
DATA6 *(3)*	A7	D30	D30
DATA5 *(3)*	E9	C31	C31
DATA4 *(3)*	C7	B32	B32
DATA3 *(3)*	A5	D32	D32
DATA2 *(3)*	E7	B34	B34
DATA1 *(3)*	C5	E33	E33
DATA0 *(2)*	C1	F40	F40
TDI *(2)*	J1	M40	M40
TDO *(2)*	G37	K4	K4
TCK *(2)*	A37	D4	D4
TMS *(2)*	AN37	AT4	AT4
nTRST *(2)*	AR37	AV4	AV4
Dedicated Inputs	A17, A21, AU17, AU21	D20, D24, AY24, AY20	D20, D24, AY24, AY20
Dedicated Clock Pins	A19, AU19	D22, AY22	D22, AY22
DEV_CLRn *(4)*	C17	F22	F22
DEV_OE *(4)*	C19	G21	G21

Table 18. EPF10K50, EPF10K70 & EPF10K100 Pin-Outs (Part 2 of 2)

Pin Name	403-Pin PGA EPF10K50	503-Pin PGA EPF10K70	503-Pin PGA EPF10K100
VCCINT (5.0 V)	B2, D14, E25, F22, K36, T2, T32, V6, AD34, AE5, AL5, AM6, AM20, AN25, AN29, AP4, AT16, AT36	C11, E39, G27, N5, N41, W39, AC3, AG7, AR3, AR41, AU37, AW5, AW25, AW41, BA17, BA19	C11, E39, G27, N5, N41, W39, AC3, AG7, AR3, AR41, AU37, AW5, AW25, AW41, BA17, BA19
VCCIO (5.0 V or 3.3 V)	B22, D34, E11, E27, F16, L5, L33, P4, T6, T36, V32, AB36, AG5, AG33, AH2, AM18, AM32, AN11, AN27, AP24, AT22	C9, C15, C25, C33, C37, E19, E41, G7, L3, R41, U3, U37, W5, AC41, AE5, AJ41, AL39, AU3, AU17, AW3, AW19, BA9, BA27, BA29, BA37	C9, C15, C25, C33, C37, E19, E41, G7, L3, R41, U3, U37, W5, AC41, AE5, AJ41, AL39, AU3, AU17, AW3, AW19, BA9, BA27, BA29, BA37
GNDINT	B16, B36, D4, E21, F18, F32, G33, P34, U5, Y32, AA33, AB2, AB6, AH36, AM16, AN17, AN21, AP14, AT2	C17, E3, E5, E25, G37, J3, J41, U7, AA3, AE39, AL5, AL41, AU27, AW39, BA7, BA13, BA25	C17, E3, E5, E25, G37, J3, J41, U7, AA3, AE39, AL5, AL41, AU27, AW39, BA7, BA13, BA25
GNDIO	B10, B28, D24, E5, E19, E33, F6, F20, K2, W5, W33, Y6, AB32, AD4, AM22, AN5, AN19, AN33, AP34, AT10, AT28	C21, C23, C39, C41, E13, E31, G3, G17, N3, N39, R3, W41, W3, AA41, AG37, AJ3, AN3, AN41, AU7, AU41, AW13, AW31, BA11, BA21, BA23	C21, C23, C39, C41, E13, E31, G3, G17, N3, N39, R3, W3, W41, AA41, AG37, AJ3, AN3, AN41, AU7, AU41, AW13, AW31, BA11, BA23, BA21,
No Connect (N.C.) *Note (7)*	–	A19, A21, A23, A31, A33, A35, A39, A41, B16, B18, B22, B24, B30, B40, C29, C35, D18, D26, D28, D38, E27, E37, F18, F2, F26, F30, F32, G23, G25, G29, G31, G33, G35, K6, K42, L39, L43, M2, N7, P38, P4, P42, R37, T40, V42, AC5, AD2, AE3	–
Total User I/O Pins	310	358	406

Notes to tables:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin after configuration.
(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(5) To maintain pin compatibility when migrating from the EPF10K30 to the EPF10K10 in the 208-pin RQFP package, do not use these pins as user I/O pins.
(6) To maintain pin compatibility when migrating from the EPF10K50 to the EPF10K30 in the 356-pin BGA package, do not use these pins as user I/O pins.
(7) To maintain pin compatibility when migrating from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.

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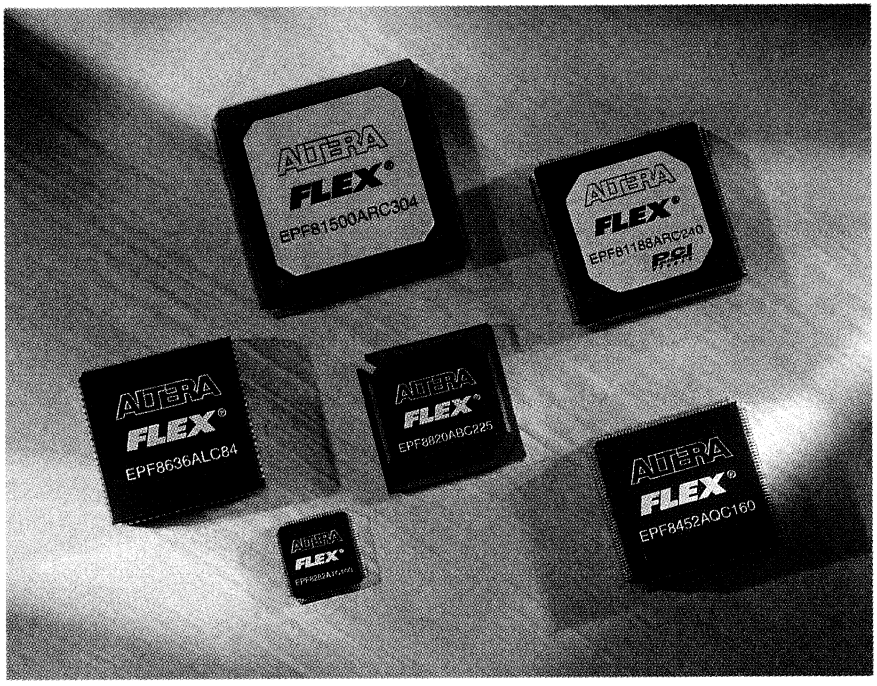
FLEX 8000 Programmable Logic Device Family Data Sheet


ALTERA
FLEX®
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FLEX®
EPF8820ABC225
ALTERA
FLEX®
EPF8452AQC160
ALTERA
FLEX®

FLEX 8000

Programmable Logic Device Family

June 1996, ver. 8 | Data Sheet

Features...

- Low-cost, high-density, register-rich CMOS programmable logic device family (see Table 1)
  - 2,500 to 16,000 usable gates
  - 282 to 1,500 registers
- System-level features
  - In-circuit reconfigurability (ICR) via external Configuration EPROM or intelligent controller
  - Fully compliant with the peripheral component interconnect (PCI) standard
  - Built-in JTAG boundary-scan test (BST) circuitry compliant with IEEE Std 1149.1-1990 on selected devices
  - 3.3- or 5.0-V I/O pins for EPF8636A and larger devices
  - Able to bridge between 3.3-V and 5.0-V systems
  - Low power consumption (less than 1 mA in standby mode)
- Flexible interconnect
  - FastTrack Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions
  - Tri-state emulation that implements internal tri-state nets
- Powerful I/O pins
  - Programmable output slew-rate control reduces switching noise
  - Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process

Table 1. FLEX 8000 Device Features

Feature	EPF8282A EPF8282AV	EPF8452A	EPF8636A	EPF8820A	EPF81188A	EPF81500A
Usable gates	2,500	4,000	6,000	8,000	12,000	16,000
Flipflops	282	452	636	820	1,188	1,500
Logic array blocks (LABs)	26	42	63	84	126	162
Logic elements	208	336	504	672	1,008	1,296
Maximum user I/O pins	78	120	136	152	184	208
JTAG BST circuitry	Yes	No	Yes	Yes	No	Yes

A-DS-F8000-08

...and More Features

- Available in a variety of packages with 84 to 304 pins (see Table 2)
- Software design support and automatic place-and-route provided by the Altera MAX+PLUS II development system for 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar, Mentor Graphics, MINC, OrCAD, Synopsys, Veribest, and Viewlogic

Table 2. FLEX 8000 Package Options & I/O Pin Count

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	208-Pin RQFP	225-Pin BGA	232-Pin PGA	240-Pin RQFP	280-Pin PGA	304-Pin RQFP
EPF8282A	68	78											
EPF8282AV	68	78											
EPF8452A	68	68		120	120								
EPF8636A	68			118		136	136	136					
EPF8820A			112	120		152	152	152	152				
EPF81188A							148			184	184		
EPF81500A											181	208	208

General Description

Altera's Flexible Logic Element MatriX (FLEX) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented with compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing (DSP), wide data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. Table 3 shows FLEX 8000 performance for typical applications, as well as the logic elements required.

Table 3. FLEX 8000A Performance

Application	LEs Used	A-2 Speed Grade	A-3 Speed Grade	A-4 Speed Grade	Unit
16-bit loadable counter	16	125	95	83	MHz
16-bit up/down counter	16	125	95	83	MHz
16-bit prescaled counter	24	270	232	185	MHz
24-bit accumulator	24	87	67	58	MHz
16-bit address decode	4	4.2	4.9	6.3	ns
16-to-1 multiplexer	10	6.6	7.9	9.5	ns

All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM elements. FLEX 8000 devices are configured at system power-up with data stored in an industry-standard parallel EPROM or an Altera serial Configuration EPROM device, or with data provided by a system controller. Altera offers the EPC1, EPC1213, and EPC1064 Configuration EPROMs, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32K × 8-bit or larger EPROM, or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 100 ms, real-time changes can be made during system operation.

FLEX 8000 devices contain an optimized microprocessor interface that permits the microprocessor to configure FLEX 8000 devices serially, in parallel, synchronously, or asynchronously. The interface also enables the microprocessor to treat a FLEX 8000 device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to create configuration software.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, library of parameterized module (LPM), VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

For more information on MAX+PLUS II, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

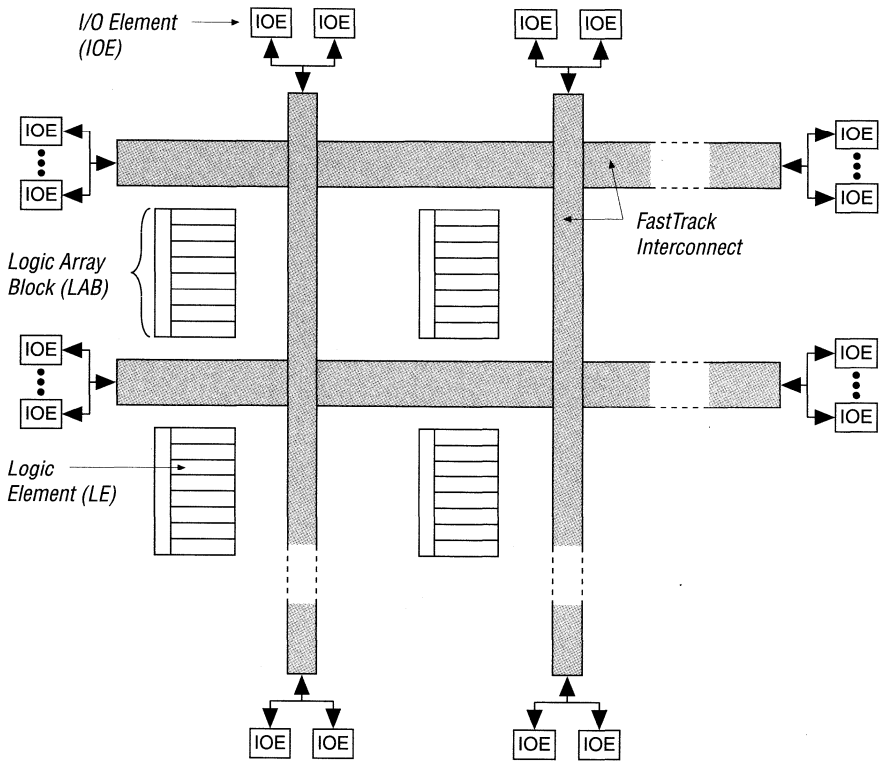
Functional Description

The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

Eight LEs are grouped together to form a logic array block (LAB). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

Figure 1. FLEX 8000 Device Block Diagram

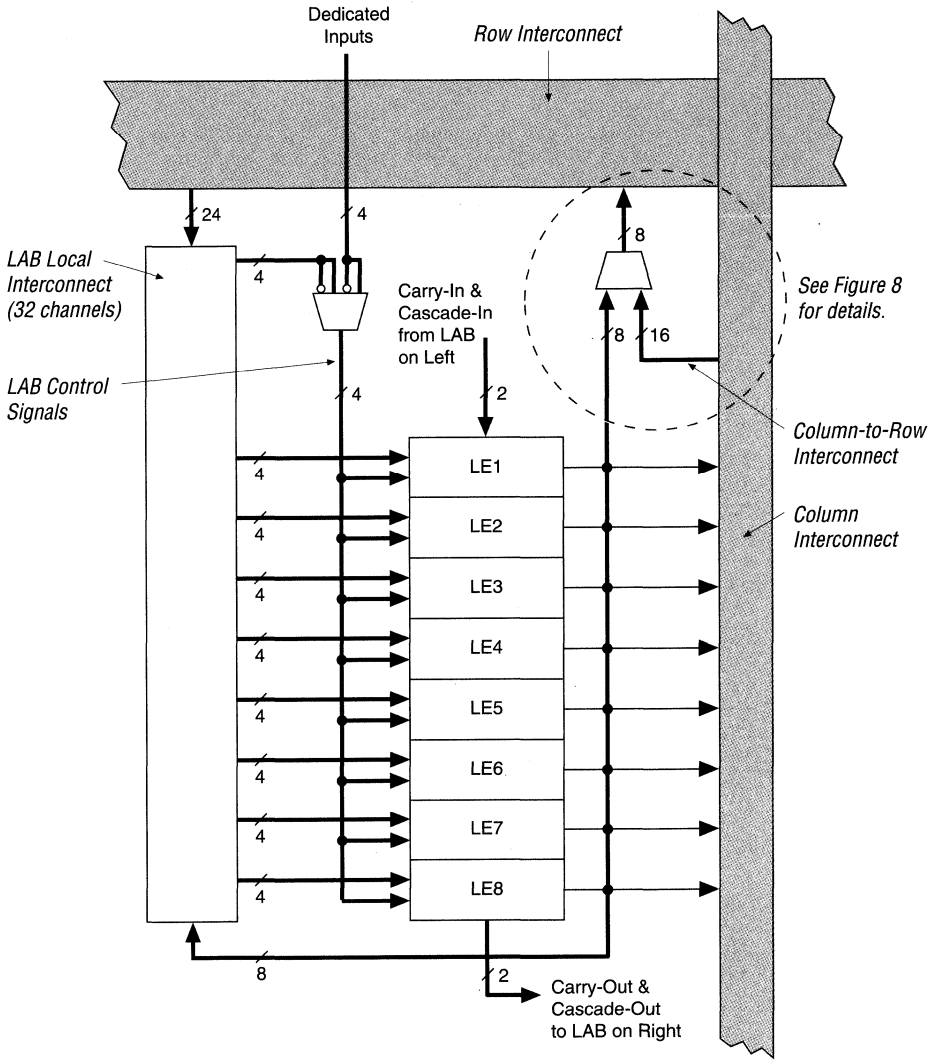


Signal interconnections within FLEX 8000 devices and between device pins are provided by the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

Logic Array Block

A logic array block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance Figure 2 shows a block diagram of the FLEX 8000 LAB.

Figure 2. FLEX 8000 Logic Array Block

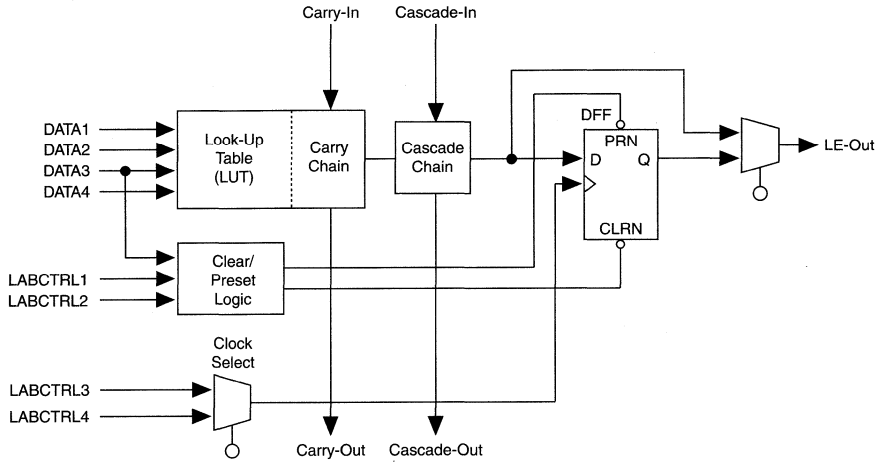


Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as clocks, and the other two for clear/preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global clock, clear, or preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global clock, clear, or preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. This process is called programmable inversion, and is available for all four LAB control signals.

Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, a programmable flipflop, a carry chain, and cascade chain. Figure 3 shows a block diagram of an LE.

Figure 3. FLEX 8000 Logic Element (LE)



The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

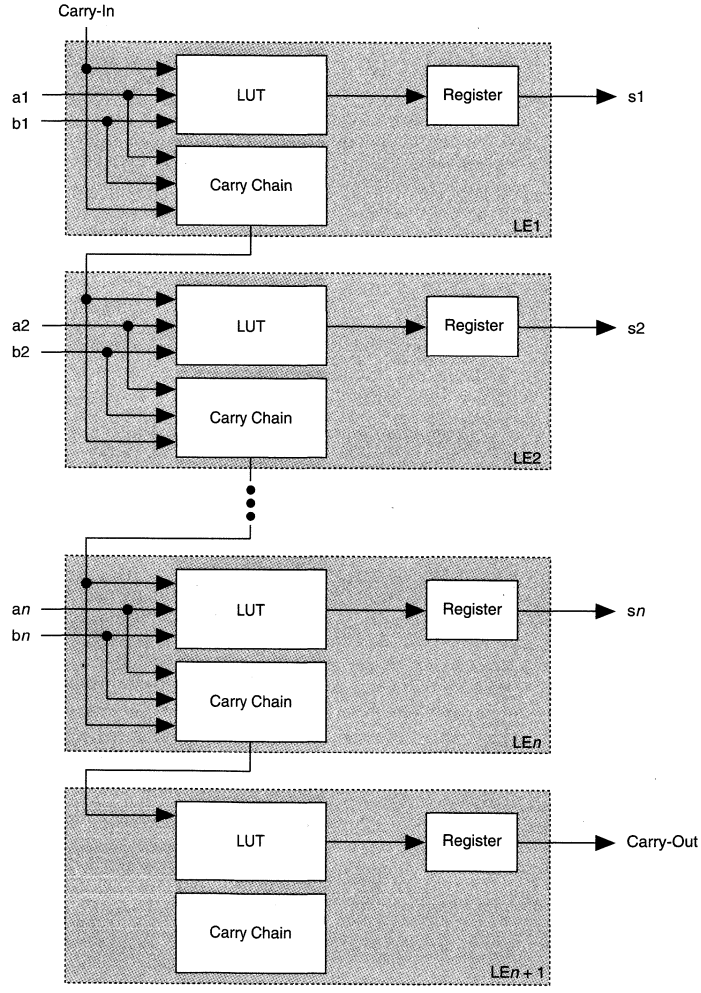
The FLEX 8000 architecture provides two dedicated high-speed data paths—carry chains and cascade chains—that connect adjacent LEs without using local interconnect paths. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Heavy use of carry and cascade chains can reduce the routing resources available for implementing other logic. Therefore, the use of carry and cascade chains should be limited to speed-critical portions of a design.

Carry Chain

The carry chain provides a very fast (less than 1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 8000 architecture to implement high-speed counters and adders of arbitrary width. The MAX+PLUS II Compiler can create carry chains automatically during design processing; designers can also insert carry chain logic manually during design entry.

Figure 4 shows how an *n*-bit full adder can be implemented in *n*+1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to another LE, where it can be used as a general-purpose signal. In addition to mathematical functions, carry chain logic supports very fast counters and comparators.

Figure 4. Carry Chain Operation

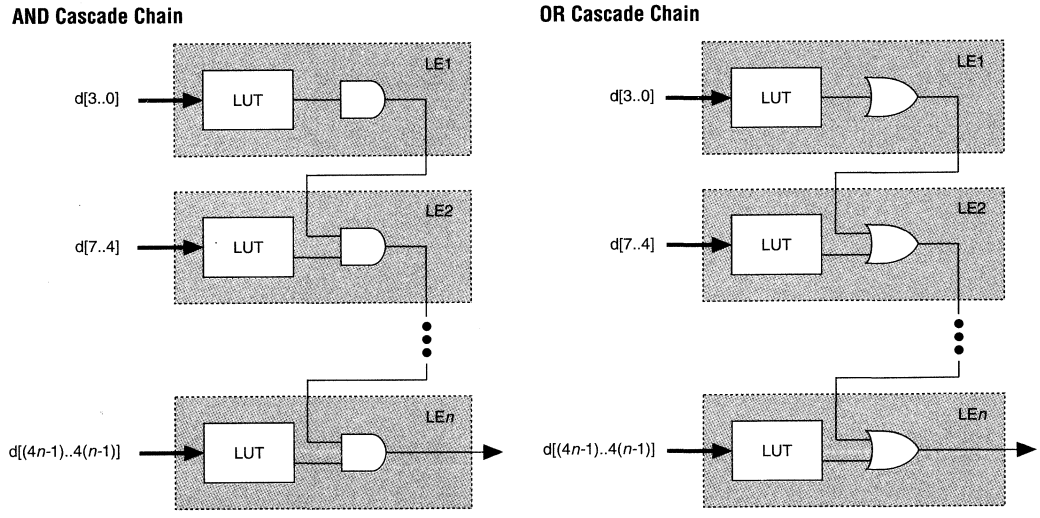


Cascade Chain

With the cascade chain, the FLEX 8000 architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.6 ns per LE. The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry. Cascade chains longer than 8 LEs are automatically implemented by linking LABs together. The last LE of an LAB cascades to the first LE in the next LAB in the row.

Figure 5 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with n LEs. For a device with an A-2 speed grade, the LUT delay is approximately 1.6 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

Figure 5. Cascade Chain Operation

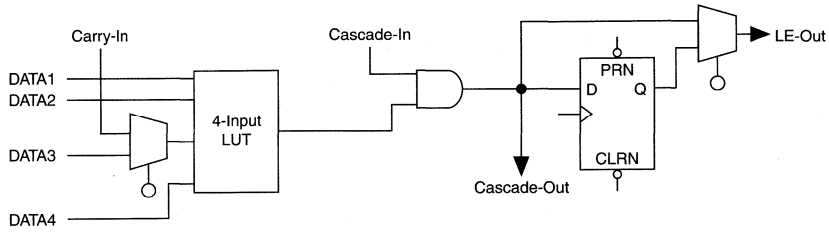


LE Operating Modes

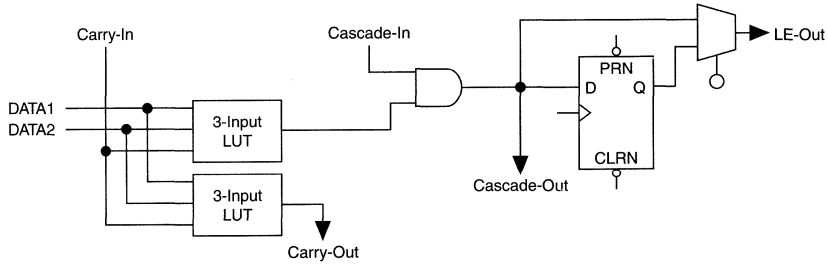
The FLEX 8000 logic element can operate in one of four modes, each of which uses LE resources differently. See Figure 6. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

Figure 6. FLEX 8000 Logic Element Operating Modes

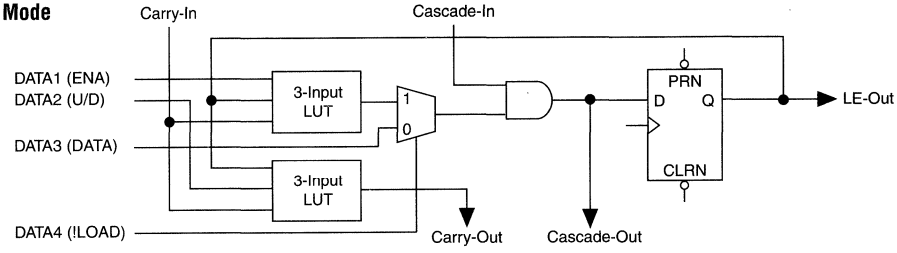
Normal Mode



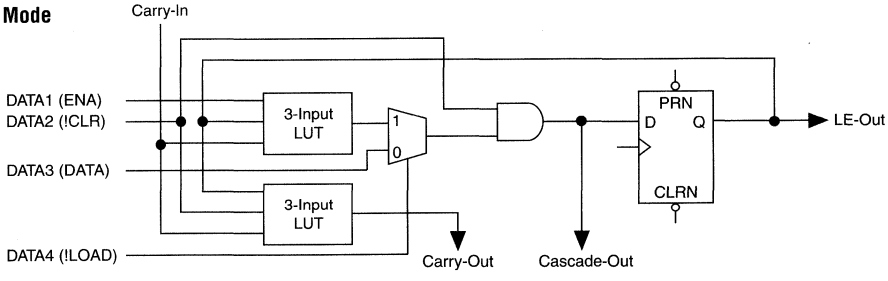
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Normal Mode

The normal mode is suitable for general logic applications and wide decode functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in signal are the inputs to a 4-input LUT. Using a configurable SRAM bit, the MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as an input. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. The LE-Out signal—the data output of the LE—is either the combinatorial output of the LUT and cascade chain, or the data output (Q) of the programmable register.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT provides a 3-bit function; the other generates a carry bit. As shown in Figure 6, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three bits: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports a cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control; the clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer, and the output of this multiplexer is ANDed with a synchronous clear.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. MAX+PLUS II automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

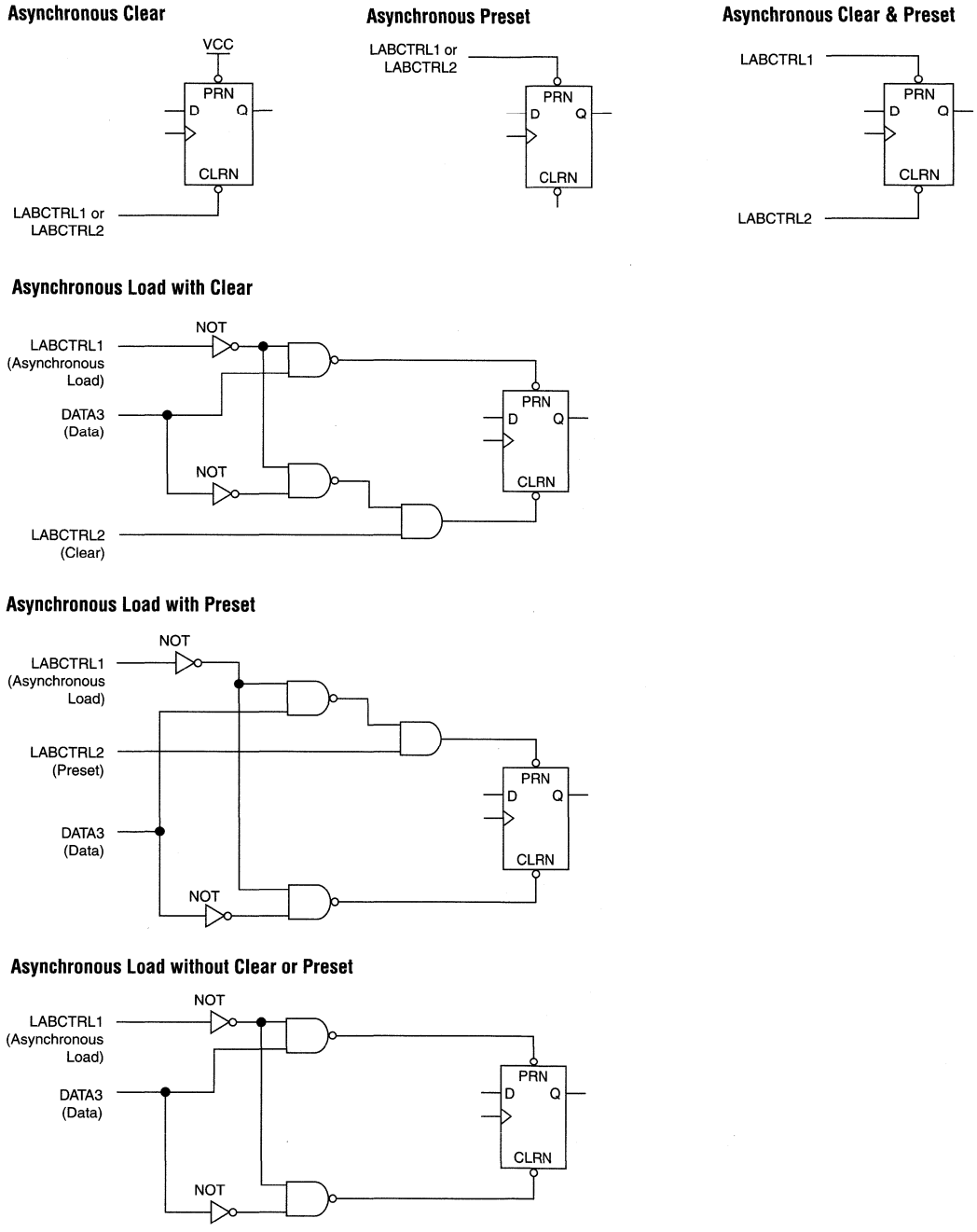
Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL11, and LABCTRL12 inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Since the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, chosen during design entry. See Figure 7.

- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

Figure 7. LE Asynchronous Clear & Preset Modes



Asynchronous Clear

A register is cleared by one of the two LABCTRL signals. When the CLRN port receives a low signal, the register is set to zero.

Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a 1 into the register. Alternatively, MAX+PLUS II can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Clear & Preset

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. The DATA3 input is tied to VCC; therefore, asserting LABCTRL1 asynchronously loads a 1 into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. However, LABCTRL2 implements the clear by controlling the register clear; therefore, LABCTRL2 does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with a preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 clears the register, while asserting LABCTRL1 loads the register. MAX+PLUS II inverts the signal that drives the DATA3 signal to account for the inversion of the register's output.

Asynchronous Load without Clear or Preset

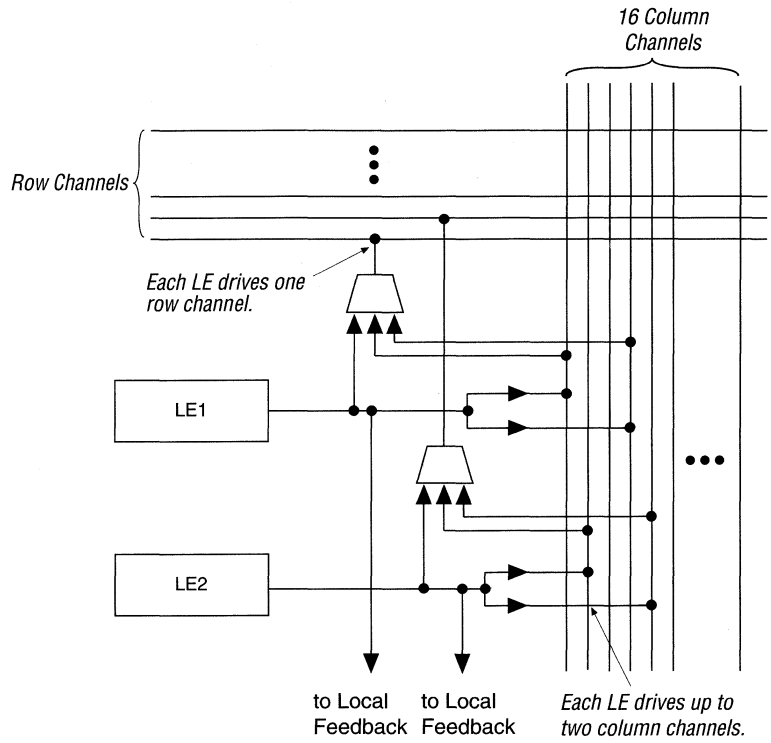
When implementing an asynchronous load without the clear or preset, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

FastTrack Interconnect

In the FLEX 8000 architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal (row) and vertical (column) routing channels that traverse the entire FLEX 8000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing structure in FPGAs requires switch matrices to connect a variable number of routing paths, which increases the delays between logic resources and reduces performance.

The LABs within FLEX 8000 devices are arranged into a matrix of columns and rows. Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Figure 8 shows how an LE drives the row and column interconnect.

Figure 8. LAB Connections to Row & Column Interconnect



Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These 3 signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 4 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

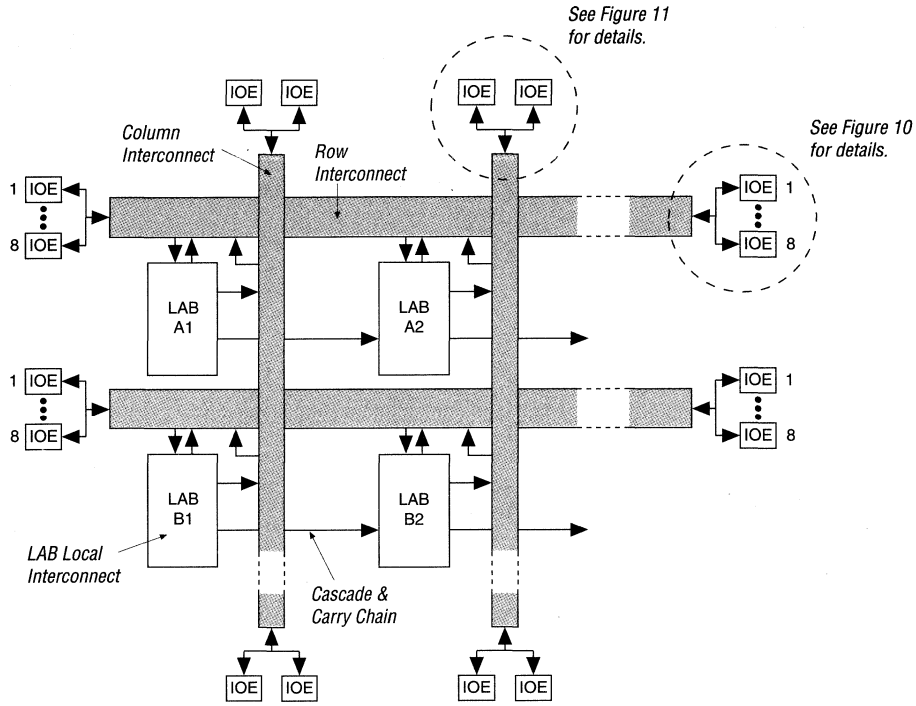
Table 4. FLEX 8000 FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF8282A EPF8282AV	2	168	13	16
EPF8452A	2	168	21	16
EPF8636A	3	168	21	16
EPF8820A	4	168	21	16
EPF81188A	6	168	21	16
EPF81500A	6	216	27	16

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

Figure 9. FLEX 8000 Device Interconnect Resources

Each LAB is named according to its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.

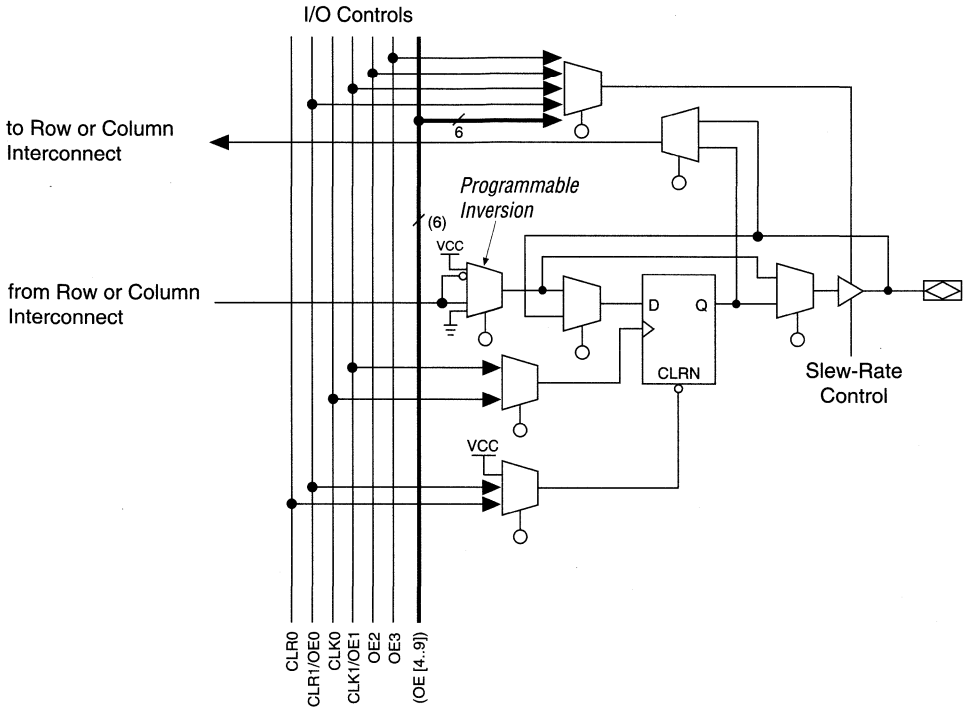


I/O Element

An I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect where appropriate. Figure 10 shows the IOE block diagram.

Figure 10. I/O Element (IOE)

Numbers in parentheses are for EPF81500A devices only.

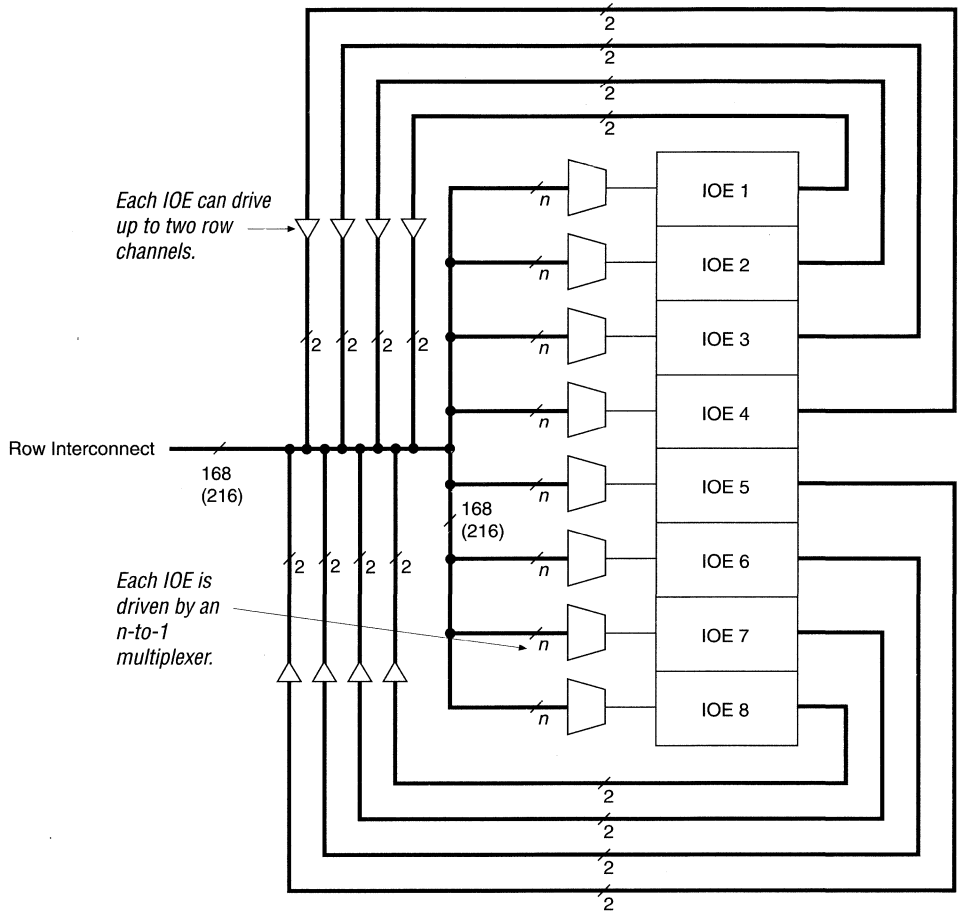


Row-to-IOE Connections

Figure 11 illustrates the connection between row interconnect channels and IOEs. An input signal from an IOE can drive two separate row channels. When an IOE is used as an output, the signal is driven by an *n*-to-1 multiplexer that selects the row channels. The size of the multiplexer varies with the number of columns in a device. EPF81500A devices use a 27-to-1 multiplexer; EPF81188A, EPF8820A, EPF8636A, and EPF8452A devices use a 21-to-1 multiplexer; and EPF8282A and EPF8282AV devices use a 13-to-1 multiplexer. Eight IOEs are connected to each side of the row channels.

Figure 11. FLEX 8000 Row-to-IOE Connection

Numbers in parentheses are for EPF81500A devices. See Note (1).



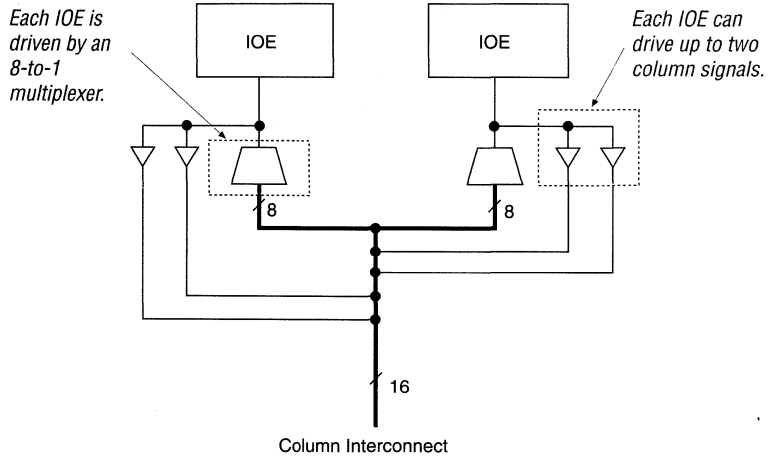
Note:

(1) n = 13 for EPF8282A and EPF8282AV devices.
n = 21 for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
n = 27 for EPF81500A devices.

Column-to-IOE Connections

Two IOEs are located at the top and bottom of the column channels (see Figure 12). When an IOE is used as an input, it can drive up to two separate column channels. The output signal to an IOE can choose up to 8 of the 16 column channels through an 8-to-1 multiplexer.

Figure 12. FLEX 8000 Column-to-IOE Connection



In addition to the general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global clock, clear, and preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

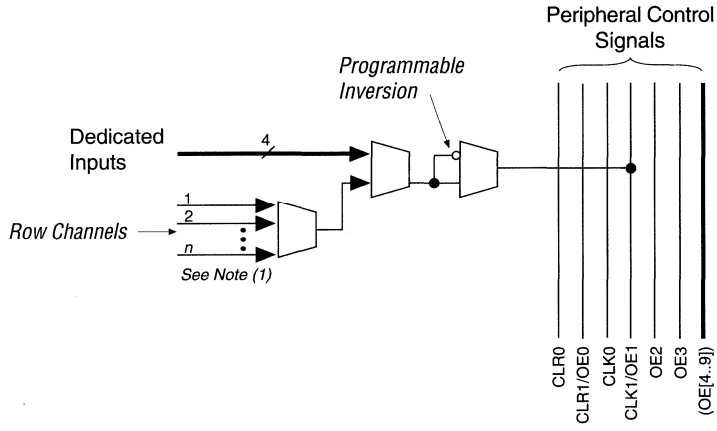
I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect when appropriate.

The clock, clear, and output enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or by internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to four output enable signals (10 in the EPF81500A devices), and up to two clock or clear signals. Figure 12 shows how two output enable signals are shared with one clock and one clear signal.

The signals for the peripheral bus can be generated by any of the four dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels used correlates to the number of columns in the FLEX 8000 device. EPF8282A and EPF8282AV devices use 13 channels; EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices use 21 channels; and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The six peripheral control signals (12 in EPF81500A devices) can be accessed by every IOE.

Figure 13. FLEX 8000 Peripheral Bus

Numbers in parentheses are for EPF81500A devices. See Note (1).



Note:

(1) n = 13 for EPF8282A and EPF8282AV devices.
n = 21 for EPF8452A, EPF8636A, EPF8820A, EPF81188A devices.
n = 27 for EPF81500A devices.

Table 5 lists the source of the peripheral control signal for each FLEX 8000 device by row.

Table 5. Row Sources of Peripheral Control Signals

Peripheral Control Signal	EPF8282A EPF8282AV	EPF8452A	EPF8636A	EPF8820A	EPF81188A	EPF81500A
CLK0	Row A	Row A	Row A	Row A	Row E	Row E
CLK1/OE1	Row B	Row B	Row C	Row C	Row B	Row B
CLR0	Row A	Row A	Row B	Row B	Row F	Row F
CLR1/OE0	Row B	Row B	Row C	Row D	Row C	Row C
OE2	Row A	Row A	Row A	Row A	Row D	Row A
OE3	Row B	Row B	Row B	Row B	Row A	Row A
OE4	–	–	–	–	–	Row B
OE5	–	–	–	–	–	Row C
OE6	–	–	–	–	–	Row D
OE7	–	–	–	–	–	Row D
OE8	–	–	–	–	–	Row E
OE9	–	–	–	–	–	Row F

Output Configuration

This section discusses slew-rate control, 3.3-V or 5.0-V I/O operation, and JTAG operation for FLEX 8000 devices.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise and adds a maximum delay of 4 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

3.3-V or 5.0-V I/O Operation

Many members of the FLEX 8000 family, including the EPF81500A, EPF81188A, EPF8820A, and EPF8636A devices (except the 84-pin PLCC EPF8636A), can be set for 3.3-V or 5.0-V operation. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCINT} pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs. The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominal additional timing delay; therefore the t_{OD2} parameter is used in place of t_{OD1}.

JTAG Operation

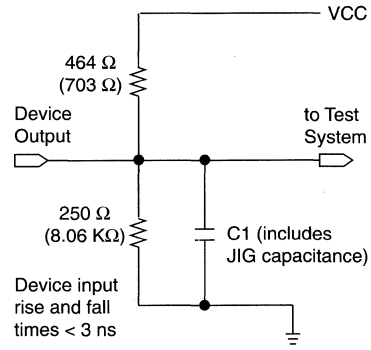
The EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices provide Joint Test Action Group (JTAG) boundary-scan testing (BST) circuitry. For detailed information on JTAG operation in these FLEX 8000 devices, refer to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices).*

Generic Testing

Each FLEX 8000 device is functionally tested and specified by Altera. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in Figure 14. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 14. FLEX 8000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices.



FLEX 8000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		Plastic and power quad flat packages, under bias		135	° C

FLEX 8000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	*Note (4)*	3.00	3.60	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 8000 5.0-V Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V	2.4			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load		0.5	10	mA

FLEX 8000 5.0-V Device Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) The maximum V_{CC} rise time is 100 ms.
(4) Numbers in parentheses are for industrial-temperature-range versions.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) Operating conditions: V_{CCINT} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(7) Capacitance is sample-tested only.

FLEX 8000 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		Plastic packages, under bias		135	° C

FLEX 8000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (3)*	3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 8000 3.3-V Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = 0.1 mA DC, *Note (5)*	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (5)*			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load, *Note (6)*		0.3	10	mA

FLEX 8000 3.3-V Device Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* and *Application Note 74 (Evaluating Power for Altera Devices)* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Capacitance is sample-tested only.
(4) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial use.
V_{CCIO} = 3.3 V ± 10% for industrial use.
(5) The IOH parameter refers to high-level TTL output current; the IOL parameter refers to low-level TTL output current.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(7) The maximum V_{cc} rise time is 100 ms.

Figures 15 and 16 show the typical output drive characteristics of 5.0-V FLEX 8000 devices. The output driver is complaint with the ***PCI Local Bus Specification,*** version 2.1.

Figure 15. Output Drive Characteristics of 5.0-V Devices (except EPF8282A)

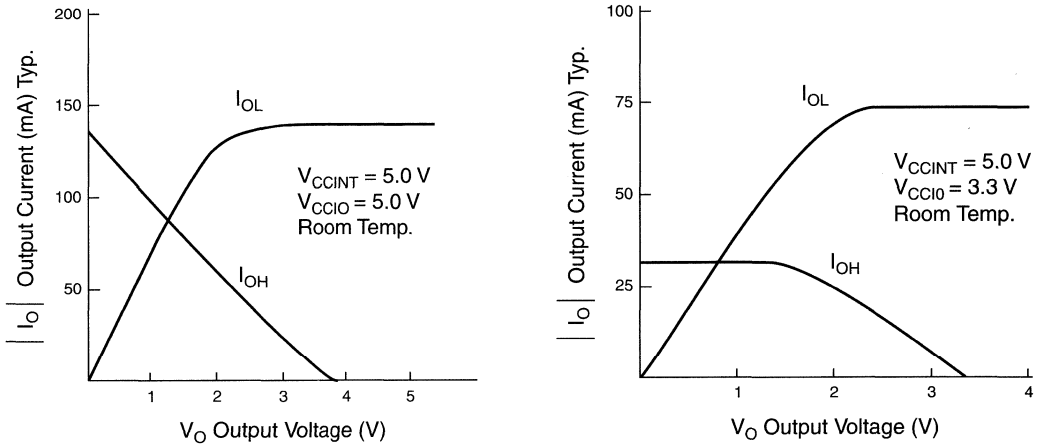


Figure 16. Output Drive Characteristics of EPF8282A Devices with 5.0-V V_{CCIO}

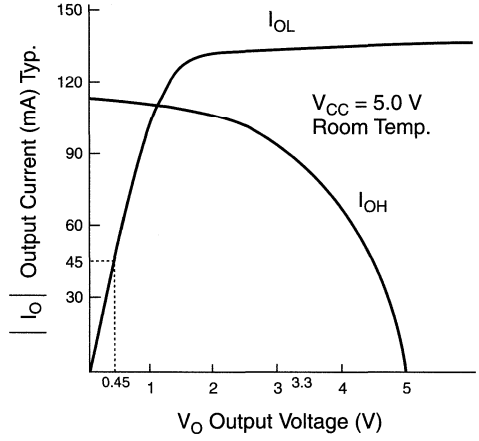
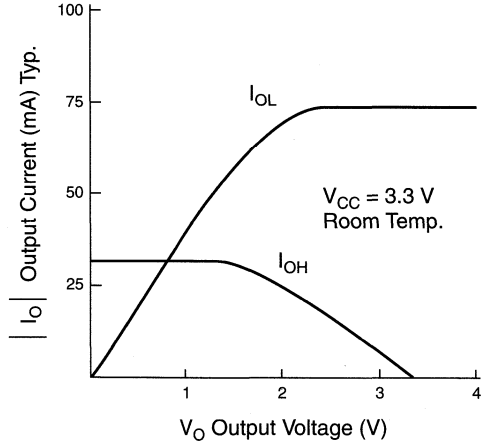


Figure 17 shows the typical output drive characteristics of EPF8282AV devices.

Figure 17. Output Drive Characteristics of EPF8282AV Devices



Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 6 through 9 describe the FLEX 8000 timing parameters and their symbols.

Table 6. FLEX 8000 Internal Timing Parameters *Note (1)*

Symbol	Parameter
t_{IOD}	IOE register data delay
t_{IOC}	IOE register control signal delay
t_{IOE}	Output enable delay
t_{IOCO}	IOE register clock-to-output delay
t_{IOCOMB}	IOE combinatorial delay
t_{IOSU}	IOE register setup time before clock
t_{IOH}	IOE register hold time after clock
t_{IOCLR}	IOE register clear delay
t_{IN}	Input pad and buffer delay
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 5.0 V, C1 = 35 pF, *Note (2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V, C1 = 35 pF, *Note (2)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on, C1 = 35 pF, *Note (3)*
t_{XZ}	Output buffer disable delay, C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 5.0 V, C1 = 35 pF
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V, C1 = 35 pF, *Note (2)*
t_{ZX3}	Output buffer enable delay, slow slew rate = on, C1 = 35 pF, *Note (3)*

Table 7. FLEX 8000 Logic Element Timing Parameters *Note (1)*	
Symbol	**Parameter**
t_{LUT}	LUT delay for data-in
t_{CLUT}	LUT delay for carry-in
t_{RLUT}	LUT delay for LE register feedback
t_{GATE}	Cascade gate delay
t_{CASC}	Cascade chain routing delay
t_{CICO}	Carry-in to carry-out delay
t_{CGEN}	Data-in to carry-out delay
t_{CGENR}	LE register feedback to carry-out delay
t_{C}	LE register control signal delay
t_{CH}	Clock high time
t_{CL}	Clock low time
t_{CO}	LE register clock-to-output delay
t_{COMB}	Combinatorial delay
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{PRE}	LE register preset delay
t_{CLR}	LE register clear delay

Table 8. FLEX 8000 Interconnect Timing Parameters *Note (1)*	
Symbol	**Parameter**
$t_{LABCASC}$	Cascade delay between LEs in different LABs
$t_{LABCARRY}$	Carry delay between LEs in different LABs
t_{LOCAL}	LAB local interconnect delay
t_{ROW}	Row interconnect routing delay, *Note (4)*
t_{COL}	Column interconnect routing delay
t_{DIN_C}	Dedicated input to LE control delay
t_{DIN_D}	Dedicated input to LE data delay, *Note (4)*
t_{DIN_IO}	Dedicated input to IOE control delay

Table 9. FLEX 8000 External Reference Timing Characteristics *Note (5)*	
Symbol	**Parameter**
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects, *Note (6)*
t_{ODH}	Output Data Hold time after clock, *Note (7)*

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) Operating conditions: V_{CCIO} = 5.0 V ± 5% for commercial use.
V_{CCIO} = 5.0 V ± 10% for industrial use.
V_{CCIO} = 3.3 V ± 10% for all temperature grades.

(3) For t_{OD3} and t_{ZX3} parameters, V_{CCIO} = 3.3 V or 5.0 V.

(4) The t_{ROW} and t_{DIN_D} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.

(6) For more information on test conditions, see *Application Note 76 (Understanding FLEX 8000 Timing)* in this data book.

(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for logic element and I/O element registers.

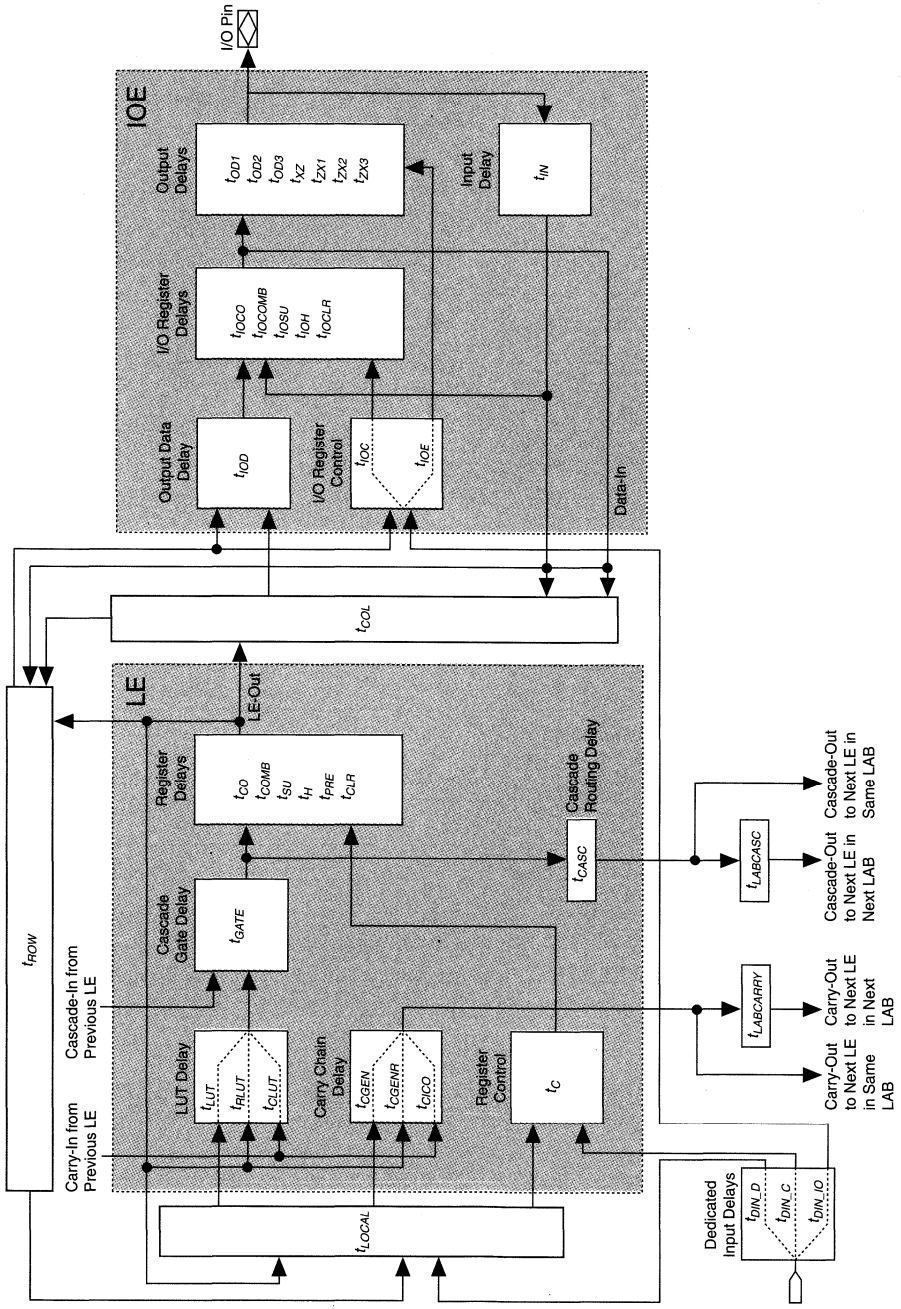
The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 18. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 18 is expressed as a worst-case value in the "Timing Parameters" tables in this data sheet. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance.

Table 10 summarizes the interconnect paths shown in Figure 18.

Table 10. FLEX 8000 Timing Model Interconnect Paths

Source	Destination	Total Delay
LE-out	LE in same LAB	t_{LOCAL}
LE-out	LE in same row, different LAB	$t_{ROW} + t_{LOCAL}$
LE-out	LE in different row	$t_{COL} + t_{ROW} + t_{LOCAL}$
LE-out	IOE on column	t_{COL}
LE-out	IOE on row	t_{ROW}
IOE on row	LE in same row	$t_{ROW} + t_{LOCAL}$
IOE on column	Any LE	$t_{COL} + t_{ROW} + t_{LOCAL}$

Figure 18. FLEX 8000 Timing Model



EPF8282A Internal Timing Parameters

EPF8282A I/O Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

EPF8282A Interconnect Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		4.2		4.2		4.2	ns
t_{COL}		2.5		2.5		2.5	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.2		7.2		7.2	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

EPF8282A Logic Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	1.7		1.7		2.7		ns
t_{CL}	1.7		1.7		2.7		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

EPF8282A External Timing Parameters

Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		15.8		19.8		24.8	ns
t_{ODH}	1		1		1		ns

EPF8282AV Internal Timing Parameters

EPF8282AV I/O Element Timing Parameters			
Symbol	A-4 Speed Grade		
	Min	**Max**	**Unit**
t_{IOD}		2.2	ns
t_{IOC}		2.0	ns
t_{IOE}		2.0	ns
t_{IOCO}		2.0	ns
t_{IOCOMB}		0.0	ns
t_{IOSU}	2.8		ns
t_{IOH}	0.2		ns
t_{IOCLR}		2.3	ns
t_{IN}		3.4	ns
t_{OD1}		4.1	ns
t_{OD2}			ns
t_{OD3}		7.1	ns
t_{XZ}		4.3	ns
t_{ZX1}		4.3	ns
t_{ZX2}			ns
t_{ZX3}		8.3	ns

EPF8282AV Interconnect Timing Parameters			
Symbol	A-4 Speed Grade		
	Min	**Max**	**Unit**
$t_{LABCASC}$		1.3	ns
$t_{LABCARRY}$		0.8	ns
$t_{LALOCAL}$		1.5	ns
t_{ROW}		6.3	ns
t_{COL}		3.8	ns
t_{DIN_C}		8.0	ns
t_{DIN_D}		10.8	ns
t_{DIN_IO}		9.0	ns

EPF8282AV Logic Element Timing Parameters			
Symbol	A-4 Speed Grade		
	Min	**Max**	**Unit**
t_{LUT}		7.3	ns
t_{CLUT}		1.4	ns
t_{RLUT}		5.1	ns
t_{GATE}		0.0	ns
t_{CASC}		2.8	ns
t_{CICO}		1.5	ns
t_{CGEN}		2.2	ns
t_{CGENR}		3.7	ns
t_{C}		4.7	ns
t_{CH}		6.0	ns
t_{CL}		6.0	ns
t_{CO}		0.9	ns
t_{COMB}		0.9	ns
t_{SU}	2.4		ns
t_{H}	4.6		ns
t_{PRE}		1.3	ns
t_{CLR}		1.3	ns

EPF8282AV External Timing Parameters

Symbol	A-4 Speed Grade		
	Min	**Max**	**Unit**
t_{DRR}		50.1	ns
t_{ODH}	1		ns

EPF8452A Internal Timing Parameters

EPF8452A I/O Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOHt}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OvD1}		1.1		1.4		1.7	ns
t_{OD2}		-		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		-		2.1		2.3	ns
t_{ZvX3}		4.9		5.1		5.3	ns

EPF8452A Interconnect Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.4		0.4	ns
$t_{LABCARRY}$		0.3		0.4		0.4	ns
t_{LOCAL}		0.5		0.5		0.7	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

EPF8452A Logic Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.3		3.0	ns
t_{CLUT}		0.0		0.2		0.1	ns
t_{RLUT}		0.9		1.6		1.6	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.9		0.8	ns
t_{CGENR}		0.9		1.4		1.5	ns
t_{C}		1.6		1.8		2.4	ns
t_{CH}	1.7		1.7		2.7		ns
t_{CL}	1.7		1.7		2.7		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.0		1.1		ns
t_{H}	0.9		1.1		1.4		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

EPF8452A External Timing Parameters

Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1		1		1		ns

EPF8636A Internal Timing Parameters

EPF8636A I/O Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

EPF8636A Interconnect Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.4		0.4	ns
$t_{LABCARRY}$		0.3		0.4		0.4	ns
t_{LOCAL}		0.5		0.5		0.7	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

EPF8636A Logic Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.3		3.0	ns
t_{CLUT}		0.0		0.2		0.1	ns
t_{RLUT}		0.9		1.6		1.6	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.9		0.8	ns
t_{CGENR}		0.9		1.4		1.5	ns
t_{C}		1.6		1.8		2.4	ns
t_{CH}	1.7		1.7		2.7		ns
t_{CL}	1.7		1.7		2.7		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.0		1.1		ns
t_{H}	0.9		1.1		1.4		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

EPF8636A External Timing Parameters

Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1		1		1		ns

EPF8820A Internal Timing Parameters

EPF8820A I/O Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

EPF8820A Interconnect Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

EPF8820A Logic Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	1.7		1.7		2.7		ns
t_{CL}	1.7		1.7		2.7		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

EPF8820A External Timing Parameters

Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1		1		1		ns

EPF81188A Internal Timing Parameters

EPF81188A I/O Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

EPF81188A Interconnect Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

EPF81188A Logic Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	1.7		1.7		2.7		ns
t_{CL}	1.7		1.7		2.7		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

EPF81188A External Timing Parameters

Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1		1		1		ns

EPF81500A Internal Timing Parameters

EPF81500A I/O Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

EPF81500A Interconnect Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		6.2		6.2		6.2	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		8.2		8.2		8.7	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

EPF81500A Logic Element Timing Parameters							
Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	1.7		1.7		2.7		ns
t_{CL}	1.7		1.7		2.7		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

EPF81500A External Timing Parameters

Symbol	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.1		20.1		25.1	ns
t_{ODH}	1		1		1		ns

Power Consumption

The supply power for FLEX 8000 devices, P, can be calculated with the following equation:

$$P = P_{INT} + P_{IO}$$

$$= (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the "FLEX 8000 5.0-V Device DC Operating Conditions" table on page 120 and the "FLEX 8000 3.3-V Device DC Operating Conditions" table on page 121. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*. The $I_{CCACTIVE}$ value depends on the switching f requency and the application logic. This value can be calculated based on the amount of current that each LE typically consumes.

The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are as follows:

$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
N = Total number of logic cells used in the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock
K = Constant, shown in Table 11

Table 11. Values for Constant K

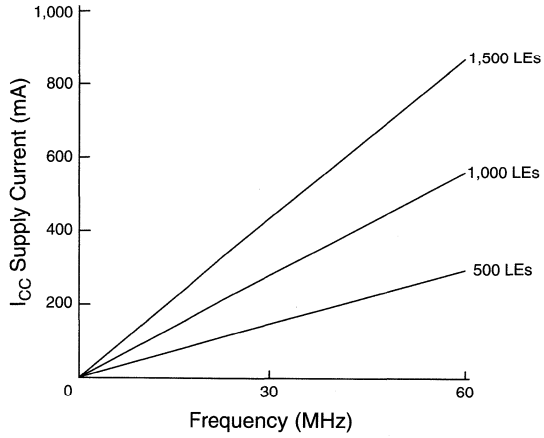
Device	K
5.0-V FLEX 8000A devices	75
3.3-V FLEX 8000A devices	60 (Preliminary)

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} value should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 19 shows the relationship between I_{CC} and operating frequency for several LE utilization values.

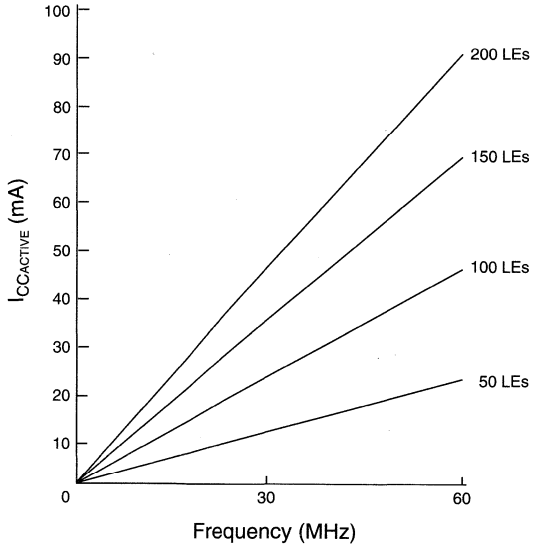
Figure 19. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency

5.0-V FLEX 8000A Devices



3.3-V FLEX 8000A Devices

Information on 3.3-V FLEX 8000A devices is preliminary.



Configuration & Operation

The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This data sheet summarizes the device operating modes and available device configuration schemes.

Go to *Application Note 33 (Configuring FLEX 8000 Devices)* for detailed descriptions of device configuration options; device configuration pins; and information on configuring FLEX 8000 devices, including sample schematics, timing diagrams, and configuration parameters.

Operating Modes

The FLEX 8000 architecture uses SRAM elements that require configuration data to be loaded whenever the device powers up and begins operation. The process of physically loading the SRAM programming data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The configuration and initialization processes together are called command mode; normal device operation is called user mode.

SRAM elements allow FLEX 8000 devices to be reconfigured in-circuit with new programming data that is loaded into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external EPROM devices, and completing the loading process. The clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device, which operates as a slave. Table 12 shows the data source for each of the six configuration schemes.

Table 12. Data Source for Configuration

Configuration Scheme	Acronym	Data Source
Active serial	AS	Altera Configuration EPROM
Active parallel up	APU	Parallel EPROM
Active parallel down	APD	Parallel EPROM
Passive serial	PS	Serial data path
Passive parallel synchronous	PPS	Intelligent host
Passive parallel asynchronous	PPA	Intelligent host

Device Pin-Outs

Tables 13 through 14 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

Table 13. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	84-Pin PLCC EPF8282A EPF8282AV	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A *Note (1)*	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A *Note (2)*
nSP *(3)*	75	75	75	76	110	R1	1
MSEL0 *(3)*	74	74	74	75	109	P2	2
MSEL1 *(3)*	53	53	51	51	72	A1	44
nSTATUS *(3)*	32	32	24	25	37	C13	82
nCONFIG *(3)*	33	33	25	26	38	A15	81
DCLK *(3)*	10	10	100	100	143	P14	125
CONF_DONE *(3)*	11	11	1	1	144	N13	124
nWS	30	30	22	23	33	F13	87
nRS	48	48	42	45	31	C6	89
RDCLK	49	49	45	46	12	B5	110
nCS	29	29	21	22	4	D15	118
CS	28	28	19	21	3	E15	121
RDYnBUSY	77	77	77	78	20	P3	100
CLKUSR	50	50	47	47	13	C5	107
ADD17	51	51	49	48	75	B4	40
ADD16	36	55	28	54	76	E2	39
ADD15	56	56	55	55	77	D1	38
ADD14	57	57	57	57	78	E1	37
ADD13	58	58	58	58	79	F3	36
ADD12	60	60	59	60	83	F2	32
ADD11	61	61	60	61	85	F1	30
ADD10	62	62	61	62	87	G2	28
ADD9	63	63	62	64	89	G1	26
ADD8	64	64	64	65	92	H1	22
ADD7	65	65	65	66	94	H2	20
ADD6	66	66	66	67	95	J1	18
ADD5	67	67	67	68	97	J2	16
ADD4	69	69	68	70	102	K2	11
ADD3	70	70	69	71	103	K1	10
ADD2	71	71	71	72	104	K3	8
ADD1	76	72	76	73	105	M1	7
ADD0	78	76	78	77	106	N3	6
DATA7	3	2	90	89	131	P8	140
DATA6	4	4	91	91	132	P10	139

Table 13. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	84-Pin PLCC EPF8282A EPF8282AV	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A *Note (1)*	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A *Note (2)*
DATA5	6	6	92	95	133	R12	138
DATA4	7	7	95	96	134	R13	136
DATA3	8	8	97	97	135	P13	135
DATA2	9	9	99	98	137	R14	133
DATA1	13	13	4	4	138	N15	132
DATA0	14	14	5	5	140	K13	129
TDI *(4)*	55	45 *(5)*	54	–	96	–	17
TDO *(4)*	27	27 *(5)*	18	–	18	–	102
TCK *(4)*	72	44 *(5)*	72	–	88	–	27
TMS *(4)*	20	43 *(5)*	11	–	86	–	29
nTRST *(3)*	52	52 *(6)*	50	–	71	–	45
Dedicated Inputs	12, 31, 54, 73	12, 31, 54, 73	3, 23, 53, 73	3, 24, 53, 74	9, 26, 82, 99	C3, D14, N2, R15	14, 33, 94, 113
VCCINT	17, 38, 59, 80	17, 38, 59, 80	6, 20, 37, 56, 70, 87	9, 32, 49, 59, 82	8, 28, 70, 90, 111	B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12	3, 24, 46, 92, 114, 160
VCCIO	–	–	–	–	16, 40, 60, 69, 91, 112, 122, 141	–	23, 47, 57, 69, 79, 104, 127, 137, 149, 159
GND	5, 26, 47, 68	5, 26, 47, 68	2, 13, 30, 44, 52, 63, 80, 94	19, 44, 69, 94	7, 17, 27, 39, 54, 80, 81, 100,101, 128, 142	C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4	12, 13, 34, 35, 51, 63, 75, 80, 83, 93, 103, 115, 126, 131, 143, 155

Table 13. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	84-Pin PLCC EPF8282A EPF8282AV	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A *Note (1)*	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A *Note (2)*
No Connect (N.C.)	–	–	–	2, 6, 13, 30, 37, 42, 43, 50, 52, 56, 63, 80, 87, 92, 93, 99	–	–	–
Total User I/O Pins	64	64	74	64	108	116	116

Table 14. FLEX 8000 160-, 192-, 208- & 225-Pin Package Pin-Outs (Part 1 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EFP8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP/RQFP EPF8636A *Notes (1), (2)*	208-Pin PQFP/RQFP EPF8820A *Notes (1), (2)*	208-Pin PQFP EPF81188A *Note (2)*
nSP *(3)*	120	1	R15	207	207	5
MSEL0 *(3)*	117	3	T15	4	4	21
MSEL1 *(3)*	84	38	T3	49	49	33
nSTATUS *(3)*	37	83	B3	108	108	124
nCONFIG *(3)*	40	81	C3	103	103	107
DCLK *(3)*	1	120	C15	158	158	154
CONF_DONE *(3)*	4	118	B15	153	153	138
nWS	30	89	C5	114	114	118
nRS	71	50	B5	66	116	121
RDCLK	73	48	C11	64	137	137
nCS	29	91	B13	116	145	142
CS	27	93	A16	118	148	144
RDYnBUSY	125	155	A8	201	127	128
CLKUSR	76	44	A10	59	134	134
ADD17	78	43	R5	57	43	46
ADD16	91	33	U3	43	42	45
ADD15	92	31	T5	41	41	44
ADD14	94	29	U4	39	40	39
ADD13	95	27	R6	37	39	37
ADD12	96	24	T6	31	35	36
ADD11	97	23	R7	30	33	31
ADD10	98	22	T7	29	31	30
ADD9	99	21	T8	28	29	29
ADD8	101	20	U9	24	25	26
ADD7	102	19	U10	23	23	25
ADD6	103	18	U11	22	21	24
ADD5	104	17	U12	21	19	18
ADD4	105	13	R12	14	14	17
ADD3	106	11	U14	12	13	16
ADD2	109	9	U15	10	11	10
ADD1	110	7	R13	8	10	9
ADD0	123	157	U16	203	9	8
DATA7	144	137	H17	178	178	177
DATA6	150	132	G17	172	176	175
DATA5	152	129	F17	169	174	172

Table 14. FLEX 8000 160-, 192-, 208- & 225-Pin Package Pin-Outs (Part 2 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EFP8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP/RQFP EPF8636A *Notes (1), (2)*	208-Pin PQFP/RQFP EPF8820A *Notes (1), (2)*	208-Pin PQFP EPF81188A *Note (2)*
DATA4	154	127	E17	165	172	170
DATA3	157	124	G15	162	171	168
DATA2	159	122	F15	160	167	166
DATA1	11	115	E16	149	165	163
DATA0	12	113	C16	147	162	161
TDI *(4)*	–	55	R11	72	20	–
TDO *(4)*	–	95	B9	120	129	–
TCK *(4)*	–	57	U8	74	30	–
TMS *(4)*	–	59	U7	76	32	–
nTRST *(3)*	–	40	R3	54	54	–
Dedicated Inputs	5, 36, 85, 116	6, 35, 87, 116	A5, U5, U13, A13	7, 45, 112, 150	17, 36, 121, 140	13, 41, 116, 146
VCCINT (5.0 V)	21, 41, 53, 67, 80, 81, 100, 121, 133, 147, 160	4, 5, 26, 85, 106	C8, C9, C10, R8, R9, R10, R14	5, 6, 33, 110, 137	5, 6, 27, 48, 119, 141	4, 20, 35, 48, 50, 102, 114, 131, 147
VCCIO (5.0 V or 3.3 V)	–	25, 41, 60, 70, 80, 107, 121, 140, 149, 160	D3, D4, D9, D14, D15, G4, G14, L4, L14, P4, P9, P14	32, 55, 78, 91, 102, 138, 159, 182, 193, 206	26, 55, 69, 87, 102, 131, 159, 173, 191, 206	3, 19, 34, 49, 69, 87, 106, 123, 140, 156, 174, 192
GND	13, 14, 28, 46, 60, 75, 93, 107, 108, 126, 140, 155	15, 16, 36, 37, 45, 51, 75, 84, 86, 96, 97, 117, 126, 131, 154	C4, D7, D8, D10, D11, H4, H14, K4, K14, P7, P8, P10, P11	19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200	15, 16, 37, 38, 60, 78, 96, 109, 110, 120, 130, 142, 152, 164, 182, 200	11, 12, 27, 28, 42, 43, 60, 78, 96, 105, 115, 122, 132, 139, 148, 155, 159, 165, 183, 201
No Connect (N.C.)	2, 3, 38, 39, 70, 82, 83, 118, 119, 148	2, 39, 82, 119	C6, C12, C13, C14, E3, E15, F3, J3, J4, J14, J15, N3, N15, P3, P15, R4, *(7)*	1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208	1, 2, 3, 50, 51, 52, 53, 104, 105, 106, 107, 154, 155, 156, 157, 208	1, 2, 51, 52, 53, 54, 103, 104, 157, 158, 207, 208
Total User I/O Pins	116	114	132, 148, *(8)*	132	148	144

Table 15. FLEX 8000 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin RQFP EPF81188A	240-Pin RQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
nSP *(3)*	A15	C14	237	237	W1	304
MSEL0 *(3)*	B14	G15	21	19	N1	26
MSEL1 *(3)*	R15	L15	40	38	H3	51
nSTATUS *(3)*	P2	L3	141	142	G19	178
nCONFIG *(3)*	R1	R4	117	120	B18	152
DCLK *(3)*	B2	C4	184	183	U18	230
CONF_DONE *(3)*	A1	G3	160	161	M16	204
nWS	L4	P1	133	134	F18	167
nRS	K5	N1	137	138	G18	171
RDCLK	F1	G2	158	159	M17	202
nCS	D1	E2	166	167	N16	212
CS	C1	E3	169	170	N18	215
RDYnBUSY	J3	K2	146	147	J17	183
CLKUSR	G2	H2	155	156	K19	199
ADD17	M14	R15	58	56	E3	73
ADD16	L12	T17	56	54	E2	71
ADD15	M15	P15	54	52	F4	69
ADD14	L13	M14	47	45	G1	60
ADD13	L14	M15	45	43	H2	58
ADD12	K13	M16	43	41	H1	56
ADD11	K15	K15	36	34	J3	47
ADD10	J13	K17	34	32	K3	45
ADD9	J15	J14	32	30	K4	43
ADD8	G14	J15	29	27	L1	34
ADD7	G13	H17	27	25	L2	32
ADD6	G11	H15	25	23	M1	30
ADD5	F14	F16	18	16	N2	20
ADD4	E13	F15	16	14	N3	18
ADD3	D15	F14	14	12	N4	16
ADD2	D14	D15	7	5	U1	8
ADD1	E12	B17	5	3	U2	6
ADD0	C15	C15	3	1	V1	4
DATA7	A7	A7	205	199	W13	254
DATA6	D7	D8	203	197	W14	252
DATA5	A6	B7	200	196	W15	250
DATA4	A5	C7	198	194	W16	248

Table 15. FLEX 8000 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin RQFP EPF81188A	240-Pin RQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
DATA3	B5	D7	196	193	W17	246
DATA2	E6	B5	194	190	V16	243
DATA1	D5	A3	191	189	U16	241
DATA0	C4	A2	189	187	V17	239
TDI	F15	–	–	63 *(9)*	B1 *(9)*	80 *(9)*
TDO	J2	–	–	117 *(9)*	C17 *(9)*	149 *(9)*
TCK	J14	–	–	116 *(9)*	A19 *(9)*	148 *(9)*
TMS	J12	–	–	64 *(9)*	C2 *(9)*	81 *(9)*
nTRST *(3)*	P14	–	–	115	A18	145
Dedicated Inputs	F4, L1, K12, E15	C1, C17, R1, R17	10, 51, 130, 171	8, 49, 131, 172	F1, F16, P3, P19	12, 64, 164, 217
VCCINT (5.0 V)	F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13	E4, H4, L4, P12, L14, H14, E14, R14, U1	20, 42, 64, 66, 114, 128, 150, 172, 236	18, 40, 60, 62, 91, 114, 129, 151, 173, 209, 236	B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301
VCCIO (5.0 V or 3.3 V)	H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2	N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13	19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235	17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300
GND	B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1	A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14	8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229	6, 7, 28, 29, 50, 51, 71, 85, 92, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 214, 228	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, U17	9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291

Table 15. FLEX 8000 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin RQFP EPF81188A	240-Pin RQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
No Connect (N.C.)	–	–	61, 62, 119, 120, 181, 182, 239, 240	–	–	10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303
Total User I/O Pins	148	180	180	177	204	204

Notes to Tables 13 through 15:

(1) Information for the following devices is preliminary: EPF8820A in 208-pin PQFP and 144-pin TQFP packages, EPF8636A in 208-pin PQFP packages.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* in this data book for more information.
(3) This is a dedicated pin and is not available as a user I/O pin.
(4) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(5) JTAG pins are available for EPF8636A devices only. These pins are dedicated user I/O pins.
(6) Pin 52 is a V_{CC} pin on EPF8452A devices only.
(7) These pins are no connect (N.C.) pins for EPF8636A devices only. They are user I/O pins in EPF8820A devices.
(8) EPF8636A devices have 132 user I/O pins; EPF8820A devices have 148 user I/O pins.
(9) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins.

Notes:

June 1996

MAX 9000 Programmable Logic Device Family Data Sheet


ALTERA
MAX®
EPM9320GC280-15
ALTERA
MAX®
EPM9400LC84-15
ALTERA
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MAX 9000

Programmable Logic Device Family

June 1996, ver. 4 — Data Sheet

Features...

- High-performance CMOS EEPROM-based programmable logic devices (PLDs) built on third-generation Multiple Array MatriX (MAX) architecture
- 5.0-V in-system programmability (ISP) through built-in JTAG interface
- High-density EPLD family ranging from 6,000 to 12,000 usable gates (see Table 1)
- 12-ns pin-to-pin logic delays with counter frequencies up to 125 MHz
- PCI-compliant -12 speed grade
- Built-in JTAG boundary-scan test (BST) circuitry as compliant with IEEE Std 1149.1-1990
- Dual-output macrocell for independent use of combinatorial and registered logic
- FastTrack Interconnect continuous routing structure for fast, predictable interconnect delays
- Input/output registers with clear and clock enable on all I/O pins
- Programmable output slew-rate control to reduce switching noise
- 3.3-V or 5.0-V I/O operation on all devices
- Configurable expander product-term distribution allowing up to 32 product terms per macrocell
- Programmable power-saving mode for more than 50% power reduction in each macrocell
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls

Table 1. MAX 9000 Device Features

Feature	EPM9320	EPM9400	EPM9480	EPM9560
Usable gates	6,000	8,000	10,000	12,000
Flipflops	484	580	676	772
Macrocells	320	400	480	560
Logic array blocks (LABs)	20	25	30	35
Maximum user I/O pins	168	159	175	216
t_{PD1} (ns)	12	12	12	12
t_{FSU} (ns)	4	4	4	4
t_{FCO} (ns)	5.5	5.5	5.5	5.5
f_{CNT} (MHz)	125	125	118	118

... and More Features

- Programmable security bit for protection of proprietary designs
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS II development system on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar, Mentor Graphics, MINC, OrCAD, Synopsys, VeriBest, and Viewlogic
- Programming support with Altera's Master Programming Unit (MPU) and BitBlaster serial download cable, as well as programming hardware from other manufacturers
- Offered in a variety of package options with 84 to 356 pins (see Table 2)

Table 2. MAX 9000 Package Options & I/O Count *Note (1)*

Device	84-Pin PLCC	208-Pin RQFP	240-Pin RQFP	280-Pin PGA	304-Pin RQFP	356-Pin BGA
EPM9320	60 *(2)*	132	–	168	–	168
EPM9400	59 *(2)*	139	159	–	–	–
EPM9480	–	146	175	–	–	–
EPM9560	–	153	191	216	216	216

Notes:

(1) Contact Altera Customer Marketing at (408) 894-7104 for up-to-date information on package availability.

(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* in this data book for more information.

General Description

The MAX 9000 family of in-system-programmable, high-density, high-performance EPLDs is based on Altera's third-generation MAX architecture. Fabricated on an advanced CMOS technology, the EEPROM-based MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 12 ns, and counter speeds of up to 125 MHz. The -12 speed grade of the MAX 9000 family is compliant with the ***PCI Local Bus Specification***, version 2. Table 3 shows the speed grades available for MAX 9000 devices.

Table 3. MAX 9000 Speed Grade Availability

Device	Speed Grade		
	-12	-15	-20
EPM9320	✓ (1)	✓	✓
EPM9400	✓ (1)	✓	✓
EPM9480	✓ (1)	✓	✓
EPM9560	✓ (1)	✓	✓

Note:
(1) This information is preliminary. Contact Altera for up-to-date information on package availability.

Table 4 shows the performance of MAX 9000 devices for typical functions.

Table 4. MAX 9000 Performance *Note (1)*

Application	Macrocells Used	Speed Grade			Unit
		-12 (2)	-15	-20	
16-bit loadable counter	16	125	118	100	MHz
16-bit up/down counter	16	125	118	100	MHz
16-bit prescaled counter	16	125	118	100	MHz
16-bit address decode	1	6.5 (12)	7.9 (15)	10 (20)	ns
16-to-1 multiplexer	1	8.9 (14.4)	10.9 (18)	16 (26)	ns

Notes:
(1) Internal logic array block (LAB) performance is shown. Numbers in parentheses show external delays from row input to row I/O.
(2) This information is preliminary.

The MAX 9000 architecture supports high-density integration of system-level logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to field-programmable gate array (FPGA) devices and erasable programmable logic devices (EPLDs). With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 9000 EPLDs are also ideal for gate-array prototyping.

All MAX 9000 device packages provide four dedicated inputs for global control signals with large fan-outs. Each I/O pin has an associated I/O cell register with a clock enable control on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

MAX 9000 EPLDs provide 5.0-V in-system programmability (ISP). This feature allows the devices to be programmed and reprogrammed on the printed circuit board (PCB) for quick and efficient iterations during design development and debug cycles. MAX 9000 devices are guaranteed for 100 program and erase cycles.

MAX 9000 EPLDs contain from 320 to 560 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. For increased flexibility, each macrocell offers a dual-output structure that allows the register and the product terms to be used independently. This feature allows register-rich and combinatorial-intensive designs to be implemented efficiently. The dual-output structure of the MAX 9000 macrocell also improves logic utilization, thus increasing the effective capacity of the devices. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 9000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the user to configure one or more macrocells to operate at 50% or less power while adding only a nominal timing delay. MAX 9000 devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. MAX 9000 output drivers can be set for either 3.3-V or 5.0-V operation, allowing MAX 9000 devices to be used in mixed-voltage systems.

The MAX 9000 family is supported by Altera's MAX+PLUS II development system, a single, integrated software package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

For more information on development tools, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

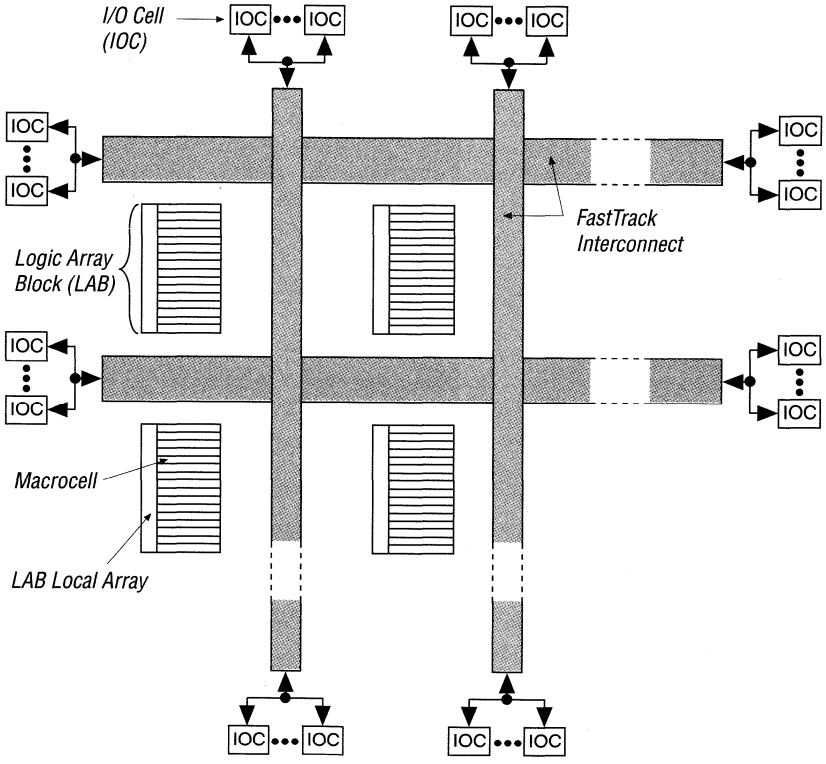
Functional Description

MAX 9000 devices use third-generation MAX architecture that yields both high performance and a high degree of utilization for most applications. The MAX 9000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- FastTrack Interconnect
- Dedicated inputs
- I/O cells

Figure 1 shows a block diagram of the MAX 9000 architecture.

Figure 1. MAX 9000 Device Block Diagram



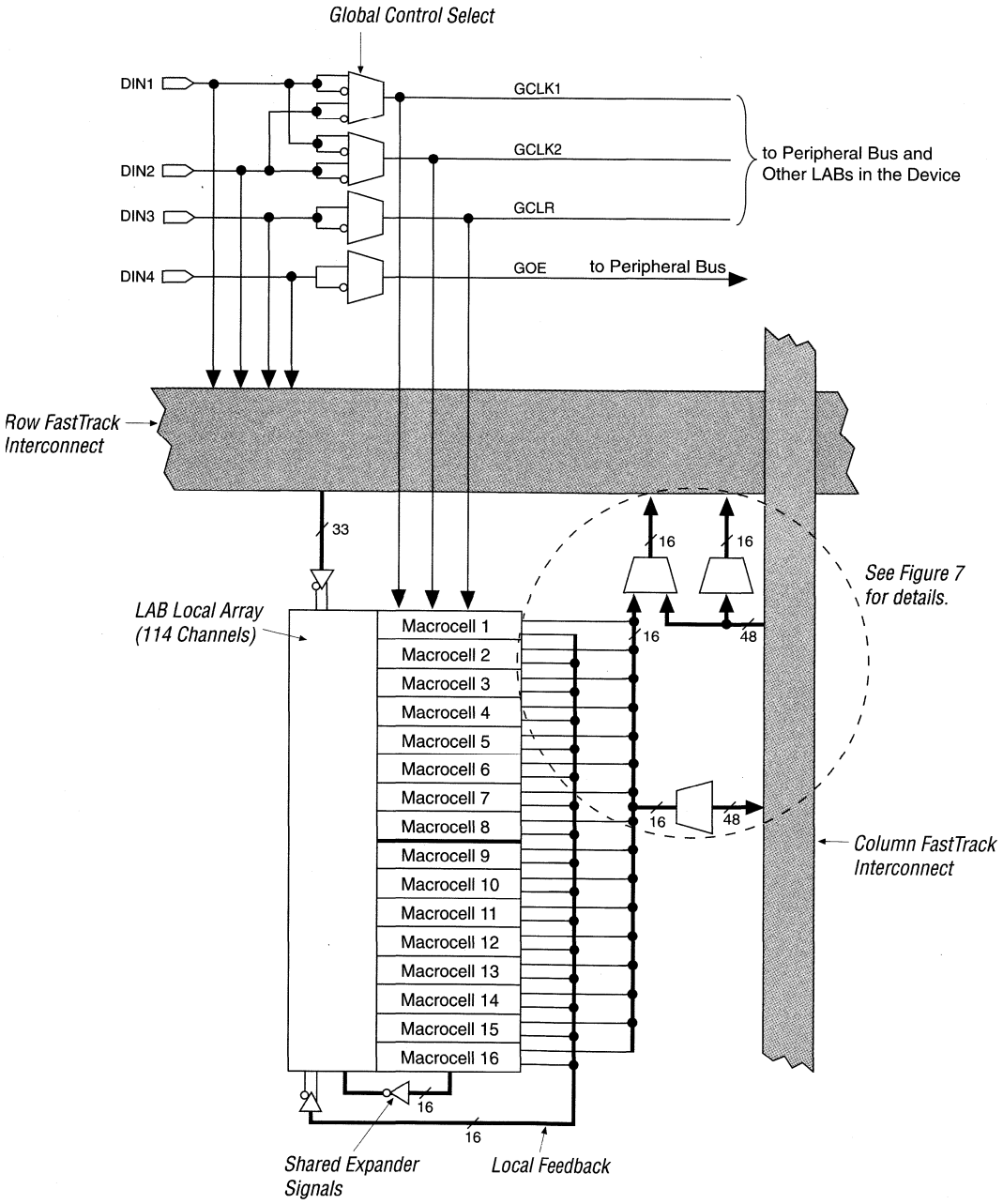
Logic Array Blocks

The MAX 9000 architecture is based on linking of high-performance, flexible logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays that are fed by the LAB local array, as shown in Figure 2. Multiple LABs are linked together via the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. The I/O pins are supported by I/O cells (IOCs) located at the end of each row (horizontal) and column (vertical) path of the FastTrack Interconnect.

Each LAB is fed by 33 inputs from the row interconnect and 16 feedback signals from the macrocells within the LAB. All of these signals are available within the LAB in their true and inverted form. In addition, 16 shared expander product terms ("expanders") are available in their inverted form, for a total of 114 signals that feed each product term in the LAB. Each LAB is also fed by two low-skew global clocks and one global clear that can be used for register control signals in all 16 macrocells.

The LAB drives the row and column interconnect directly. Each macrocell can drive out of the LAB onto one or both of these routing resources. Once signals are on the row or column interconnect, they can quickly traverse to other LABs or to the IOCs.

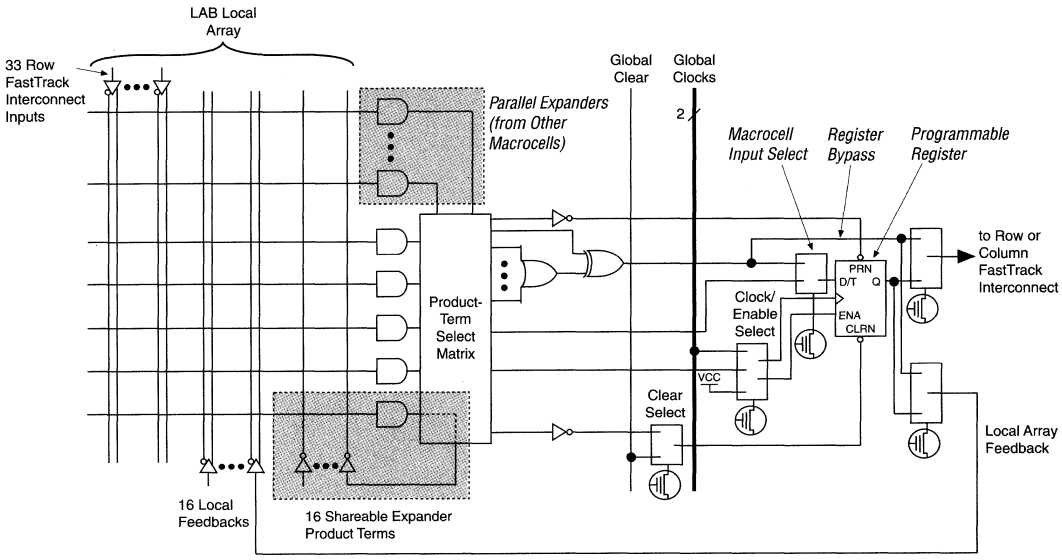
Figure 2. MAX 9000 Logic Array Block



Macrocells

The MAX 9000 macrocell consists of three functional blocks: the product terms, the product-term select matrix, and the programmable register. The macrocell can be individually configured for both sequential and combinatorial logic operation. See Figure 3.

Figure 3. MAX 9000 Macrocell & Local Array



Combinatorial logic is implemented in the local array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

MAX+PLUS II automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation with programmable clock control. The flipflop can also be bypassed for combinatorial operation. During design entry, the user specifies the desired register type; MAX+PLUS II then selects the most efficient register operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By either global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available. As shown in Figure 2, these global clock signals can be the true or the complement of either of the global clock pins, DIN1 and DIN2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the dedicated global clear pin (DIN3). The global clear can be programmed for active-high or active-low operation.

All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. This function is implemented by a process called register packing. When register packing is used, the product-term select matrix allocates one product term to the D input of the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.

Expander Product Terms

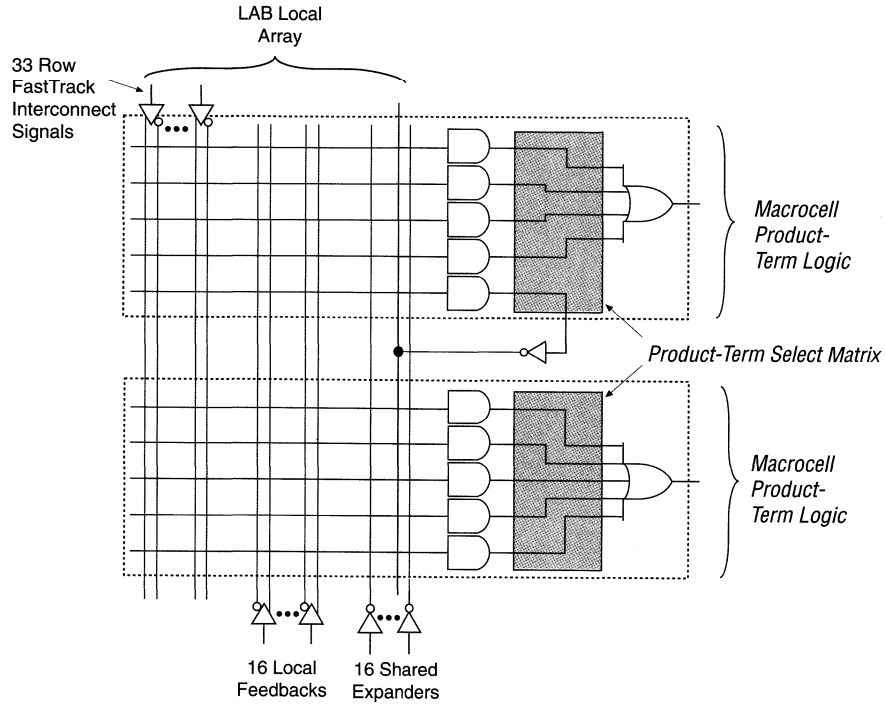
Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although another macrocell can supply the required logic resources, the MAX 9000 architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the LAB local array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{LOCAL} + t_{SEXP}$) is incurred when shareable expanders are used. Figure 4 shows how shareable expanders can feed multiple macrocells.

Figure 4. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in the LAB.

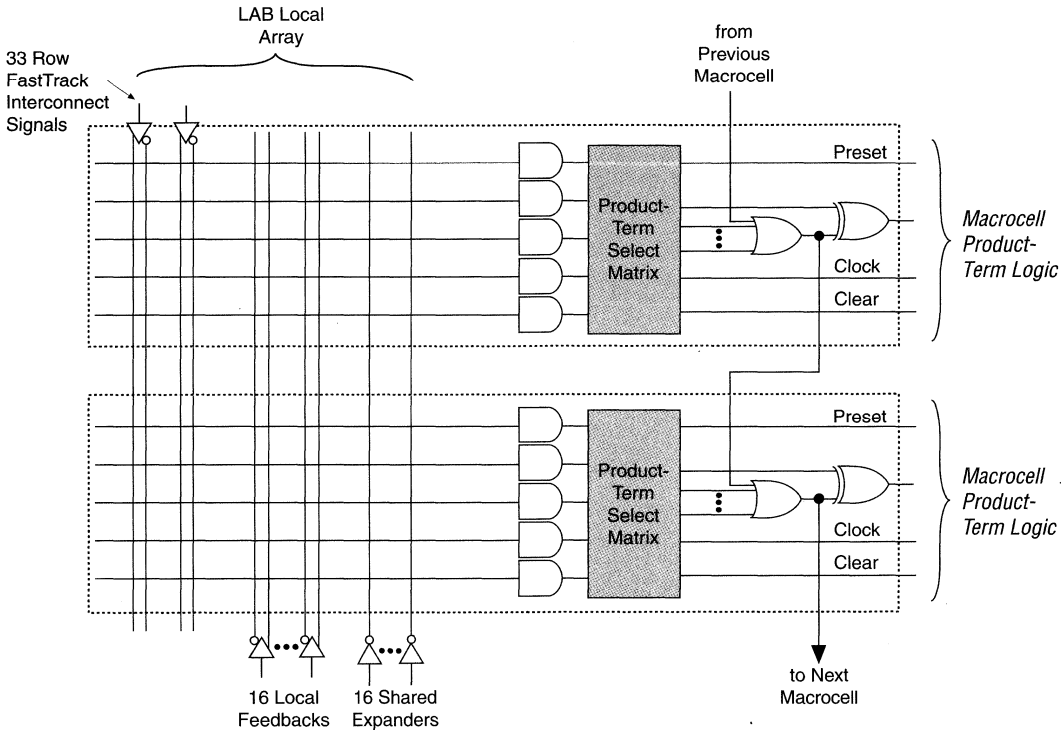


Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with 5 product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. Figure 5 shows how parallel expanders can feed the neighboring macrocell.

Figure 5. Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



The MAX+PLUS II Compiler can automatically allocate as many as 3 sets of up to 5 parallel expanders to the macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

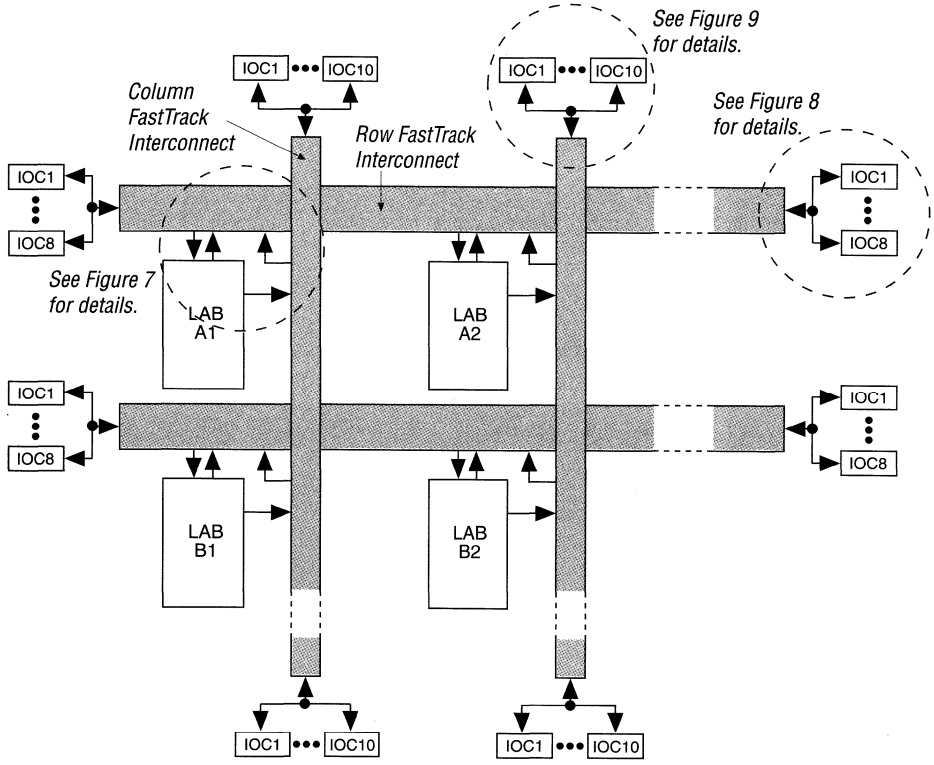
Two groups of 8 macrocells within each LAB (e.g., macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. Figure 6 shows the interconnection of four adjacent LABs with row and column interconnects.

Figure 6. MAX 9000 Device Interconnect Resources

Each LAB is named on the basis of its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.



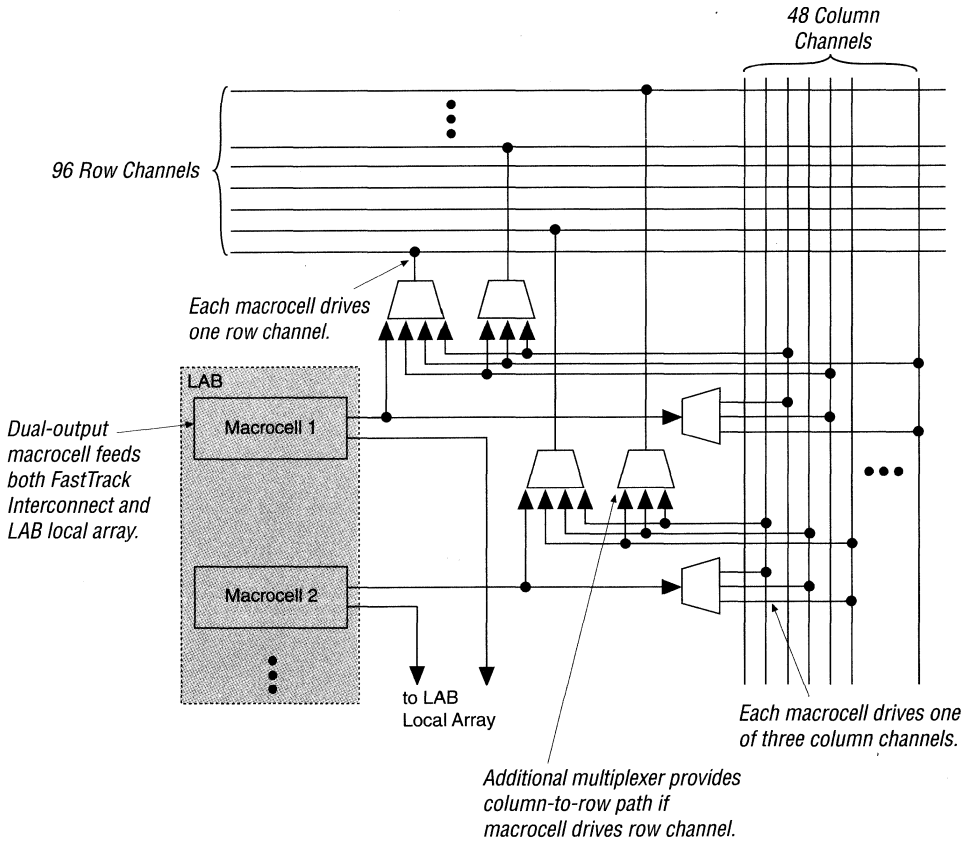
The LABs within MAX 9000 devices are arranged into a matrix of columns and rows. Table 5 shows the number of columns and rows in each MAX 9000 device.

Table 5. MAX 9000 Rows & Columns

Device	Rows	Columns
EPM9320	4	5
EPM9400	5	5
EPM9480	6	5
EPM9560	7	5

Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Each row interconnect has a total of 96 channels. Figure 7 shows how a macrocell drives the row and column interconnect.

Figure 7. LAB Connections to Row & Column Interconnect



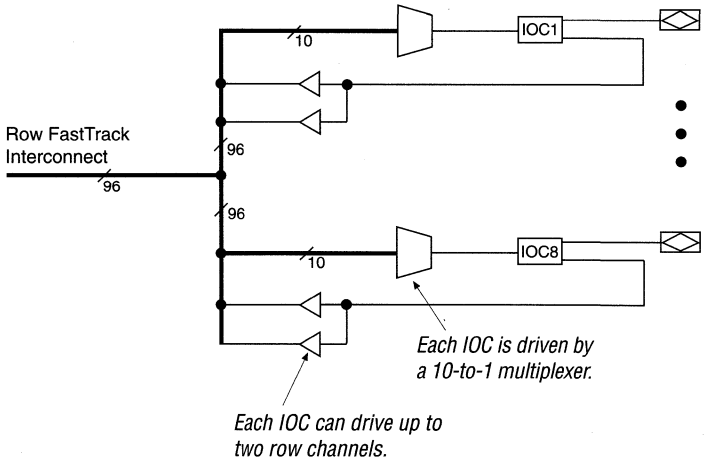
Each macrocell in the LAB can drive one of three separate column interconnect channels. The column channels run vertically across the entire device, and are shared by the macrocells in the same column. The MAX+PLUS II Compiler automatically optimizes connections to a column channel.

A row interconnect channel can be fed by the output of the macrocell through a 4-to-1 multiplexer that the macrocell shares with three column channels. If the multiplexer is used for a macrocell-to-row connection, the three column signals can access another row channel via an additional 3-to-1 multiplexer. Within any LAB, the multiplexers provide all 48 column channels with access to 32 row channels.

Row-to-I/O Cell Connections

Figure 8 illustrates the connections between row interconnect channels and I/O cells (IOCs). An input signal from an IOC can drive two separate row channels. When an IOC is used as an output, the signal is driven by a 10-to-1 multiplexer that selects the row channels. Each end of the row channel feeds up to eight IOCs on the periphery of the device.

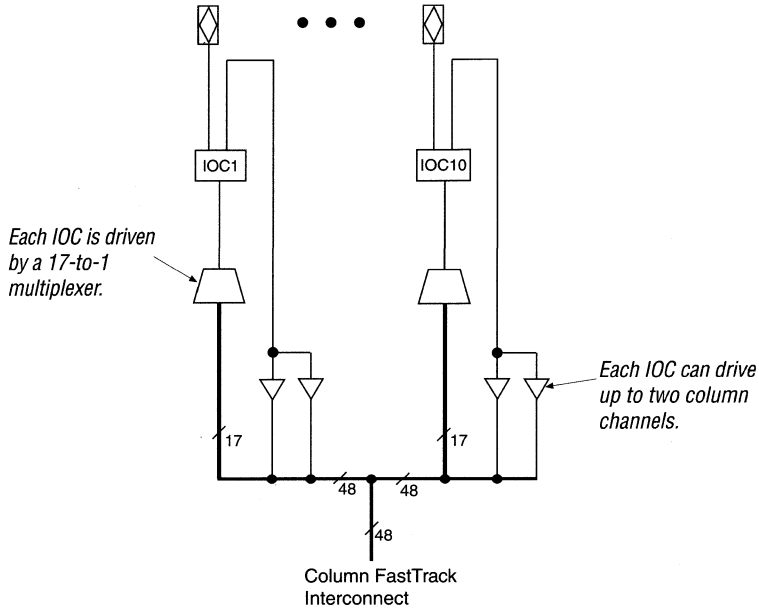
Figure 8. MAX 9000 Row-to-IOC Connections



Column-to-I/O Cell Connections

Each end of a column channel has up to 10 IOCs (see Figure 9). An input signal from an IOC can drive two separate column channels. When an IOC is used as an output, the signal is driven by a 17-to-1 multiplexer that selects the column channels.

Figure 9. MAX 9000 Column-to-IOC Connections



Dedicated Inputs

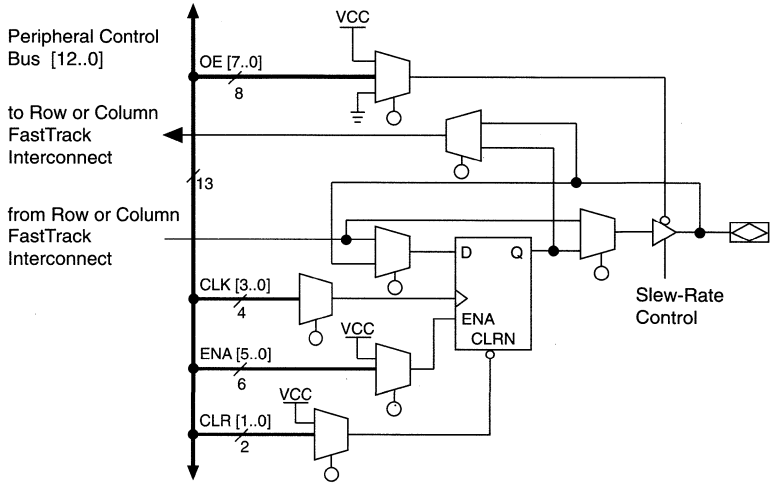
In addition to the general-purpose I/O pins, MAX 9000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution to the LABs and IOCs in the device, and are typically used for global clock, clear, and output enable control signals. The global control signals can feed the macrocell or IOC clock and clear inputs, as well as the IOC output enable. The dedicated inputs can also be used as general-purpose data inputs because they can feed the row FastTrack Interconnect.

I/O Cells

Figure 10 shows the I/O cell (IOC) block diagram. Signals enter the MAX 9000 device from either the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOCs are located at the ends of the row and column interconnect channels.

I/O pins can be used as input, output, or bidirectional pins. Each IOC has an IOC register with a clock enable input. This register can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The IOC register clock enable allows the global clock to be used for fast clock-to-output performance, while maintaining the flexibility required for selective clocking.

Figure 10. I/O Cell (IOC)



The clock, clock enable, clear, and output enable controls for the IOCs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOC control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to eight output enable signals, up to four clock signals, up to six clock enable signals, and up to two clear signals. Table 6 shows the sources that drive the peripheral bus and how the IOC control signals share the peripheral bus.

The output buffer in each IOC has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces board-level noise and adds a nominal timing delay to the output buffer delay (t_{OD}) parameter. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

Table 6. Peripheral Bus Sources

Peripheral Control Signal	Source			
	EPM9320	EPM9400	EPM9480	EPM9560
OE0/ENA0	Row C	Row E	Row F	Row G
OE1/ENA1	Row B	Row E	Row F	Row F
OE2/ENA2	Row A	Row E	Row E	Row E
OE3/ENA3	Row B	Row B	Row B	Row B
OE4/ENA4	Row A	Row A	Row A	Row A
OE5	Row D	Row D	Row D	Row D
OE6	Row C	Row C	Row C	Row C
OE7/CLR1	Row B/GOE	Row B/GOE	Row B/GOE	Row B/GOE
CLR0/ENA5	Row A/GCLR	Row A/GCLR	Row A/GCLR	Row A/GCLR
CLK0	GCLK1	GCLK1	GCLK1	GCLK1
CLK1	GCLK2	GCLK2	GCLK2	GCLK2
CLK2	Row D	Row D	Row D	Row D
CLK3	Row C	Row C	Row C	Row C

3.3-V or 5.0-V I/O Operation

All MAX 9000 devices can be set to interface at 3.3 V or 5.0 V. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCINT} pins must always be connected to a 5.0-V supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs. The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V supply, the output high is at 3.3 V and is therefore compatible with 3.3-V systems. Devices operating with a V_{CCIO} level below 4.75 V incur a nominal timing delay adder for the output buffer delay (t_{OD}).

In-System Programmability (ISP)

MAX 9000 devices can be programmed in-system through a 4-pin JTAG BST interface. In-system programmability (ISP) offers quick and efficient iterations during design development and debug cycles. The MAX 9000 architecture internally generates the 12.0-V programming voltage required to program EEPROM cells, eliminating the need for an external 12.0-V power supply to program the devices on the board. During ISP, the I/O pins are tri-stated to eliminate board conflicts.

ISP simplifies the manufacturing flow by allowing the devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 9000 devices can be programmed by downloading the information via automatic test equipment, embedded processors, or the Altera BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high pin-count packages (e.g., QFP packages) due to device handling. MAX 9000 devices can be reprogrammed in the field. For example, product upgrades can be performed in the field via software or modem.

Go to *Application Brief 141 (In-System Programmability in MAX 9000 Devices)* for more information.

Programming with External Hardware

MAX 9000 devices can be programmed on 486- and Pentium-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. For more information, see *Altera's Programming Hardware Data Sheet* in this data book.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 9000 device with the results of simulation.

Data I/O and other programming hardware manufacturers also provide programming support for Altera devices. See *Programming Hardware Manufacturers* in this data book for more information.

JTAG Operation

All MAX 9000 devices provide JTAG BST circuitry as specified by IEEE Std 1149.1-1990. The supported features are SAMPLE/PRELOAD, EXTEST, and BYPASS. MAX 9000 devices have four dedicated JTAG pins that are used for JTAG BST and in-system programming.

For detailed information on JTAG operation in MAX 9000 devices, refer to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)*.

Programmable Speed/Power Control

MAX 9000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, since most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 9000 device for either high-speed (Turbo Bit on) or low-power (Turbo Bit off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the LAB local array delay (t_{LOCAL}).

Design Security

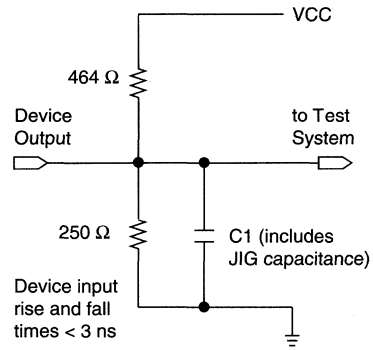
All MAX 9000 EPLDs contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased.

Generic Testing

MAX 9000 EPLDs are fully functionally tested. Complete testing of each programmable EEPROM bit and all logic functionality ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 11. Test patterns can be used and then erased during the early stages of the production flow.

Figure 11. MAX 9000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold test must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



QFP Carrier & Development Socket

MAX 9000 devices in QFP packages with 100 or more pins can be shipped in plastic carriers to protect the fragile QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress. When programming in-system, devices in QFP packages generally do not require a carrier and a prototype development socket.

For detailed information, go to the *QFP Carrier & Development Socket Data Sheet* in this data book.

MAX 9000 Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
V_{CCISP}	Supply voltage during in-system programming		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		Plastic and power quad flat pack packages, under bias		135	° C

MAX 9000 Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output drivers, 5.0-V operation	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	*Note (3)*	3.00	3.60	V
V_{CCISP}	Supply voltage during in-system programming		4.75	5.25	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

MAX 9000 Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V high level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V, *Note (7)*	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.0 V, *Note (7)*	2.4		V
V_{OL}	5.0-V high level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V, *Note (7)*		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.0 V, *Note (7)*		0.45	
I_I	Input leakage current	$V_I = V_{CC}$ or GND, *Note (8)*	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40	40	µA

MAX 9000 Device Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{DIN1}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		18	pF
C_{DIN2}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		18	pF
C_{DIN3}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		17	pF
C_{DIN4}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
$C_{I/O}$	I/O pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF

MAX 9000 Device Typical I_{CC} Supply Current Values

Symbol	Parameter	Conditions	EPM9320	EPM9400	EPM9480	EPM9560	Unit
I_{CC1}	I_{CC} supply current (low-power mode, standby, typical)	V_I = GND, No load, *Note (10)*	100	110	140	150	mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(3) V_{CC} must rise monotonically.

(4) Numbers in parentheses are for industrial-temperature-range versions.

(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.

(6) Operating conditions: V_{CCINT} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CCIO} = 5.0 V ± 5% for 5.0-V operation.
V_{CCIO} = 3.3 V ± 10% for 3.3-V operation.

(7) This parameter is measured with 50% of the outputs each sinking 12 mA. The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to the low-level TTL output current.

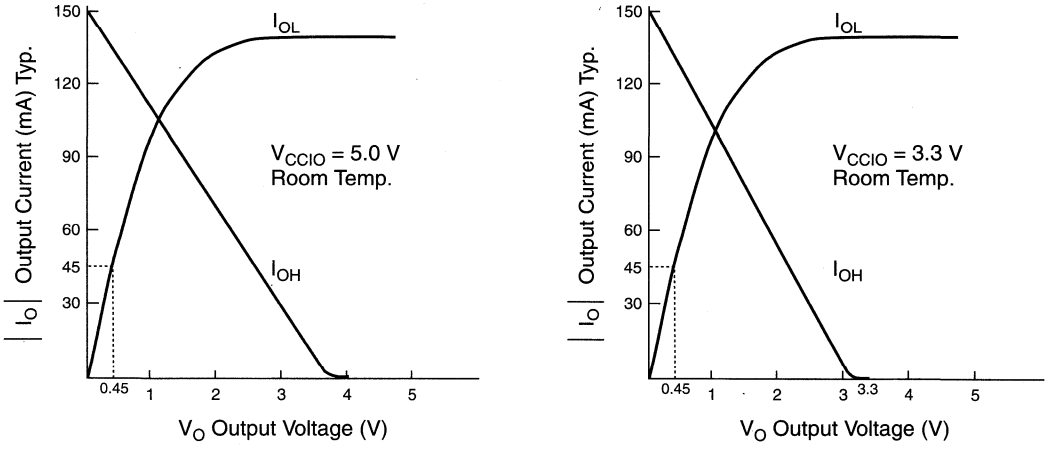
(8) JTAG input leakage is typically –60 µA.

(9) Capacitance sample-tested only and measured at 25° C.

(10) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.

Figure 12 shows typical output drive characteristics for MAX 9000 devices with 5.0-V and 3.3-V V_{CCIO}.

Figure 12. Output Drive Characteristics of MAX 9000 Devices *Note (1)*



Note:
(1) Output drive characteristics include a JTAG TDO pin.

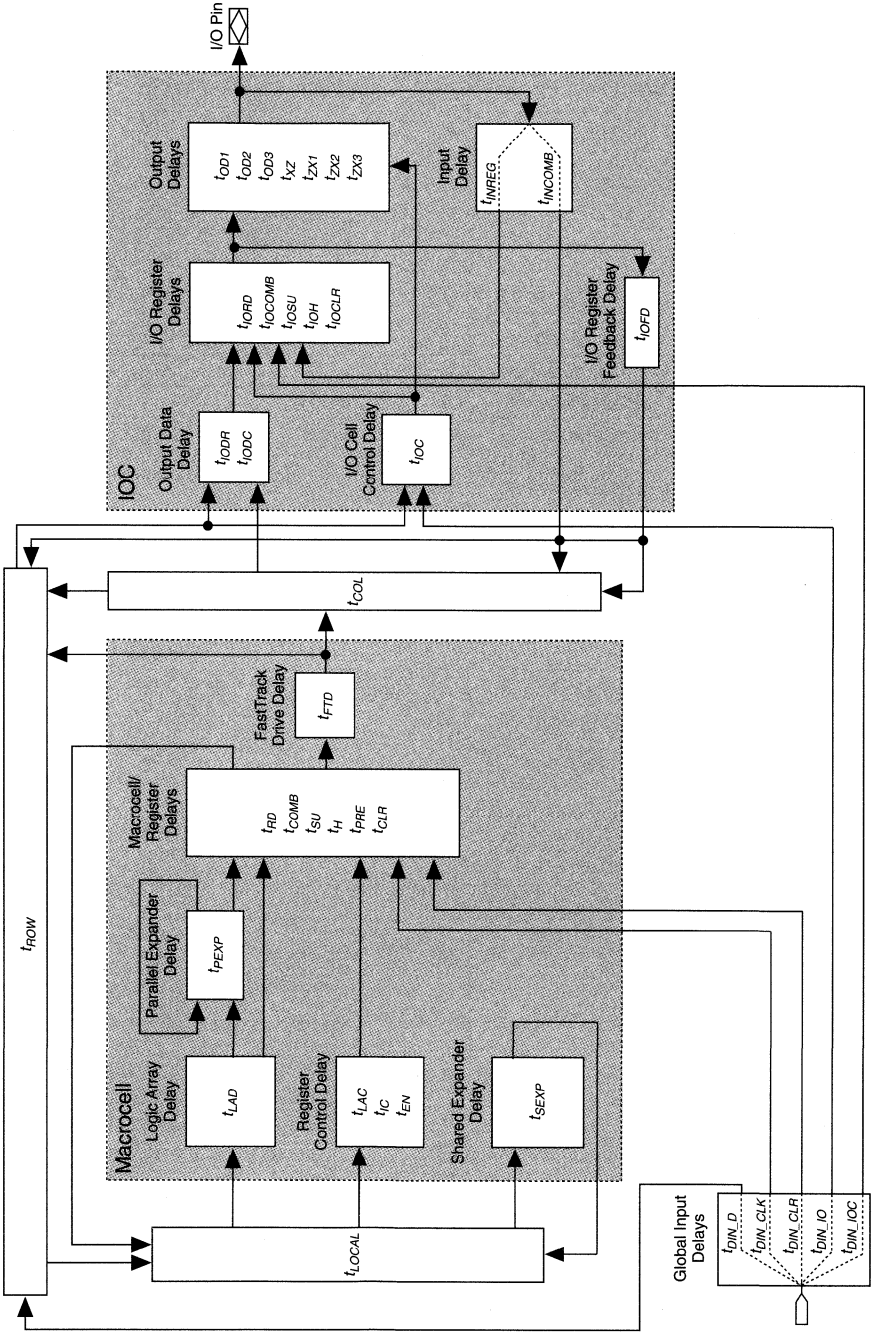
Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

The MAX 9000 timing model in Figure 13 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the macrocell; the IOC; and the interconnect, including the row and column FastTrack Interconnect and LAB local array paths. Each parameter shown in Figure 13 is expressed as a worst-case value in the "Internal Timing Characteristics" tables in this data sheet. Hand-calculations that use the MAX 9000 timing model and these timing parameters can be used to estimate MAX 9000 device performance.

For more information on calculating MAX 9000 timing delays, go to *Application Note 77* (*Understanding MAX 9000 Timing*) in this data book.

Figure 13. MAX 9000 Timing Model



MAX 9000 External Timing Characteristics *Note (1)*

				-12 Speed Grade *(2)*		-15 Speed Grade		-20 Speed Grade		
Symbol	**Parameter**	**Conditions**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Row I/O pin input to row I/O pin output	C1 = 35 pF, *Note (3)*			12.0		15.0		20.0	ns
t_{PD2}	Column I/O pin input to column I/O pin output	C1 = 35 pF	EPM9320		12.8		16.0		23.0	ns
			EPM9400		13.0		16.2		23.2	ns
			EPM9480		13.2		16.4		23.4	ns
			EPM9560		13.4		16.6		23.6	ns
t_{FSU}	Global clock setup time for I/O cell			4.0		5.0		6.0		ns
t_{FH}	Global clock hold time for I/O cell			0.0		0.0		0.0		ns
t_{FCO}	Global clock to I/O cell output delay	C1 = 35 pF			5.5		7.0		8.5	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (4)*		1.0		1.0		1.0		ns
t_{CNT}	Minimum internal global clock period	*Note (5)*			8.0		8.5		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*Note (5)*		125.0		117.6		100.0		MHz

MAX 9000 Internal Timing Characteristics *Note (1)*

Macrocell Delays			-12 Speed Grade *(2)*		-15 Speed Grade		-20 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LAD}	Logic array delay			3.8		4		4.5	ns
t_{LAC}	Logic control array delay			3.8		4		4.5	ns
t_{IC}	Array clock delay			3.8		4		4.5	ns
t_{EN}	Register enable time			3.8		4		4.5	ns
t_{SEXP}	Shared expander delay			4.1		5		7.5	ns
t_{PEXP}	Parallel expander delay			0.8		1		2	ns
t_{RD}	Register delay			0.8		1		1	ns
t_{COMB}	Combinatorial delay			0.6		1		1	ns
t_{SU}	Register setup time		3.0		3.0		4.0		ns
t_{H}	Register hold time		2.0		3.5		4.5		ns
t_{PRE}	Register preset time			3.9		4		4.5	ns
t_{CLR}	Register clear time			3.9		4		4.5	ns
t_{FTD}	FastTrack drive delay			0.7		1		2.0	ns
t_{LPA}	Low-power adder	*Note (6)*		12.0		15.0		20.0	ns

IOC Delays			-12 Speed Grade *(2)*		-15 Speed Grade		-20 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IODR}	I/O row output data delay			0.4		0.2		1.5	ns
t_{IODC}	I/O column output data delay			0.4		0.2		1.5	ns
t_{IOC}	I/O control delay	*Note (7)*		1.2		1.0		2.0	ns
t_{IORD}	I/O register clock-to-output delay			0.7		1.0		1.5	ns
t_{IOCOMB}	I/O combinatorial delay			0.3		1.0		1.5	ns
t_{IOSU}	I/O register setup time before clock		3.0		4.0		5.0		ns
t_{IOH}	I/O register hold time after clock		1.0		1.0		1.0		ns
t_{IOCLR}	I/O register clear delay			2.5		3.0		3.0	ns
t_{IOFD}	I/O register feedback delay			0.0		0.0		0.5	ns
t_{INREG}	I/O input pad and buffer to I/O register delay			3.8		4.5		5.5	ns
t_{INCOMB}	I/O input pad and buffer to row and column delay			1.8		2.0		2.5	ns
t_{OD1}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 5.0 V	*Note (8)*		2.0		2.5		2.5	ns
t_{OD2}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 3.3 V	*Note (8)*		3.0		3.5		3.5	ns
t_{OD3}	Output buffer and pad delay, Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	*Note (8)*		9.0		10.0		10.5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		2.0		2.5		2.5	ns
t_{ZX1}	Output buffer enable delay, Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF		2.0		2.5		2.5	ns
t_{ZX2}	Output buffer enable delay, Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF		3.0		3.5		3.5	ns
t_{ZX3}	Output buffer enable delay, Slow slew rate = on, V_{CCIO} = 3.3 V or 5.0 V	C1 = 35 pF		9.0		10.0		10.5	ns

Interconnect Delays			-12 Speed Grade *(2)*		-15 Speed Grade		-20 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LOCAL}	LAB local array delay			0.4		0.5		0.5	ns
t_{ROW}	FastTrack row delay	*Note (5)*		1.0		1.4		2.0	ns
t_{COL}	FastTrack column delay	*Note (5)*		1.2		1.7		3.0	ns
t_{DIN_D}	Dedicated input data delay			4.5		4.5		5.0	ns
t_{DIN_CLK}	Dedicated input clock delay			3.0		3.5		4.0	ns
t_{DIN_CLR}	Dedicated input clear delay			4.5		5.0		5.5	ns
t_{DIN_IOC}	Dedicated input I/O register clock delay			2.8		3.5		4.5	ns
t_{DIN_IO}	Dedicated input I/O register control delay			5.5		6.0		6.5	ns

Notes to tables:

(1) Operating conditions: $V_{CCINT} = 5.0\ V \pm 5\%$, $V_{CCIO} = 5.0\ V \pm 5\%$ (except where noted).
(2) Timing parameters for the -12 speed grade are preliminary.
(3) Go to *Application Note 77 (Understanding MAX 9000 Timing)* in this data book for more information on test conditions for t_{PD1} and t_{PD2} delays.
(4) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization. This parameter applies for both global and array clocking as well as both macrocell and I/O cell registers.
(5) Measured with a 16-bit loadable, enabled, up/down counter programmed in each LAB.
(6) The t_{LPA} parameter must be added to the t_{LOCAL} parameter for macrocells running in low-power mode.
(7) The t_{ROW}, t_{COL}, and t_{IOC} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(8) Operating conditions: $V_{CCIO} = 5.0\ V \pm 5\%$ for 5-V operation.
$V_{CCIO} = 3.3\ V \pm 10\%$ for 3.3-V operation.

Power Consumption

Supply power (P) versus frequency (f_{MAX}) for MAX 9000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO}$$

$$P = I_{CCACTIVE} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in this data book. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times tog_{LC}$$

The parameters in this equation are as follows:

MC_{TON} = Number of macrocells with Turbo Bit on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Number of macrocells used in the design, as reported in the MAX+PLUS II Report File (**.rpt**)
f_{MAX} = Highest clock frequency to the device
tog_{LC} = Average ratio of logic cells toggling at each clock (typically 0.125)
A, B, C = Constants, shown in Table 7

Table 7. MAX 9000 I_{CC} Equation Constants

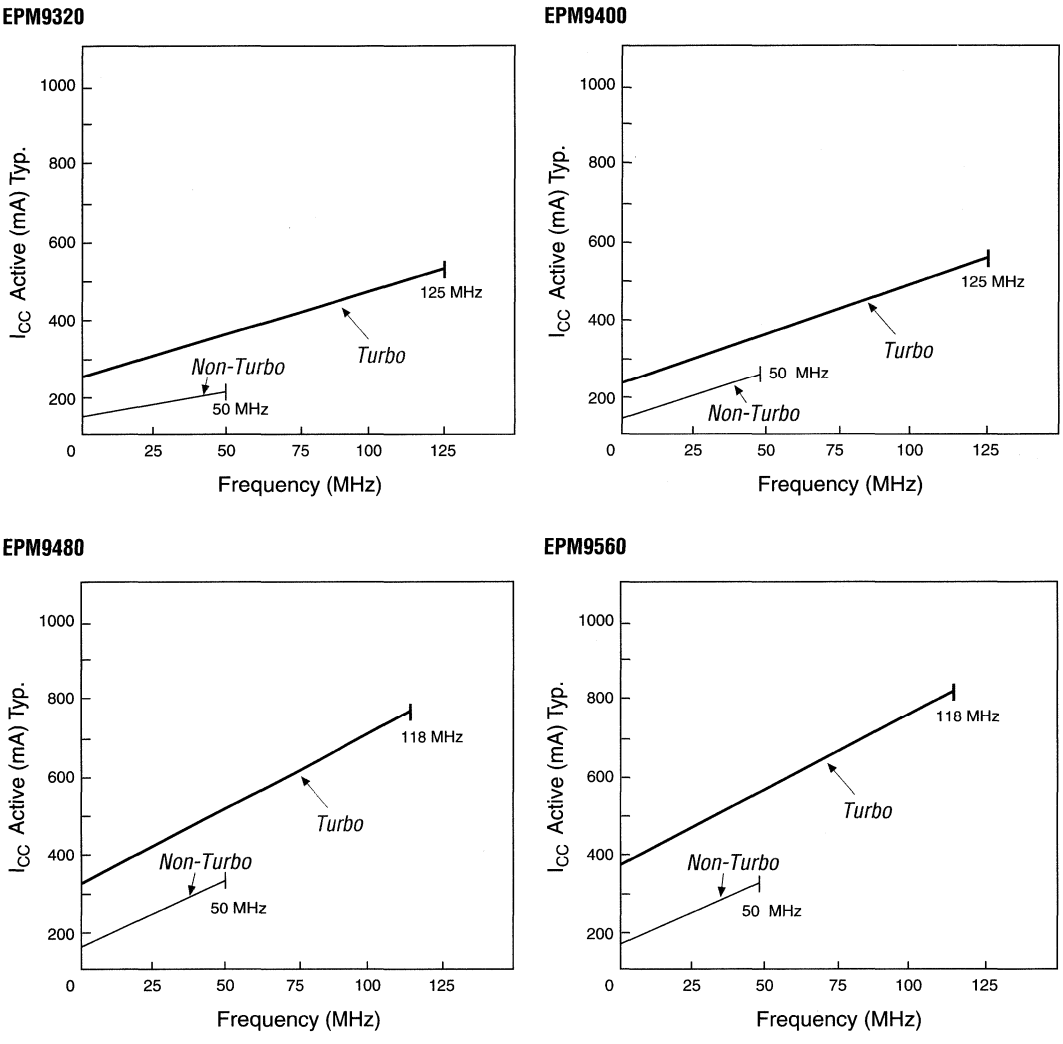
Device	Constant A	Constant B	Constant C
EPM9320	0.81	0.33	0.056
EPM9400 *(1)*	0.60	0.33	0.053
EPM9480	0.68	0.29	0.064
EPM9560	0.68	0.26	0.052

Note:
(1) This information is preliminary.

This calculation provides an I_{CC} estimate based on typical conditions with no output load, using a typical pattern of a 16-bit, loadable, enabled up/down counter in each LAB. Actual I_{CC} should be verified during operation, because the measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 14 shows typical supply current versus frequency for MAX 9000 devices.

Figure 14. I_{CC} vs. Frequency for MAX 9000 Devices



Device Pin-Outs

Tables 8, 9, 10, and 11 show the pin names and numbers for the dedicated pins in each EPM9320, EPM9400, EPM9480, and EPM9560 package, respectively.

Table 8. EPM9320 Dedicated Pin-Outs

Pin Name	84-Pin PLCC *(1)*	208-Pin RQFP	280-Pin PGA
DIN1 (GCLK1)	1	182	V10
DIN2 (GCLK2)	84	183	U10
DIN3 (GCLR)	13	153	V17
DIN4 (GOE)	72	4	W2
TCK	43	78	A9
TMS	55	49	D6
TDI	42	79	C11
TDO	30	108	A18
GND	6, 18, 24, 25, 48, 61, 67, 70	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16
VCCINT (5.0 V only)	14, 21, 28, 57, 64, 71	10, 19, 30, 45, 112, 128, 139, 148	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14
VCCIO (3.3 or 5.0 V)	15, 37, 60, 79	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15
No Connect (N.C.)	29	6, 7, 8, 9, 11, 12, 13, 15, 16, 17, 18, 109, 140, 141, 142, 144, 145, 146, 147, 149, 150, 151	B6, K19, L2, L4, L18, L19, M1, M2, M3, M4, M16, M17, M18, M19, N1, N2, N3, N4, N16, N17, N18, N19, P1, P2, P3, P17, P18, P19, R1, R2, R3, R17, R18, R19, T1, T2, T3, T17, T18, T19, U1, U2, U3, U17, U18, U19, V1, V2, V19, W1
VPP, *Note (2)*	56	48	C4

Notes:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* in this data book for more information.

(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

Table 9. EPM9400 Dedicated Pin-Outs

Pin Name	84-Pin PLCC *(1)*	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	2	182	210
DIN2 (GCLK2)	1	183	211
DIN3 (GCLR)	12	153	187
DIN4 (GOE)	74	4	234
TCK	43	78	91
TMS	54	49	68
TDI	42	79	92
TDO	31	108	114
GND	6, 13, 20, 26, 27, 47, 60, 66, 69, 73	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	16, 23, 30, 56, 63, 70	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	17, 37, 59, 80	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	–	6, 7, 8, 9, 11, 12, 13, 109, 144, 145, 146, 147, 149, 150, 151	1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 168, 169, 170, 171, 172, 173, 174, 175, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP, *Note (2)*	55	48	67

Notes:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* in this data book for more information.

(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

Table 10. EPM9480 Dedicated Pin-Outs

Pin Name	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	182	210
DIN2 (GCLK2)	183	211
DIN3 (GCLR)	153	187
DIN4 (GOE)	4	234
TCK	78	91
TMS	49	68
TDI	79	92
TDO	108	114
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	6, 7, 8, 9, 109, 149, 150, 151	1, 2, 3, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP, *Note (1)*	48	67

Note:

(1) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

Table 11. EPM9560 Dedicated Pin-Outs

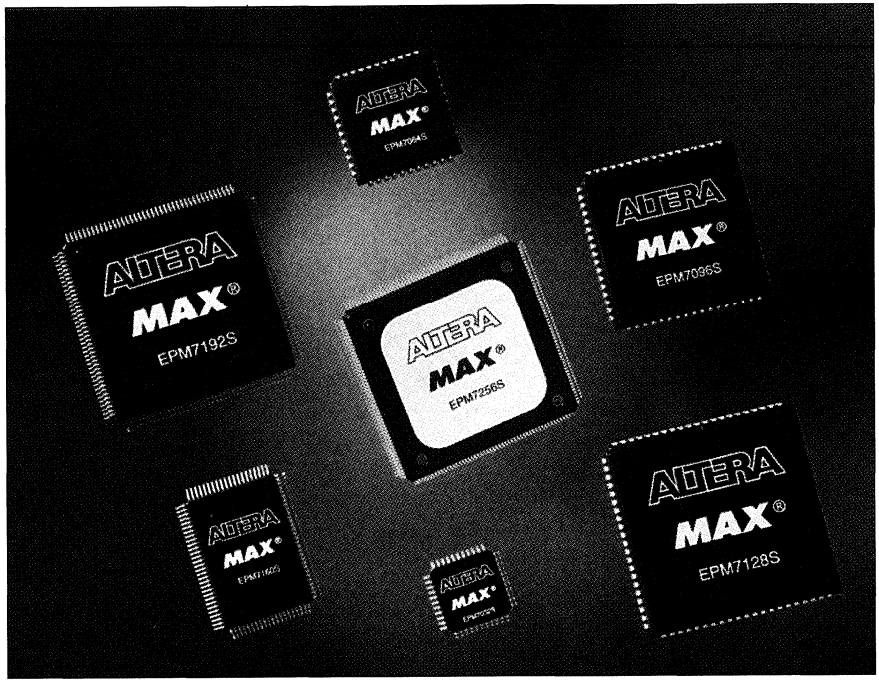
Pin Name	208-Pin CQFP	240-Pin RQFP	280-Pin PGA	304-Pin RQFP
DIN1 (GCLK1)	182	210	V10	266
DIN2 (GCLK2)	183	211	U10	267
DIN3 (GCLR)	153	187	V17	237
DIN4 (GOE)	4	234	W2	296
TCK	78	91	A9	114
TMS	49	68	D6	85
TDI	79	92	C11	115
TDO	108	114	A18	144
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16	13, 22, 33, 42, 53, 62, 73, 74, 102, 121, 138, 155, 166, 167, 186, 187, 206, 207, 226, 254, 273, 290
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	12, 32, 52, 72, 157, 177, 197, 217
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	3, 23, 43, 63, 91, 108, 127, 156, 176, 196, 216, 243, 260, 279
No Connect (N.C.)	109	–	B6, W1	1, 2, 76, 77, 78, 79, 80, 81, 82, 83, 84, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 297, 298, 299, 300, 301, 302, 303, 304
VPP, *Note (1)*	48	67	C4	75

Note:

(1) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

June 1996

MAX 7000 Programmable Logic Device Family Data Sheet


ALTERA
MAX®
EPM7064S
EPM7192S
EPM7096S
EPM7256S
EPM7128S

MAX 7000

Programmable Logic Device Family

Includes MAX 7000E & MAX 7000S

June 1996, ver. 4 — Data Sheet

Features...

- High-performance, EEPROM-based programmable logic devices (PLDs) based on second-generation Multiple Array MatriX (MAX) architecture
- In-system programmability (ISP) via standard Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990) available in MAX 7000S devices
- Built-in JTAG boundary-scan test (BST) circuitry in MAX 7000S devices with 128 or more macrocells
- Complete EPLD family with logic densities ranging from 600 to 5,000 usable gates (see Table 1)
- 5-ns pin-to-pin logic delays with up to 178.6-MHz counter frequencies (including interconnect)
- PCI-compliant devices available
- ClockBoost option for clock multiplication
- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls

Table 1. MAX 7000 Device Features *Note (1)*

Feature	EPM7032 EPM7032V EPM7032S	EPM7064 EPM7064S	EPM7096 EPM7096S	EPM7128E EPM7128S EPM7128SV	EPM7160E EPM7160S	EPM7192E EPM7192S	EPM7256E EPM7256S
Usable gates	600	1,250	1,800	2,500	3,200	3,750	5,000
Macrocells	32	64	96	128	160	192	256
Logic array blocks	2	4	6	8	10	12	16
Max. user I/O pins	36	68	76	100	104	124	164
t_{PD} (ns)	5 (12)	5	6	6 (10)	6	7.5	7.5
t_{SU} (ns)	4 (10)	4	5	5 (7)	5	6	6
t_{FSU} (ns)	2.5 (–)	2.5	2.5	2.5 (3)	2.5	3	3
t_{CO1} (ns)	3.5 (7)	3.5	4	4 (5)	4	4.5	4.5
f_{CNT} (MHz)	178.6 (90.9)	178.6	151.5	151.5 (100)	151.5	125	125

Notes:
(1) Values in parentheses are for 3.3-V devices.

...and More Features

- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in J-lead (PLCC), pin-grid array (PGA), quad flat pack (QFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
  - Full 3.3-V EPM7032V and EPM7128SV
  - 3.3-V or 5.0-V I/O pins on all devices (except 44-pin packages)
- Enhanced features available in MAX 7000E and MAX 7000S devices
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS II development system on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar Logic, VeriBest, Mentor Graphics, OrCAD, Synopsys, and Viewlogic
- Programming support with Altera's Master Programming Unit (MPU) and BitBlaster serial download cable, as well as programming hardware from other manufacturers

General Description

The MAX 7000 family of high-density, high-performance programmable logic devices is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 178.6 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, -12P speed grades comply with the *PCI Local Bus Specification*, version 2. See Table 2 for available speed grades.

Table 2. MAX 7000 Speed Grades

Device	Speed Grade									
	-5	-6	-7	-10P	-10	-12P	-12	-15	-15T	-20
EPM7032	✓ (1)	✓	✓		✓		✓	✓	✓	
EPM7032V							✓	✓		✓
EPM7032S	✓ (1)	✓ (1)	✓ (1)		✓ (1)			✓ (1)		
EPM7064		✓ (1)	✓		✓		✓	✓		
EPM7064S		✓ (1)	✓ (1)		✓ (1)			✓ (1)		
EPM7096		✓ (1)	✓		✓		✓	✓		
EPM7096S		✓ (1)	✓ (1)		✓ (1)			✓ (1)		
EPM7128E		✓ (1)	✓ (1)	✓	✓		✓	✓		✓
EPM7128S		✓ (1)	✓ (1)		✓ (1)			✓ (1)		
EPM7128SV					✓ (1)			✓ (1)		
EPM7160E			✓ (1)	✓	✓		✓	✓		✓
EPM7160S			✓ (1)		✓ (1)			✓ (1)		
EPM7192E			✓ (1)	✓ (1)	✓ (1)	✓	✓	✓		✓
EPM7192S			✓ (1)		✓ (1)			✓ (1)		
EPM7256E			✓ (1)		✓ (1)	✓	✓	✓		✓
EPM7256S			✓ (1)		✓ (1)			✓ (1)		

Note:
(1) This information is preliminary. Contact Altera Customer Marketing at (408) 894-7104 for product availability.

The higher-density members of the MAX 7000 family—called MAX 7000E devices—include the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices. These devices have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In system programmable versions of the MAX 7000 family—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7096S, EPM7128S, EPM7128SV, EPM7160S, EPM7192S and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as ISP, JTAG boundary-scan test (BST) circuitry in devices with 128 or more macrocells, and an open-drain output option. See Table 3.

Table 3. MAX 7000 Device Features

Feature	EPM7032 EPM7032V EPM7064 EPM7096	All MAX 7000E Devices	All MAX 7000S Devices
ISP via JTAG interface			✓
JTAG BST circuitry			✓ *(1)*
ClockBoost clock multiplier versions available			✓ *(2)*
Open-drain output option			✓
Fast input registers		✓	✓
Six global output enables		✓	✓
Two global clocks		✓	✓
Slew-rate control		✓	✓
3.3-V I/O option	✓	✓	✓
Programmable register	✓	✓	✓
Parallel expanders	✓	✓	✓
Shared expanders	✓	✓	✓
Power-saving mode	✓	✓	✓
Security bit	✓	✓	✓
PCI-compliant versions available	✓	✓	✓

Notes:
(1) Available in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
(2) Information on ClockBoost clock multiplier circuitry is preliminary. Contact your local Altera representative for more information.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple PLDs ranging from PALs, GALs, and 22V10s to MACH, pLSI, and FPGA devices. With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 7000 devices are also ideal for gate-array prototyping. MAX 7000 devices are available in a wide range of packages, including plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1-mm thin quad flat pack (TQFP) packages. See Table 4.

Table 4. MAX 7000 Maximum User I/O Pins *Notes (1), (2), (3)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin RQFP
EPM7032	36	36	36								
EPM7032V	36		36								
EPM7032S	36		36								
EPM7064	36		36	52	68	68					
EPM7064S	36		36	52	68	68					
EPM7096				52	64	76					
EPM7096S				52	64	76	76				
EPM7128E					68	84		100			
EPM7128S					68	84	84, *(4)*	100			
EPM7128SV					68	84	84, *(4)*	100			
EPM7160E					64	84		104			
EPM7160S					64	84	84, *(4)*	104			
EPM7192E								124	124		
EPM7192S								124			
EPM7256E								132, *(4)*		164	164
EPM7256S								132, *(4)*			164

Notes:

(1) Contact Altera for up-to-date information on available device package options.
(2) For the MAX 7000S JTAG interface, four I/O pins become JTAG pins.
(3) Information on MAX 7000S devices is preliminary.
(4) Perform a complete thermal analysis before committing a design to this device package. See *Operating Requirements for Altera Devices Data Sheet* in this data book for more information.

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased over 100 times.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

For more information on development tools, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of the EPM7032, EPM7032V, EPM7064, and EPM7096 devices.

Figure 1. EPM7032, EPM7032V, EPM7064 & EPM7096 Device Block Diagram

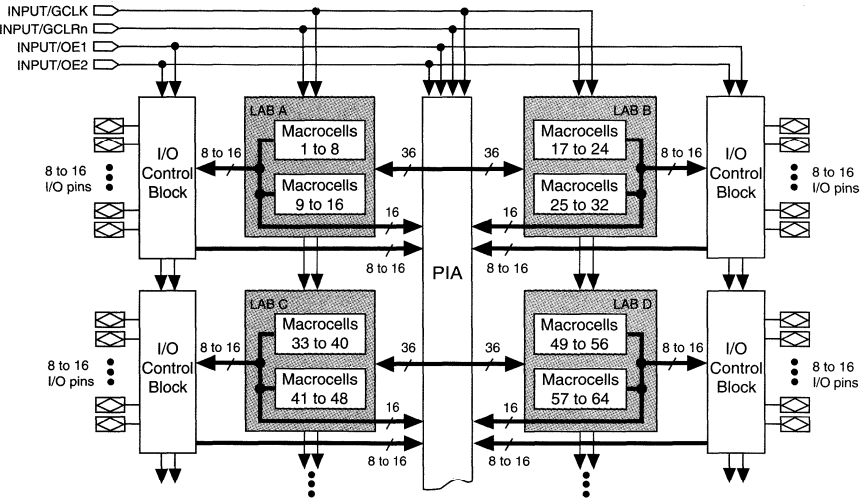
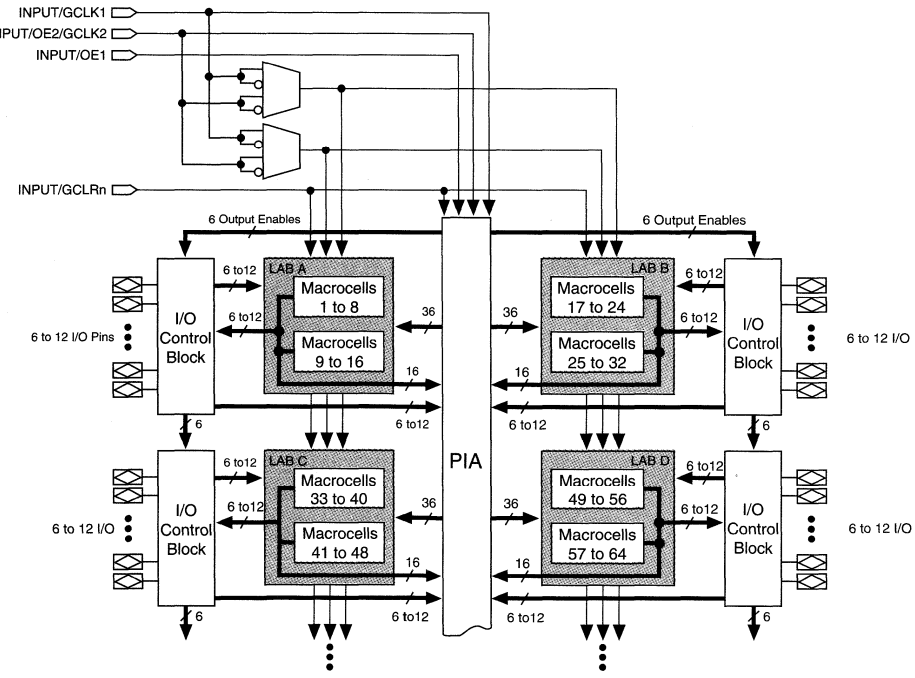


Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

Figure 2. MAX 7000E & MAX 7000S Device Block Diagram



Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

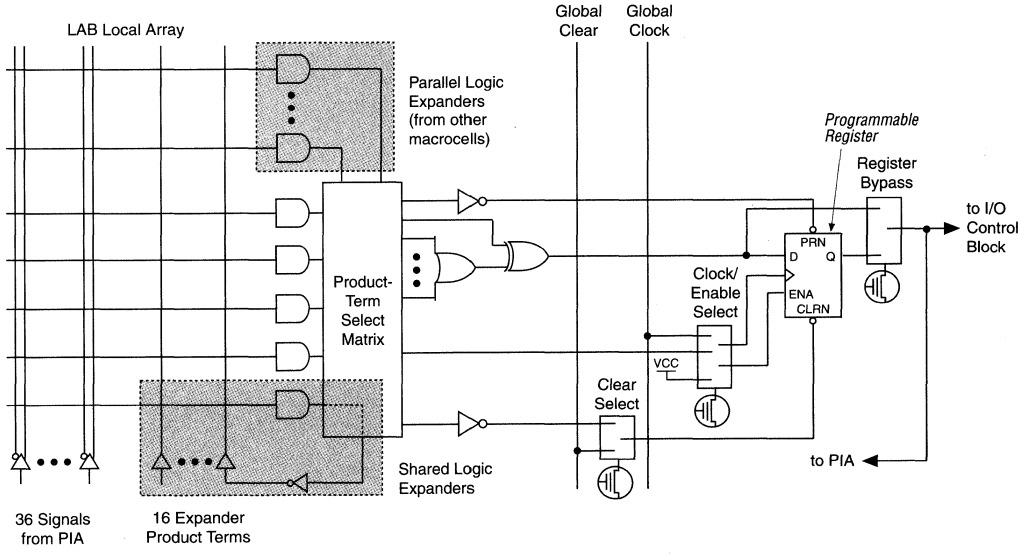
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

Macrocells

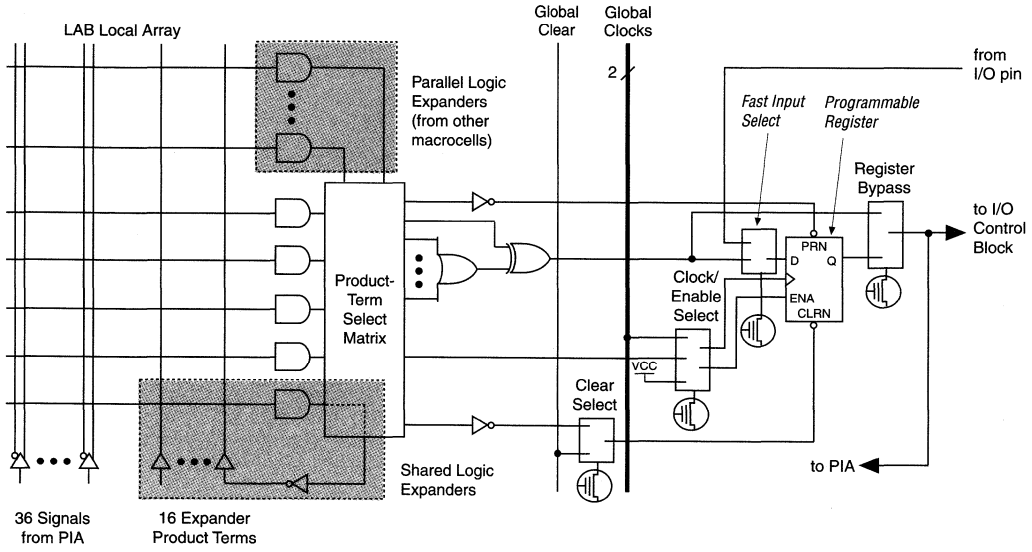
The MAX 7000 macrocell can be individually configured for both sequential and combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7032V, EPM7064, and EPM7096 devices is shown in Figure 3.

Figure 3. EPM7032, EPM7032V, EPM7064 & EPM7096 Device Macrocell



The macrocell of MAX 7000E and MAX 7000S devices is shown in Figure 4.

Figure 4. MAX 7000E & MAX 7000S Device Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

MAX+PLUS II automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; MAX+PLUS II then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In the EPM7032, EPM7032V, EPM7064, and EPM7096 devices, the global clock signal is available from a dedicated clock pin, GCLK, as shown in Figure 1. In MAX 7000E and MAX 7000S devices, two global clock signals are available. As shown in Figure 2, these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figures 3 and 4, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn).

All MAX 7000E and MAX 7000S I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (3-ns) input setup time.

Expander Product Terms

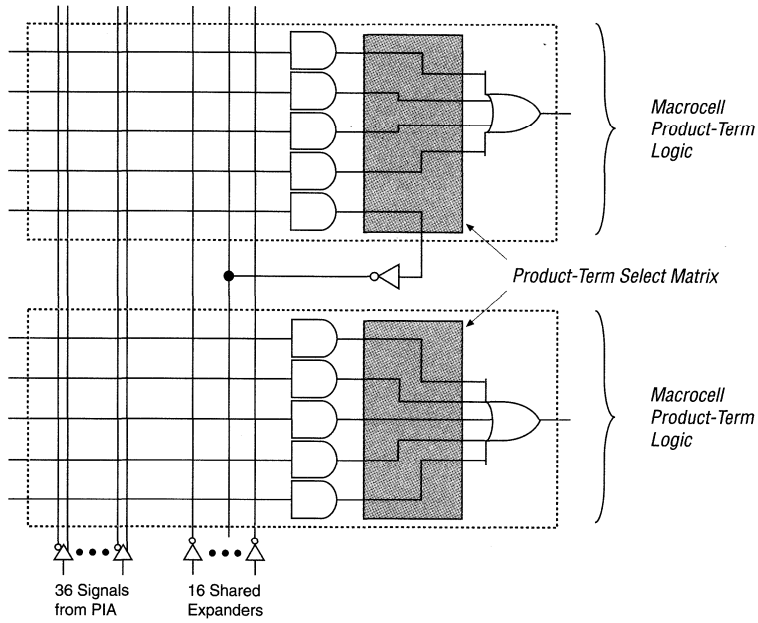
Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000 architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

Figure 5. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

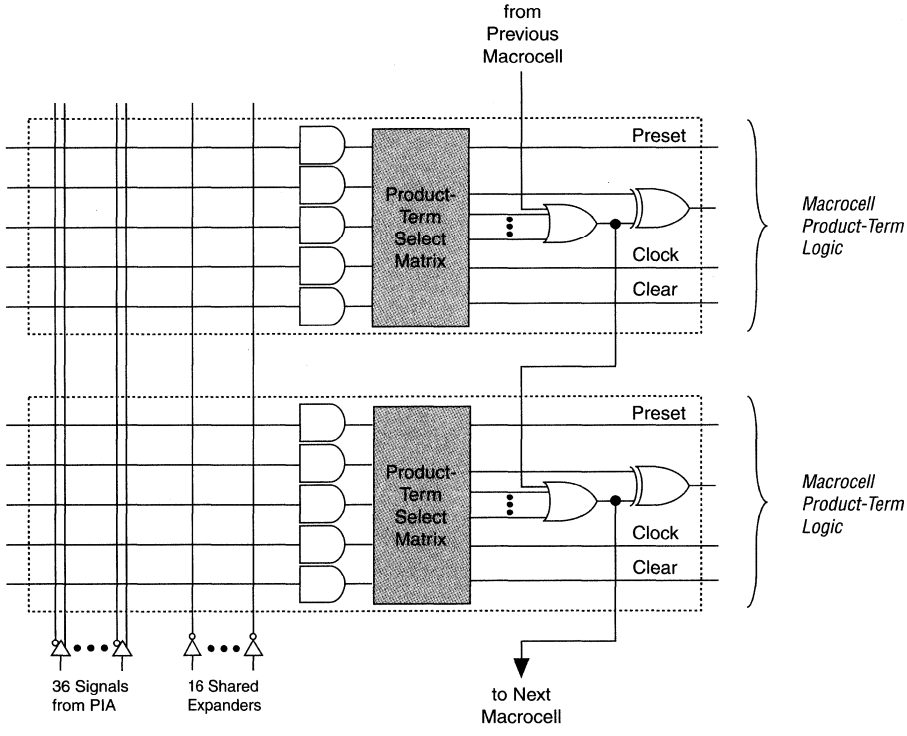
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with 5 product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The MAX+PLUS II Compiler can automatically allocate up to 3 sets of up to 5 parallel expanders to the macrocells that require additional product terms. Each set of 5 parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 6. Parallel Expanders

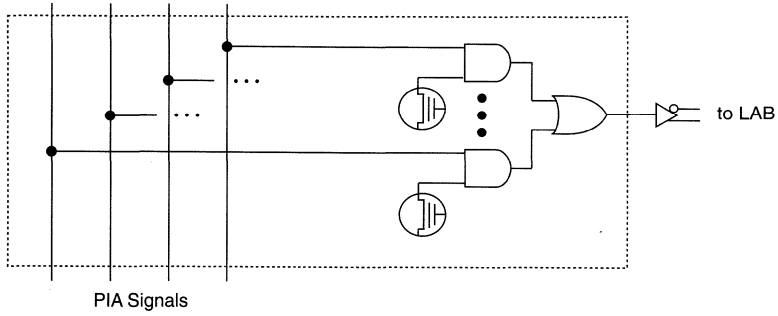
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 7. PIA Routing



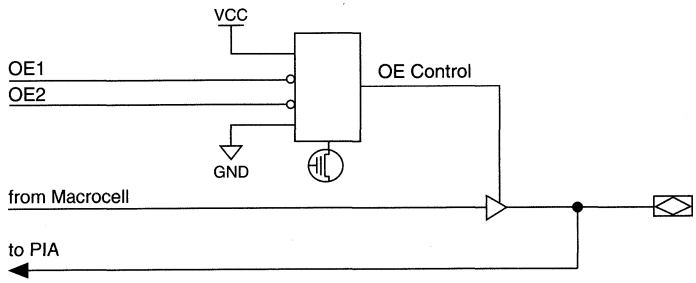
While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

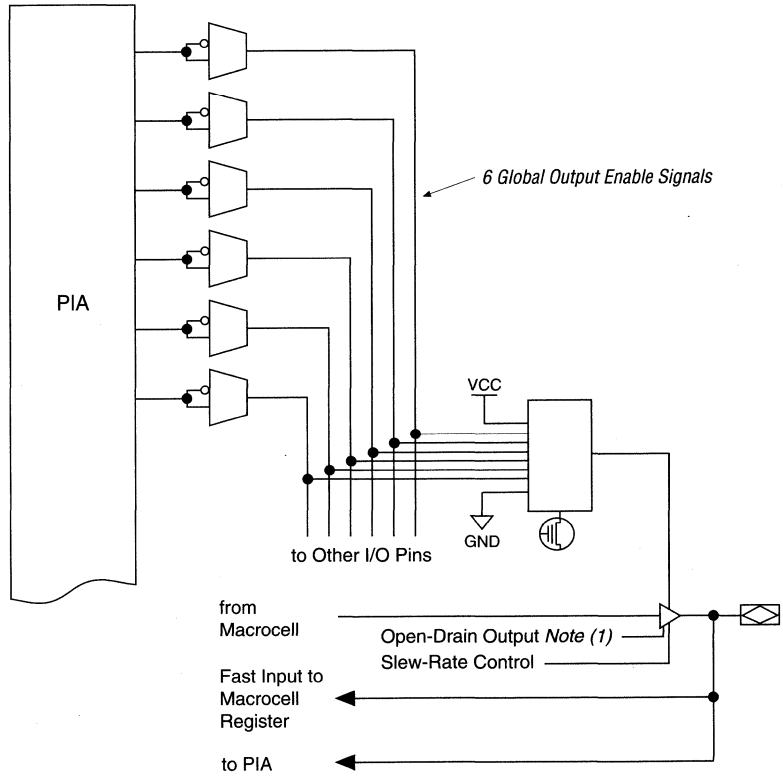
The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to GND or VCC. Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7032V, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 8. I/O Control Block of MAX 7000 Devices

EPM7032, EPM7032V, EPM7064 & EPM7096 Devices



MAX 7000E & MAX 7000S Devices



Note:
(1) The open-drain output option is available in MAX 7000S devices only.

When the tri-state buffer control is connected to GND, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to VCC, the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std 1149.1-1990). ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the 12.0-V programming voltage required to program EEPROM cells, eliminating the need for an external 12.0-V power supply to program the devices on the board. During ISP, the I/O pins are tri-stated to eliminate board conflicts.

ISP simplifies the manufacturing flow by allowing the devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via automatic test equipment, embedded processors, or the Altera BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000S devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

Go to *Application Brief 145 (Designing for In-System Programmability in MAX 7000S Devices)* for more information.

ClockBoost

To support high-speed designs, specially marked MAX 7000S devices offer optional ClockBoost circuitry. This circuit is a phase-locked loop (PLL) and can be used to increase design speed and reduce resource usage. With the ClockBoost circuitry, which provides a clock multiplier, designers can easily implement time-domain-multiplexed logic to reduce resource usage in a design.

Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (Turbo Bit on) or low-power (Turbo Bit off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters.

Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

3.3-V or 5.0-V I/O Operation

All MAX 7000 devices, except 44-pin devices, can be set for 3.3-V or 5.0-V I/O operation. These devices have two sets of V_{CC} pins: one set for internal operation and input buffers (V_{CCINT}) and another set for I/O output drivers (V_{CCIO}).

V_{CCINT} pins must always be connected to a 5.0-V power supply. With this V_{CCINT} level, input voltages are at TTL levels, and are compatible with both 3.3-V and 5.0-V inputs. V_{CCIO} pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When V_{CCIO} pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When they are connected to a 3.3-V supply, the output high is 3.3 V and is compatible with both 3.3-V and 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominal timing delay adder to the output buffer timing parameter (t_{OD}).

Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (or equivalent open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

Programming with External Hardware

MAX 7000 devices can be programmed on 486- and Pentium-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. For more information, see *Altera Programming Hardware* in this data book.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation.

Data I/O and other programming hardware manufacturers also provide programming support for Altera devices. See *Programming Hardware Manufacturers* in this data book for more information.

JTAG Operation

MAX 7000S devices support JTAG BST circuitry as specified by IEEE Std 1149.1-1990. The EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices support the following four JTAG modes: SAMPLE/PRELOAD, EXTEST, BYPASS, and IDCODE. The EPM7032S, EPM7064S, and EPM7096S devices support the IDCODE mode; these devices also support the BYPASS mode to ensure that JTAG chains are not interrupted. The pin-out tables starting on page 237 of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Go to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)* for more information.

Design Security

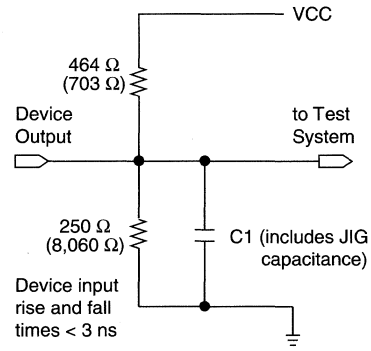
All MAX 7000 devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000 devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9. Test patterns can be used and then erased during early stages of the production flow.

Figure 9. MAX 7000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices.



QFP Carrier & Development Socket

MAX 7000 and MAX 7000E devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the fragile QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress. For detailed information and carrier dimensions, refer to the *QFP Carrier & Development Socket Data Sheet* in this data book.

☞ MAX 7000S devices are not shipped in carriers.

MAX 7000 5.0-V Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (3)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		Plastic and power quad flat pack packages, under bias		135	° C

MAX 7000 5.0-V Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (4), (5)*	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers, 5.0-V operation	*Notes (4), (5)*	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers, 3.3-V operation	*Notes (5), (6)*	3.00	3.60	V
V_{CCISP}	Supply voltage during ISP	*Note (7)*	4.75	5.25	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

MAX 7000 5.0-V Device DC Operating Conditions *Notes (2), (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V, *Note (9)*	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.0 V, *Note (9)*	2.4		V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V, *Note (10)*		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.0 V, *Note (10)*		0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40	40	µA

MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 *Note (11)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

MAX 7000 5.0-V Device Capacitance: MAX 7000E *Note (11)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

MAX 7000 5.0-V Device Capacitance: MAX 7000S *Notes (2), (11), (12)*

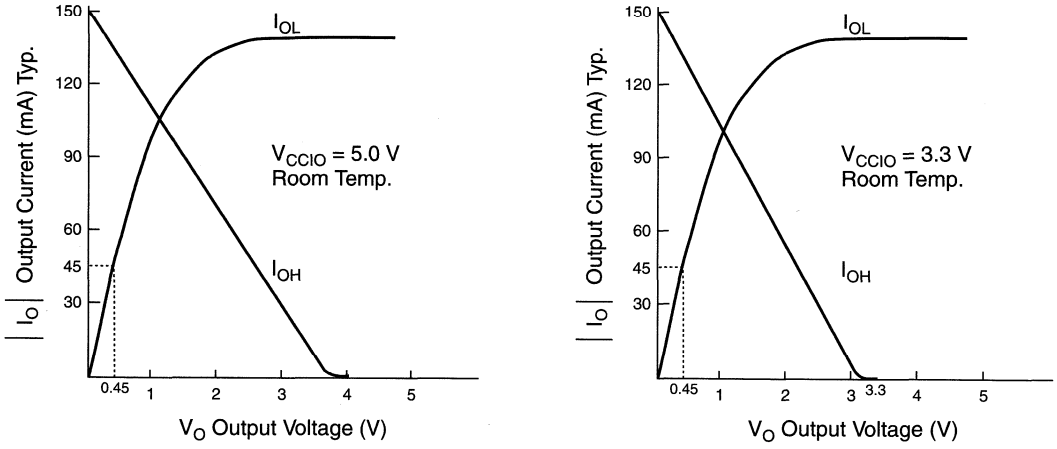
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Information on MAX 7000S devices is preliminary.
(3) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(4) Numbers in parentheses are for industrial-temperature-range versions.
(5) V_{CC} must rise monotonically.
(6) 3.3-V I/O operation is not available for 44-pin packages.
(7) The V_{CCISP} parameter applies only to MAX 7000S devices.
(8) Operating conditions: V_{CCINT} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
(9) The I_{OH} parameter refers to high-level TTL output current.
(10) The I_{OL} parameter refers to low-level TTL output current.
(11) Capacitance is measured at 25° C and is sample-tested only. The `OE1` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(12) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically –60 µA.

Figure 10 shows the typical output drive characteristics of MAX 7000 devices.

Figure 10. Output Drive Characteristics of 5.0-V MAX 7000 Devices



3.3-V EPM7032V

The EPM7032V device is a high-performance MAX 7000 device that meets the low power and voltage requirements of 3.3-V applications ranging from notebook computers to battery-operated, hand-held equipment. The EPM7032V provides in-system speeds of up to 90.9 MHz and propagation delays of 12 ns. It is available in 44-pin reprogrammable PLCC or TQFP packages and can accommodate designs with up to 36 inputs and 32 outputs.

Power Management

The 3.3-V operation of the EPM7032V offers power savings of 30% to 50% over the 5.0-V operation of the EPM7032. Power-saving features of the EPM7032V include the programmable speed/power control as specified for non-3.3-V MAX 7000 devices and a power-down mode.

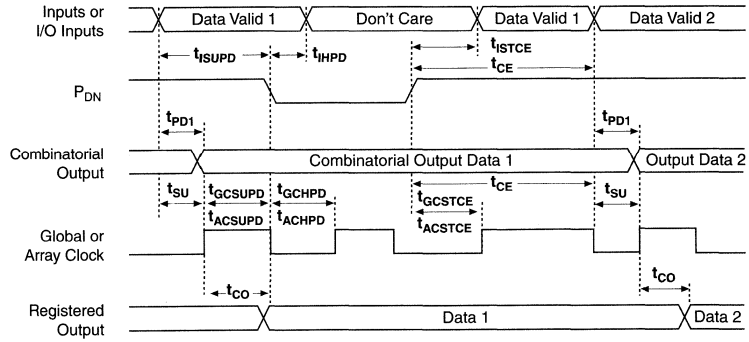
Power-Down Mode

The EPM7032V device provides a unique power-down mode that allows the device to consume near-zero power (typically 50 µA). The power-down mode is controlled externally by the dedicated power-down pin (PDn). When PDn is asserted (active low), the power-down sequence latches all input pins, internal logic, and output pins of the EPM7032V device, preserving their present state. Output pins maintain their present low, high, or tri-state value while in power-down mode.

Once in power-down mode, any or all of the inputs, including clocks, can be toggled without affecting the state of the device. Because internal latches are used to ensure that the proper state exists during power-down mode, the external inputs and clocks must meet certain setup and hold time requirements. See Figure 11 and the "Power-Down Timing Parameters" and "Chip-Enable Timing Parameters" tables on page 231 of this data sheet.

Figure 11. Power-Down Mode Switching Waveforms

The switching waveforms for the EPM7032V are identical to those of the 5.0-V EPM7032 in all modes, except for the additional power-down mode shown here. t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



When the PDn signal is brought high, the device is enabled and the combinatorial outputs respond to the present input conditions within the specified chip enable delay (t_{CE}). Registered outputs respond to clock transitions within t_{CE}. Clocking the device during the chip enable sequence can cause the data to change inside the chip if a clock transition occurs during certain intervals of the chip enable or chip disable sequences. All clocks should be gated to prevent clock transitions during the clock setup time (t_{GCSUPD} or t_{ACSUPD}) and during the chip enable setup time (t_{GCSTCE} or t_{ACSTCE}), as shown in Figure 11.

All registers in the EPM7032V provide clock enable control, which makes it easy to disable clocks. If output signals must be frozen in a high-impedance state during power-down, the associated output enable signal must be asserted, the system clock must be removed, and the PDn pin must be asserted. To reactivate the device, the sequence is reversed. For some systems, it may be more appropriate to switch the order of the clock and output enable controls.

All power-down/chip-enable timing parameters are computed from external input or I/O pins, with the macrocell Turbo Bit turned on, and without the use of parallel expanders. For macrocells in low-power mode (Turbo Bit off), the low-power adder, t_{LPA}, must be added to the power-down/chip enable timing parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH}, and t_{SEXP}. For macrocells that use shared or parallel expanders, t_{SEXP} or t_{PEXP} must be added. For data or clock paths that use more than one logic array delay, the worst-case data or clock delay must be added to the respective power-down/chip-enable parameters. Actual worst-case timing of data and clock paths can be calculated with the MAX+PLUS II Simulator or Timing Analyzer, or with other industry-standard EDA verification tools.

MAX 7000 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (2)*	–2.0	5.6	V
V_I	DC input voltage	With respect to GND, *Note (2)*	–2.0	5.6	V
I_{OUT}	DC output current per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		135	° C
P_D	Power dissipation			1,000	mW
I_{MAX}	DC V_{CC} or GND current			300	mA

MAX 7000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (3)*	3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

MAX 7000 3.3-V Device DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –0.1 mA DC, *Note (6)*	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (7)*			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10		10	µA
I_{CC0}	V_{CC} supply current (standby, power-down mode)	*Note (8)*		2	150	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, no load, *Note (8)*		10	20	mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, no load, f = 1.0 MHz, *Note (8)*		15	25	mA

MAX 7000 3.3-V Device Capacitance *Note (9)*

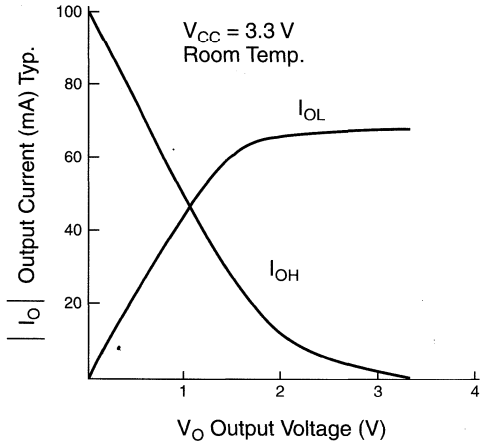
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to V_{CC} + 2.0 V for periods shorter than 20 ns under no-load conditions.
(3) V_{CC} must rise monotonically.
(4) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(5) Operating conditions: V_{CC} = 3.3 V ± 10%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 3.3 V ± 10%, T_A = –40° C to 85° C for industrial use.
(6) The I_{OH} parameter refers to high-level TTL output current.
(7) The I_{OL} parameter refers to low-level TTL output current.
(8) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.
(9) Capacitance is measured at 25° C and is sample-tested only. The `OE1` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

Figure 12 shows the typical output drive characteristics of the EPM7032V.

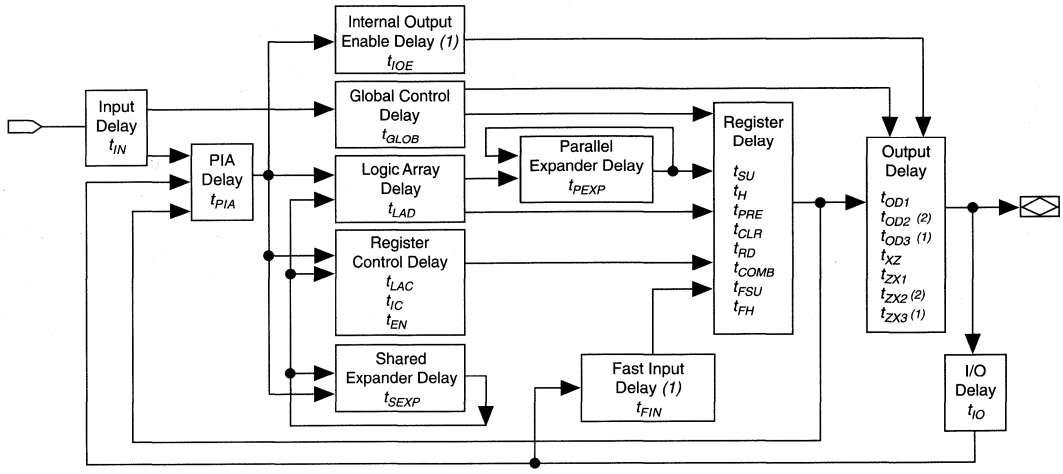
Figure 12. EPM7032V Output Drive Characteristics



Timing Model

MAX 7000 device timing can be analyzed with the MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 13. MAX 7000 Timing Model



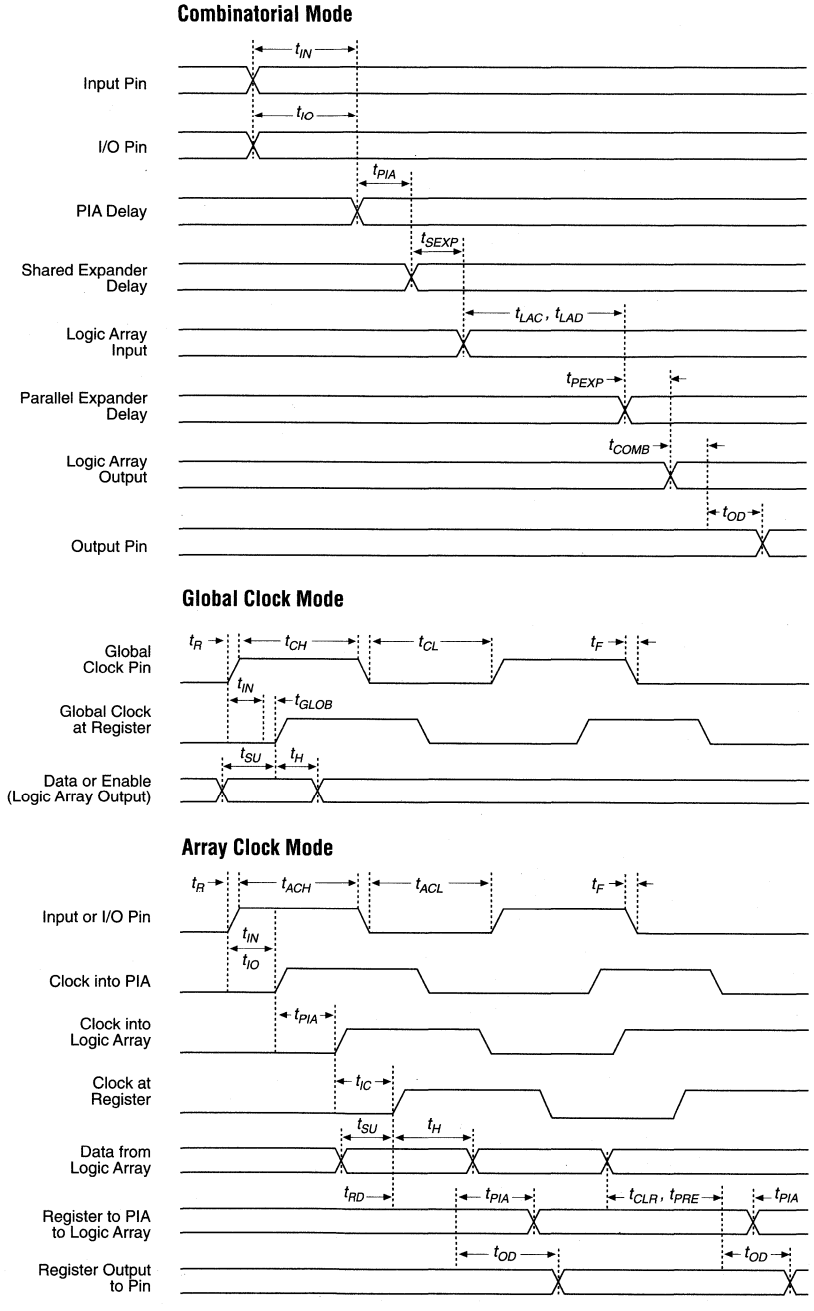
Notes:
(1) Not available in 44-pin devices.
(2) Only available in MAX 7000E and MAX 7000S devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the internal timing relationship of internal and external delay parameters.

See *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book for more information.

Figure 14. Switching Waveforms

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



MAX 7000 AC Operating Conditions *Notes (1), (2)*

External Timing Parameters			Speed Grade						
			-5		-6		-7		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		5		6		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		5		6		7.5	ns
t_{SU}	Global clock setup time		4		5		6		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{FSU}	Global clock setup time of fast input	*Note (3)*	–		–		3		ns
t_{FH}	Global clock hold time of fast input	*Note (3)*	–		–		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		3.5		4		4.5	ns
t_{CH}	Global clock high time		2		2.5		3		ns
t_{CL}	Global clock low time		2		2.5		3		ns
t_{ASU}	Array clock setup time		2		2.5		3		ns
t_{AH}	Array clock hold time		2		2		2		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		5.5		6.5		7.5	ns
t_{ACH}	Array clock high time		2.5		3		3		ns
t_{ACL}	Array clock low time		2.5		3		3		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (4)*	1		1		1		ns
t_{CNT}	Minimum global clock period			5.6		6.6		8	ns
f_{CNT}	Maximum internal global clock frequency	*Note (5)*	178.6		151.5		125		MHz
t_{ACNT}	Minimum array clock period			5.6		6.6		8	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (5)*	178.6		151.5		125		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	250		200		166.7		MHz

Internal Timing Parameters			Speed Grade						
			-5		-6		-7		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			0.4		0.4		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.4		0.5	ns
t_{FIN}	Fast input delay	*Note (3)*						1	ns
t_{SEXP}	Shared expander delay			3		3.5		4	ns
t_{PEXP}	Parallel expander delay			0.8		0.8		0.8	ns
t_{LAD}	Logic array delay			1.5		2		3	ns
t_{LAC}	Logic control array delay			1.5		2		3	ns
t_{IOE}	Internal output enable delay	*Note (3)*						2	ns
t_{OD1}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF *Note (1)*		1.5		2		2	ns
t_{OD2}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *Note (7)*		2.0		2.5		2.5	ns
t_{OD3}	Output buffer & pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF Notes *(1), (3), (7)*		6.5		7		7	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF *Note (7)*		4		4		4	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *Note (7)*		–		4.5		4.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *Note (7)*		–		–		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4		4		4	ns
t_{SU}	Register setup time		2.5		3		3		ns
t_{H}	Register hold time		1.5		1.5		2		ns
t_{FSU}	Register setup time of fast input	*Note (3)*					3		ns
t_{FH}	Register hold time of fast input	*Note (3)*					0.5		ns
t_{RD}	Register delay			0.8		0.8		1	ns
t_{COMB}	Combinatorial delay			0.8		0.8		1	ns
t_{IC}	Array clock delay			2		2.5		3	ns
t_{EN}	Register enable time			1.5		2		3	ns
t_{GLOB}	Global control delay			0.8		0.8		1	ns
t_{PRE}	Register preset time			2		2		2	ns
t_{CLR}	Register clear time			2		2		2	ns
t_{PIA}	PIA delay			0.8		0.8		1	ns
t_{LPA}	Low-power adder	*Note (8)*		8		10		10	ns

External Timing Parameters			Speed Grade				
			MAX 7000E (-10P) MAX 7000S (-10)		MAX 7000 (-10) MAX 7000E (-10)		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		10	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		10		10	ns
t_{SU}	Global clock setup time		7		8		ns
t_{H}	Global clock hold time		0		0		ns
t_{FSU}	Global clock setup time of fast input	*Note (3)*	3		3		ns
t_{FH}	Global clock hold time of fast input	*Note (3)*	0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5		5	ns
t_{CH}	Global clock high time		4		4		ns
t_{CL}	Global clock low time		4		4		ns
t_{ASU}	Array clock setup time		2		3		ns
t_{AH}	Array clock hold time		3		3		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10		10	ns
t_{ACH}	Array clock high time		4		4		ns
t_{ACL}	Array clock low time		4		4		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (4)*	1		1		ns
t_{CNT}	Minimum global clock period			10		10	ns
f_{CNT}	Maximum internal global clock frequency	*Note (8)*	100		100		MHz
t_{ACNT}	Minimum array clock period			10		10	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (8)*	100		100		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	125		125		MHz

Internal Timing Parameters			Speed Grade				
			MAX 7000E (-10P) MAX 7000S (-10)		MAX 7000 (-10) MAX 7000E (-10)		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			0.5		1	ns
t_{IO}	I/O input pad and buffer delay			0.5		1	ns
t_{FIN}	Fast input delay	*Note (3)*		1		1	ns
t_{SEXP}	Shared expander delay			5		5	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			5		5	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{IOE}	Internal output enable delay	*Note (3)*		2		2	ns
t_{OD1}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF, *Note (1)*		1.5		2	ns
t_{OD2}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (7)*		2		2.5	ns
t_{OD3}	Output buffer & pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF, *Notes (1), (3), (7)*		5.5		6	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF, *Note (7)*		5		5	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (7)*		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF, *Note (7)*		9		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		2		3		ns
t_{H}	Register hold time		3		3		ns
t_{FSU}	Register setup time of fast input	*Note (3)*	3		3		ns
t_{FH}	Register hold time of fast input	*Note (3)*	0.5		0.5		ns
t_{RD}	Register delay			2		1	ns
t_{COMB}	Combinatorial delay			2		1	ns
t_{IC}	Array clock delay			5		5	ns
t_{EN}	Register enable time			5		5	ns
t_{GLOB}	Global control delay			1		1	ns
t_{PRE}	Register preset time			3		3	ns
t_{CLR}	Register clear time			3		3	ns
t_{PIA}	PIA delay			1		1	ns
t_{LPA}	Low-power adder	*Note (8)*		11		11	ns

External Timing Parameters			Speed Grade				
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		12	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		12		12	ns
t_{SU}	Global clock setup time		7		10		ns
t_{H}	Global clock hold time		0		0		ns
t_{FSU}	Global clock setup time of fast input	*Note (3)*	3		3		ns
t_{FH}	Global clock hold time of fast input	*Note (3)*	1		1		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6		6	ns
t_{CH}	Global clock high time		4		4		ns
t_{CL}	Global clock low time		4		4		ns
t_{ASU}	Array clock setup time		3		4		ns
t_{AH}	Array clock hold time		4		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12		12	ns
t_{ACH}	Array clock high time		5		5		ns
t_{ACL}	Array clock low time		5		5		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (4)*	1		1		ns
t_{CNT}	Minimum global clock period			11		11	ns
f_{CNT}	Maximum internal global clock frequency	*Note (8)*	90.9		90.9		MHz
t_{ACNT}	Minimum array clock period			11		11	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (8)*	90.9		90.9		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	125		125		MHz

Internal Timing Parameters			Speed Grade				
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			1		2	ns
t_{IO}	I/O input pad and buffer delay			1		2	ns
t_{FIN}	Fast input delay	*Note (3)*		1		1	ns
t_{SEXP}	Shared expander delay			7		7	ns
t_{PEXP}	Parallel expander delay			1		1	ns
t_{LAD}	Logic array delay			7		5	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{IOE}	Internal output enable delay	*Note (3)*		2		2	ns
t_{OD1}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF, *Note (1)*		1		3	ns
t_{OD2}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (7)*		2		4	ns
t_{OD3}	Output buffer & pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF, *Notes (1), (3), (7)*		5		7	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF, *Note (7)*		6		6	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (7)*		7		7	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF, *Note (7)*		10		10	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6	ns
t_{SU}	Register setup time		1		4		ns
t_{H}	Register hold time		6		4		ns
t_{FSU}	Register setup time of fast input	*Note (3)*	4		2		ns
t_{FH}	Register hold time of fast input	*Note (3)*	0		2		ns
t_{RD}	Register delay			2		1	ns
t_{COMB}	Combinatorial delay			2		1	ns
t_{IC}	Array clock delay			5		5	ns
t_{EN}	Register enable time			7		5	ns
t_{GLOB}	Global control delay			2		0	ns
t_{PRE}	Register preset time			4		3	ns
t_{CLR}	Register clear time			4		3	ns
t_{PIA}	PIA delay			1		1	ns
t_{LPA}	Low-power adder	*Note (8)*		12		12	ns

External Timing Parameters			Speed Grade						
			-15		-15T		-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		15		20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		15		15		20	ns
t_{SU}	Global clock setup time		11		11		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{FSU}	Global clock setup time of fast input	*Note (3)*	3		–		5		ns
t_{FH}	Global clock hold time of fast input	*Note (3)*	1		–		2		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8		8		12	ns
t_{CH}	Global clock high time		5		6		6		ns
t_{CL}	Global clock low time		5		6		6		ns
t_{ASU}	Array clock setup time		4		4		5		ns
t_{AH}	Array clock hold time		4		4		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		15		20	ns
t_{ACH}	Array clock high time		6		6.5		8		ns
t_{ACL}	Array clock low time		6		6.5		8		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (4)*	1		1		1		ns
t_{CNT}	Minimum global clock period			13		13		16	ns
f_{CNT}	Maximum internal global clock frequency	*Note (8)*	76.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			13		13		16	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (8)*	76.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	100		83.3		83.3		MHz

Internal Timing Parameters			Speed Grade						
			-15		-15T		-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2		2		3	ns
t_{IO}	I/O input pad and buffer delay			2		2		3	ns
t_{FIN}	Fast input delay	*Note (3)*		2		–		4	ns
t_{SEXP}	Shared expander delay			8		10		9	ns
t_{PEXP}	Parallel expander delay			1		1		2	ns
t_{LAD}	Logic array delay			6		6		8	ns
t_{LAC}	Logic control array delay			6		6		8	ns
t_{IOE}	Internal output enable delay	*Note (3)*		3		–		4	ns
t_{OD1}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF, *Note (1)*		4		4		5	ns
t_{OD2}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (7)*		5		–		6	ns
t_{OD3}	Output buffer & pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF, *Notes (3), (7)*		8		–		9	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF, *Note (7)*		6		6		10	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (7)*		7		–		11	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF, *Note (7)*		10		–		14	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		10	ns
t_{SU}	Register setup time		4		4		4		ns
t_{H}	Register hold time		4		4		5		ns
t_{FSU}	Register setup time of fast input	*Note (3)*	2		–		4		ns
t_{FH}	Register hold time of fast input	*Note (3)*	2		–		3		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			6		6		8	ns
t_{EN}	Register enable time			6		6		8	ns
t_{GLOB}	Global control delay			1		1		3	ns
t_{PRE}	Register preset time			4		4		4	ns
t_{CLR}	Register clear time			4		4		4	ns
t_{PIA}	PIA delay			2		2		3	ns
t_{LPA}	Low-power adder	*Note (8)*		13		15		15	ns

Notes to tables:

(1) Operating conditions:
V_{CCINT} = 5.0 V ± 5%, V_{CCIO} = 5.0 V ± 5% (except where noted), T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5.0 V ± 10%, V_{CCIO} = 5.0 V ± 10% (except where noted), T_A = –40° C to 85° C for industrial use.

(2) Timing parameters for some devices are preliminary. See Table 2 on page 195 of this data sheet for available speed grades and Table 4 on page 197 for available packages.

(3) This parameter applies only to MAX 7000E and MAX 7000S devices.

(4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(5) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(6) The f_{MAX} values represent the highest frequency for pipelined data.

(7) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial and industrial use.

(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in the low-power mode.

EPM7032V AC Operating Conditions *Note (1)*

External Timing Parameters			EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{SU}	Global clock setup time		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		7		8		12	ns
t_{CH}	Global clock high time		4		5		6		ns
t_{CL}	Global clock low time		4		5		6		ns
t_{ASU}	Array clock setup time		4		4		5		ns
t_{AH}	Array clock hold time		4		4		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12		15		20	ns
t_{ACH}	Array clock high time		5		6		8		ns
t_{ACL}	Array clock low time		5		6		8		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (2)*	1		1		1		ns
t_{CNT}	Minimum global clock period			11		13		16	ns
f_{CNT}	Maximum internal global clock frequency	*Note (3)*	90.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			11		13		16	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (3)*	90.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (4)*	125		100		83.3		MHz

EPM7032V AC Operating Conditions *Note (1)*

Internal Timing Parameters			EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		2		3	ns
t_{IO}	I/O input pad and buffer delay			3		2		3	ns
t_{SEXP}	Shared expander delay			7		8		9	ns
t_{PEXP}	Parallel expander delay			1		1		2	ns
t_{LAD}	Logic array delay			4		6		8	ns
t_{LAC}	Logic control array delay			4		6		8	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4		5	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		9	ns
t_{SU}	Register setup time		5		4		4		ns
t_{H}	Register hold time		4		4		5		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			4		6		8	ns
t_{EN}	Register enable time			4		6		8	ns
t_{GLOB}	Global control delay			0		1		3	ns
t_{PRE}	Register preset time			3		4		4	ns
t_{CLR}	Register clear time			3		4		4	ns
t_{PIA}	PIA delay			1		2		3	ns
t_{LPA}	Low-power adder	*Note (5)*		15		17		20	ns

Notes to tables:

(1) Operating conditions: V_{CC} = 3.3 V ± 10%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 3.3 V ± 10%, T_A = –40° C to 85° C for industrial use.

(2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.

(4) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(5) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

MAX 7000 3.3-V Device Power-Down/Chip-Enable Timing Parameters

Power-Down Timing Parameters		EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{ISUPD}	Input or I/O input setup time before power down	30		30		35		ns
t_{IHPD}	Input or I/O input hold time after power down	0		0		0		ns
t_{GCSUPD}	Global clock setup time before power down	20		20		25		ns
t_{GCHPD}	Global clock hold time after power down	0		0		0		ns
t_{ACSUPD}	Array clock setup time before power down	30		30		35		ns
t_{ACHPD}	Array clock hold time after power down	0		0		0		ns
t_{HPD}	Minimum high pulse width of power-down pin	800		800		900		ns
t_{LPD}	Minimum low pulse width of power-down pin	800		800		900		ns
t_{PDOWN}	Power down delay		800		800		900	ns

Chip-Enable Timing Parameters		EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{ISTCE}	Input or I/O input stable after chip enable		60		60		70	ns
t_{GCSTCE}	Global clock stable after chip enable		60		60		70	ns
t_{ACSTCE}	Array clock stable after chip enable		60		60		70	ns
t_{CE}	Data stable after chip enable		700		700		800	ns

Power Consumption

Supply power (P) versus frequency (f_{MAX} in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO}$$

$$P = I_{CCACTIVE} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in this data book.

The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} =$$

$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times tog_{LC}$$

The parameters in this equation are:

MC_{TON} = Number of macrocells with the Turbo Bit on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (**.rpt**)
f_{MAX} = Highest clock frequency to the device
tog_{LC} = Average ratio of logic cells toggling at each clock (typically 0.125)
A, B, C = Constants, shown in Table 5

Table 5. MAX 7000 I_{CC} Equation Constants

Device	Constant A	Constant B	Constant C
EPM7032	1.87	0.52	0.144
EPM7032V	0.83	0.40	0.048
EPM7064	1.63	0.74	0.144
EPM7096	1.63	0.74	0.144
EPM7128E	1.17	0.54	0.096
EPM7160E	1.17	0.54	0.096
EPM7192E	1.17	0.54	0.096
EPM7256E	1.17	0.54	0.096
EPM7032S, *Note (1)*	0.93	0.40	0.040
EPM7064S, *Note (1)*	0.93	0.40	0.040
EPM7096S, *Note (1)*	0.93	0.40	0.040
EPM7128S, *Note (1)*	0.93	0.40	0.040
EPM7160S, *Note (1)*	0.93	0.40	0.040
EPM7192S, *Note (1)*	0.93	0.40	0.040
EPM7256S, *Note (1)*	0.93	0.40	0.040

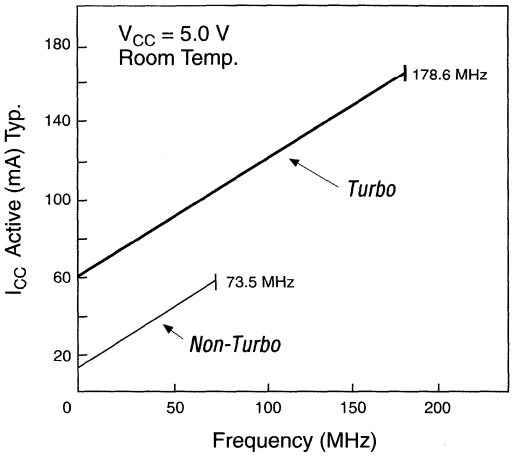
Note:
(1) Values for MAX 7000S devices are preliminary.

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

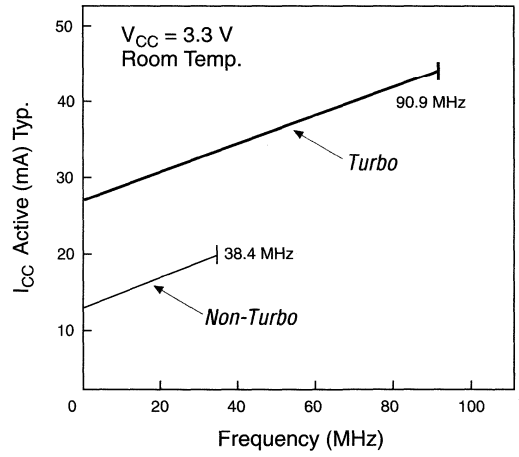
Figure 15 shows typical supply current versus frequency for MAX 7000 devices.

Figure 15. I_{CC} vs. Frequency for MAX 7000 Devices (Part 1 of 2)

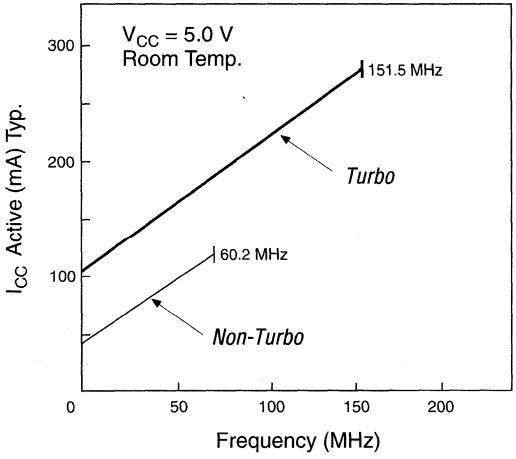
EPM7032



EPM7032V



EPM7064



EPM7096

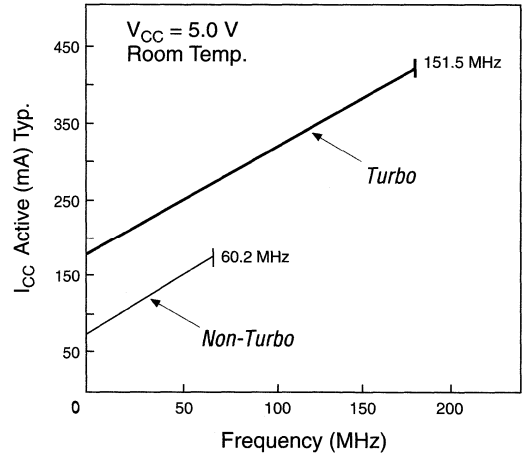
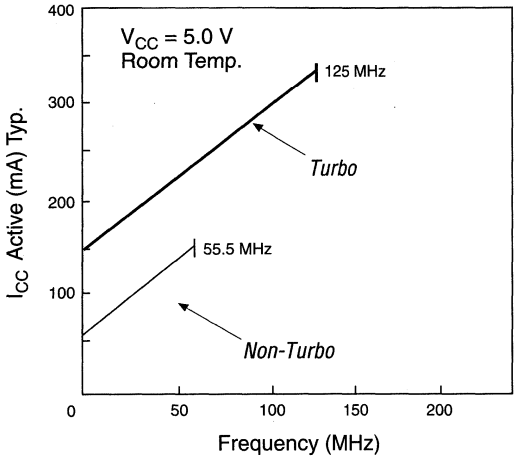
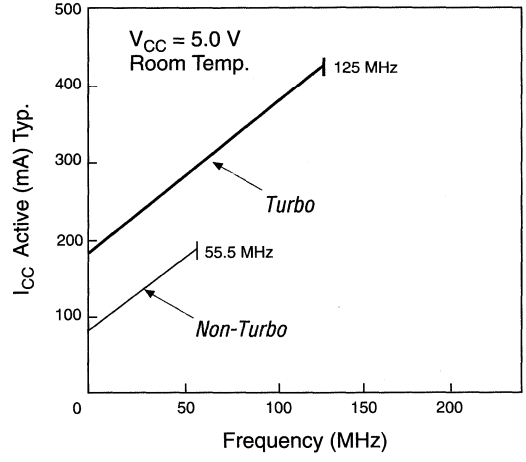


Figure 15. I_{CC} vs. Frequency for MAX 7000 Devices (Part 2 of 2)

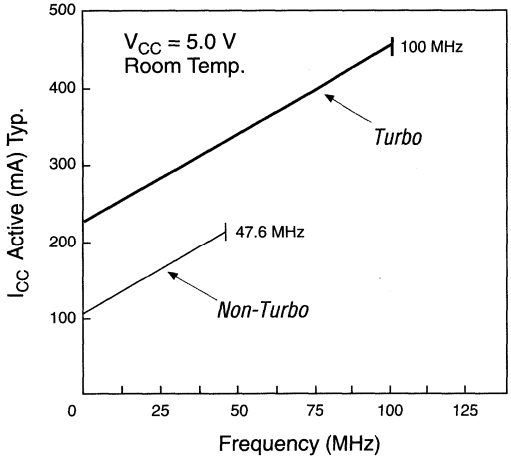
EPM7128E



EPM7160E



EPM7192E



EPM7256E

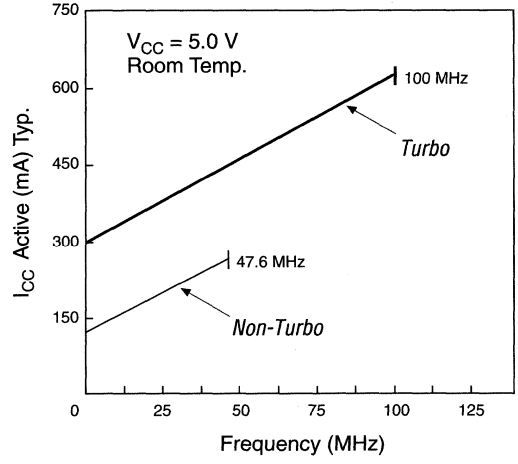
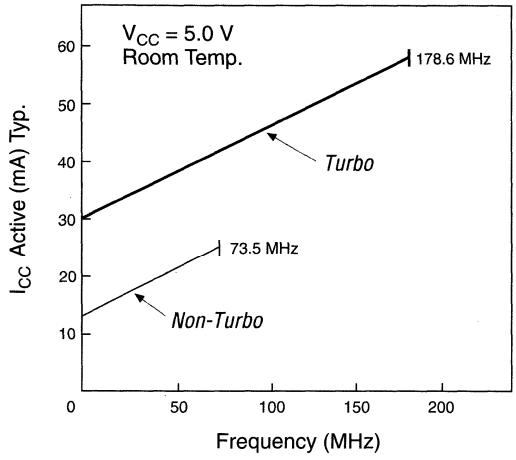


Figure 16 shows typical supply current versus frequency for MAX 7000S devices.

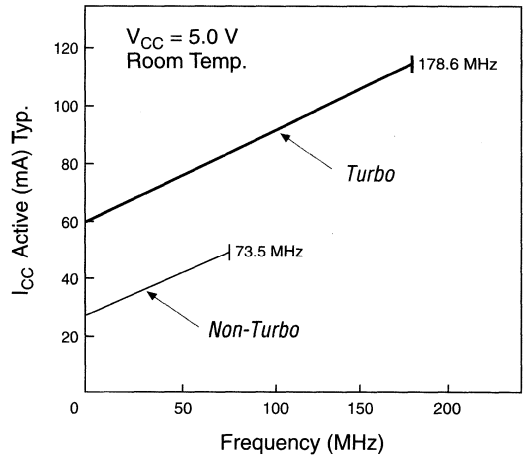
Figure 16. I_{CC} vs. Frequency for MAX 7000S Devices (Part 1 of 2)

Information on MAX 7000S devices is preliminary.

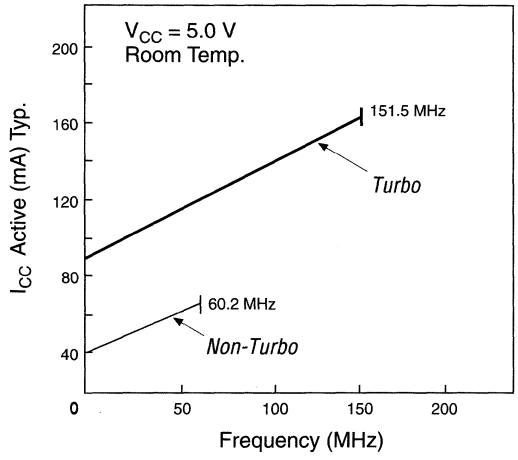
EPM7032S



EPM7064S



EPM7096S



EPM7128S

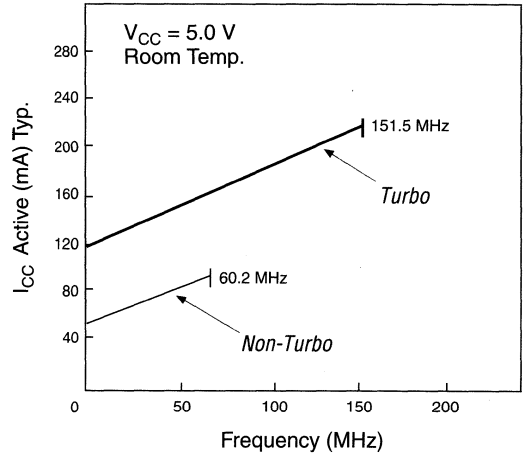
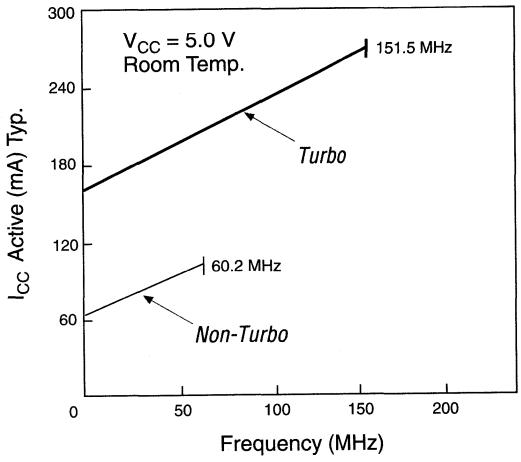


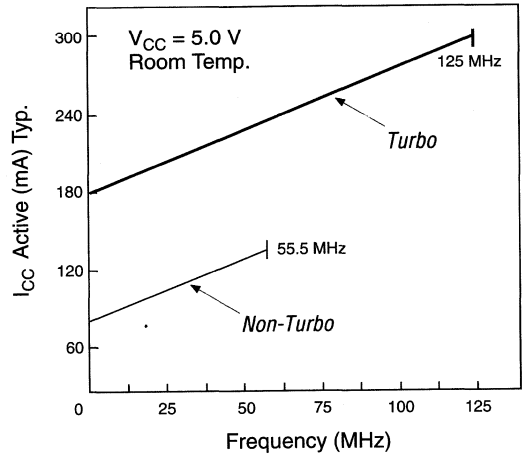
Figure 16. I_{CC} vs. Frequency for MAX 7000S Devices (Part 2 of 2)

Information on MAX 7000S devices is preliminary.

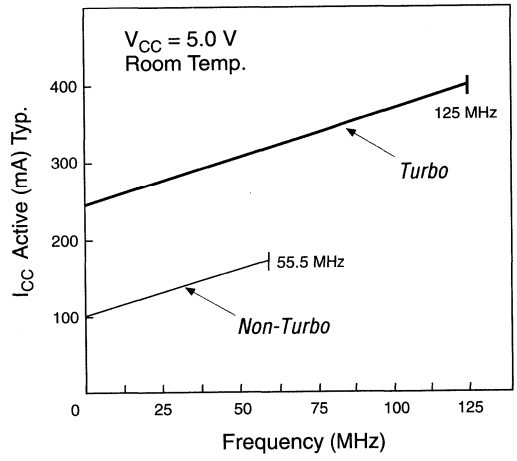
EPM7160S



EPM7192S



EPM7256S



Device Pin-Outs

Tables 6 through 19 show the pin names and numbers for the pins in each MAX 7000 device package.

Table 6. EPM7032, EPM7032V & EPM7032S Dedicated Pin-Outs *Note (1)*

Pin Name	44-Pin J-Lead	44-Pin PQFP/TQFP
INPUT/GCLK	43	37
INPUT/GCLRn	1	39
INPUT/OE1	44	38
INPUT/OE2/GCLK2 *(2)*	2	40
TDI *(3)*	7	1
TMS *(3)*	13	7
TCK *(3)*	32	26
TDO *(3)*	38	32
PDn *(4)*	3	41
GND	10, 22, 30, 42	4, 16, 24, 36
VCC	3, 15, 23, 35	9, 17, 29, 41
No Connect (N.C.)	–	–
Total User I/O Pins	32	32

Table 7. EPM7032, EPM7032V & EPM7032S I/O Pin-Outs *Note (1)*

MC	LAB	44-Pin J-Lead	44-Pin PQFP/TQFP	MC	LAB	44-Pin J-Lead	44-Pin PQFP/TQFP
1	A	4	42	17	B	41	35
2	A	5	43	18	B	40	34
3	A	6	44	19	B	39	33
4	A	7 *(3)*	1 *(3)*	20	B	38 *(3)*	32 *(3)*
5	A	8	2	21	B	37	31
6	A	9	3	22	B	36	30
7	A	11	5	23	B	34	28
8	A	12	6	24	B	33	27
9	A	13 *(3)*	7 *(3)*	25	B	32 *(3)*	26 *(3)*
10	A	14	8	26	B	31	25
11	A	16	10	27	B	29	23
12	A	17	11	28	B	28	22
13	A	18	12	29	B	27	21
14	A	19	13	30	B	26	20
15	A	20	14	31	B	25	19
16	A	21	15	32	B	24	18

Notes to tables:

(1) Information on MAX 7000S devices is preliminary.
(2) The GCLK2 pin is available in MAX 7000S devices only.
(3) In MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.
(4) The PDn pin is available in the EPM7032V device only.

Table 8. EPM7064 & EPM7064S Dedicated Pin-Outs *Note (1)*

Dedicated Pin	44-Pin J-Lead	44-Pin TQFP	68-Pin J-Lead	84-Pin J-Lead	100-Pin PQFP
INPUT/GCLK	43	37	67	83	89
INPUT/GCLRn	1	39	1	1	91
INPUT/OE1	44	38	68	84	90
INPUT/OE2/GCLK2 *(2)*	2	40	2	2	92
TDI *(3)*	7	1	12	14	6
TMS *(3)*	13	7	19	23	17
TCK *(3)*	32	26	50	62	64
TDO *(3)*	38	32	57	71	75
GND	10, 22, 30, 42	4, 16, 24, 36	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
VCCINT (5.0 V only)	3, 15, 23, 35	9, 17, 29, 41	3, 35	3, 43	41, 93
VCCIO (3.3 V or 5.0 V)	–	–	11, 21, 31, 43, 53, 63	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84
No Connect (N.C.)	–	–	–	–	1, 2, 7, 9, 24, 26, 29, 30, 51, 52, 55, 57, 72, 74, 79, 80
Total User I/O Pins	32	32	48	64	64

Table 9. EPM7064 & EPM7064S I/O Pin-Outs *Note (1)*

MC	LAB	44-Pin J-Lead	44-Pin TQFP	68-Pin J-Lead	84-Pin J-Lead	100-Pin PQFP	MC	LAB	44-Pin J-Lead	44-Pin TQFP	68-Pin J-Lead	84-Pin J-Lead	100-Pin PQFP
1	A	12	6	18	22	16	17	B	21	15	33	41	39
2	A	–	–	–	21	15	18	B	–	–	–	40	38
3	A	11	5	17	20	14	19	B	20	14	32	39	37
4	A	9	3	15	18	12	20	B	19	13	30	37	35
5	A	8	2	14	17	11	21	B	18	12	29	36	34
6	A	–	–	13	16	10	22	B	–	–	28	35	33
7	A	–	–	–	15	8	23	B	–	–	–	34	32
8	A	7 *(3)*	1 *(3)*	12 *(3)*	14 *(3)*	6 *(3)*	24	B	17	11	27	33	31
9	A	–	–	10	12	4	25	B	16	10	25	31	27
10	A	–	–	–	11	3	26	B	–	–	–	30	25
11	A	6	44	9	10	100	27	B	–	–	24	29	23
12	A	–	–	8	9	99	28	B	–	–	23	28	22
13	A	–	–	7	8	98	29	B	–	–	22	27	21
14	A	5	43	5	6	96	30	B	14	8	20	25	19
15	A	–	–	–	5	95	31	B	–	–	–	24	18
16	A	4	42	4	4	94	32	B	13 *(3)*	7 *(3)*	19 *(3)*	23 *(3)*	17 *(3)*
33	C	24	18	36	44	42	49	D	33	27	51	63	65
34	C	–	–	–	45	43	50	D	–	–	–	64	66
35	C	25	19	37	46	44	51	D	34	28	52	65	67
36	C	26	20	39	48	46	52	D	36	30	54	67	69
37	C	27	21	40	49	47	53	D	37	31	55	68	70
38	C	–	–	41	50	48	54	D	–	–	56	69	71
39	C	–	–	–	51	49	55	D	–	–	–	70	73
40	C	28	22	42	52	50	56	D	38 *(3)*	32 *(3)*	57 *(3)*	71 *(3)*	75 *(3)*
41	C	29	23	44	54	54	57	D	39	33	59	73	77
42	C	–	–	–	55	56	58	D	–	–	–	74	78
43	C	–	–	45	56	58	59	D	–	–	60	75	81
44	C	–	–	46	57	59	60	D	–	–	61	76	82
45	C	–	–	47	58	60	61	D	–	–	62	77	83
46	C	31	25	49	60	62	62	D	40	34	64	79	85
47	C	–	–	–	61	63	63	D	–	–	–	80	86
48	C	32 *(3)*	26 *(3)*	50 *(3)*	62 *(3)*	64 *(3)*	64	D	41	35	65	81	87

Notes to tables:

(1) Information on MAX 7000S devices is preliminary.

(2) The GCLK2 pin is available in MAX 7000S devices only.

(3) In MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

Table 10. EPM7096 & EPM7096S Dedicated Pin-Outs *Notes (1), (2)*

Dedicated Pin	68-Pin J-Lead	84-Pin J-Lead	100-Pin PQFP
INPUT/GCLK1	67	83	89
INPUT/GCLRn	1	1	91
INPUT/OE1	68	84	90
INPUT/OE2/GCLK2 *(2)*	2	2	92
TDI *(3)*	12	14	6
TMS *(3)*	19	23	17
TCK *(3)*	50	62	64
TDO *(3)*	57	71	75
GND	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
VCCINT (5.0 V only)	3, 35	3, 43	41, 93
VCCIO (3.3 V or 5.0 V)	11, 21, 31, 43, 53, 63	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84
No Connect (N.C.)	–	6, 39, 46, 79	9, 24, 37, 44, 57, 72, 85, 96
Total User I/O Pins	48	60	72

Table 11. EPM7096 & EPM7096S I/O Pin-Outs (Part 1 of 2) *Note (1)*

MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin PQFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin PQFP
1	A	13	16	8	17	B	23	28	23
2	A	–	–	–	18	B	–	–	–
3	A	–	15	7	19	B	22	27	22
4	A	12 *(3)*	14 *(3)*	6 *(3)*	20	B	–	–	21
5	A	–	–	4	21	B	20	25	19
6	A	10	12	3	22	B	–	24	18
7	A	–	–	–	23	B	–	–	–
8	A	9	11	2	24	B	19 *(3)*	23 *(3)*	17 *(3)*
9	A	8	10	1	25	B	18	22	16
10	A	–	–	–	26	B	–	–	–
11	A	–	9	100	27	B	17	21	15
12	A	7	8	99	28	B	–	20	14
13	A	–	–	98	29	B	15	18	12
14	A	5	5	95	30	B	–	–	11
15	A	–	–	–	31	B	–	–	–
16	A	4	4	94	32	B	14	17	10

Table 11. EPM7096 & EPM7096S I/O Pin-Outs (Part 2 of 2) *Note (1)*

MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin PQFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin PQFP
33	C	33	41	39	49	D	36	44	42
34	C	–	–	–	50	D	–	–	–
35	C	32	40	38	51	D	37	45	43
36	C	–	–	35	52	D	–	–	46
37	C	30	37	34	53	D	39	48	47
38	C	–	36	33	54	D	–	49	48
39	C	–	–	–	55	D	–	–	–
40	C	29	35	32	56	D	40	50	49
41	C	28	34	31	57	D	41	51	50
42	C	–	–	–	58	D	–	–	–
43	C	27	33	30	59	D	42	52	51
44	C	–	–	29	60	D	–	–	52
45	C	25	31	27	61	D	44	54	54
46	C	–	30	26	62	D	–	55	55
47	C	–	–	–	63	D	–	–	–
48	C	24	29	25	64	D	45	56	56
65	E	46	57	58	81	F	56	69	73
66	E	–	–	–	82	F	–	–	–
67	E	47	58	59	83	F	–	70	74
68	E	–	–	60	84	F	57 *(3)*	71 *(3)*	75 *(3)*
69	E	49	60	62	85	F	–	–	77
70	E	–	61	63	86	F	59	73	78
71	E	–	–	–	87	F	–	–	–
72	E	50 *(3)*	62 *(3)*	64 *(3)*	88	F	60	74	79
73	E	51	63	65	89	F	61	75	80
74	E	–	–	–	90	F	–	–	–
75	E	52	64	66	91	F	–	76	81
76	E	–	65	67	92	F	62	77	82
77	E	54	67	69	93	F	–	–	83
78	E	–	–	70	94	F	64	80	86
79	E	–	–	–	95	F	–	–	–
80	E	55	68	71	96	F	65	81	87

Notes to tables:

(1) Information on MAX 7000S devices is preliminary.

(2) The GCLK2 pin is available in MAX 7000S devices only.

(3) In MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

Table 12. EPM7128E & EPM7128S Dedicated Pin-Outs *Note (1)*

Dedicated Pin	84-Pin J-Lead	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP
INPUT/GCLK1	83	89	–	139
INPUT/GCLRn	1	91	–	141
INPUT/OE1	84	90	88	140
INPUT/OE2/GCLK2	2	92	87	142
TDI *(2)*	14	6	4	9
TMS *(2)*	23	17	15	22
TCK *(2)*	62	64	62	99
TDO *(2)*	71	75	73	112
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	11, 26, 38, 43, 59, 74, 86	17, 42, 60, 66, 95, 113, 138, 148
VCCINT (5.0 V only)	3, 43	41, 93	39, 91	61, 143
VCCIO (3.3 V or 5.0 V)	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84	3, 18, 34, 51, 66	8, 26, 55, 79, 104, 133
No Connect (N.C.)	–	–	–	1, 2, 3, 4, 5, 6, 7, 34, 35, 36, 37, 38, 39, 40, 44, 45, 46, 47, 74, 75, 76, 77, 81, 82, 83, 84, 85, 86, 87, 114, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157
Total User I/O PIns	64	80	80	96

Table 13. EPM7128E & EPM7128S I/O Pin-Outs (Part 1 of 2) *Note (1)*

MC	LAB	84-Pin J-Lead	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	MC	LAB	84-Pin J-Lead	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP
1	A	–	4	2	160	17	B	22	16	14	21
2	A	–	–	–	–	18	B	–	–	–	–
3	A	12	3	1	159	19	B	21	15	13	20
4	A	–	–	–	158	20	B	–	–	–	19
5	A	11	2	100	153	21	B	20	14	12	18
6	A	10	1	99	152	22	B	–	12	10	16
7	A	–	–	–	–	23	B	–	–	–	–
8	A	9	100	98	151	24	B	18	11	9	15
9	A	–	99	97	150	25	B	17	10	8	14
10	A	–	–	–	–	26	B	–	–	–	–
11	A	8	98	96	149	27	B	16	9	7	13
12	A	–	–	–	147	28	B	–	–	–	12
13	A	6	96	94	146	29	B	15	8	6	11
14	A	5	95	93	145	30	B	–	7	5	10
15	A	–	–	–	–	31	B	–	–	–	–
16	A	4	94	92	144	32	B	14 *(2)*	6 *(2)*	4 *(2)*	9 *(2)*
33	C	–	27	25	41	49	D	41	39	37	59
34	C	–	–	–	–	50	D	–	–	–	–
35	C	31	26	24	33	51	D	40	38	36	58
36	C	–	–	–	32	52	D	–	–	–	57
37	C	30	25	23	31	53	D	39	37	35	56
38	C	29	24	22	30	54	D	–	35	33	54
39	C	–	–	–	–	55	D	–	–	–	–
40	C	28	23	21	29	56	D	37	34	32	53
41	C	–	22	20	28	57	D	36	33	31	52
42	C	–	–	–	–	58	D	–	–	–	–
43	C	27	21	19	27	59	D	35	32	30	51
44	C	–	–	–	25	60	D	–	–	–	50
45	C	25	19	17	24	61	D	34	31	29	49
46	C	24	18	16	23	62	D	–	30	28	48
47	C	–	–	–	–	63	D	–	–	–	–
48	C	23 *(2)*	17 *(2)*	15 *(2)*	22 *(2)*	64	D	33	29	27	43

Table 13. EPM7128E & EPM7128S I/O Pin-Outs (Part 2 of 2) *Note (1)*

MC	LAB	84-Pin J-Lead	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	MC	LAB	84-Pin J-Lead	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP
65	E	44	42	40	62	81	F	–	54	52	80
66	E	–	–	–	–	82	F	–	–	–	–
67	E	45	43	41	63	83	F	54	55	53	88
68	E	–	–	–	64	84	F	–	–	–	89
69	E	46	44	42	65	85	F	55	56	54	90
70	E	–	46	44	67	86	F	56	57	55	91
71	E	–	–	–	–	87	F	–	–	–	–
72	E	48	47	45	68	88	F	57	58	56	92
73	E	49	48	45	69	89	F	–	59	57	93
74	E	–	–	–	–	90	F	–	–	–	–
75	E	50	49	47	70	91	F	58	60	58	94
76	E	–	–	–	71	92	F	–	–	–	96
77	E	51	50	48	72	93	F	60	62	60	97
78	E	–	51	49	73	94	F	61	63	61	98
79	E	–	–	–	–	95	F	–	–	–	–
80	E	52	52	50	78	96	F	62 *(2)*	64 *(2)*	62 *(2)*	99 *(2)*
97	G	63	65	63	100	113	H	–	77	75	121
98	G	–	–	–	–	114	H	–	–	–	–
99	G	64	66	64	101	115	H	73	78	76	122
100	G	–	–	–	102	116	H	–	–	–	123
101	G	65	67	65	103	117	H	74	79	77	128
102	G	–	69	67	105	118	H	75	80	78	129
103	G	–	–	–	–	119	H	–	–	–	–
104	G	67	70	68	106	120	H	76	81	79	130
105	G	68	71	69	107	121	H	–	82	80	131
106	G	–	–	–	–	122	H	–	–	–	–
107	G	69	72	70	108	123	H	77	83	81	132
108	G	–	–	–	109	124	H	–	–	–	134
109	G	70	73	71	110	125	H	79	85	83	135
110	G	–	74	72	111	126	H	80	86	84	136
111	G	–	–	–	–	127	H	–	–	–	–
112	G	71 *(2)*	75 *(2)*	73 *(2)*	112 *(2)*	128	H	81	87	85	137

Notes to tables:

(1) Information on MAX 7000S devices is preliminary.

(2) In MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for boundary-scan testing or for ISP, this pin is not available as a user I/O pin.

Table 14. EPM7160E & EPM7160S Dedicated Pin-Outs *Note (1)*

Dedicated Pin	84-Pin J-Lead	100-Pin PQFP	160-Pin PQFP
INPUT/GCLK1	83	89	139
INPUT/GCLRn	1	91	141
INPUT/OE1	84	90	140
INPUT/OE2/GCLK2	2	92	142
TDI *(2)*	14	6	9
TMS *(2)*	23	17	22
TCK *(2)*	62	64	99
TDO *(2)*	71	75	112
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCCINT (5.0 V only)	3, 43	41, 93	61, 143
VCCIO (3.3 V or 5.0 V)	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84	8, 26, 55, 79, 104, 133
No Connect (N.C.)	6, 39, 46, 79	–	1, 2, 3, 4, 5, 6, 34, 35, 36, 37, 38, 39, 40, 45, 46, 47, 74, 75, 76, 81, 82, 83, 84, 85, 86, 87, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157
Total User I/O Pins	60	80	100

Table 15. EPM7160E & EPM7160S I/O Pin-Outs (Part 1 of 3) *Note (1)*

MC	LAB	84-Pin J-Lead	100-Pin PQFP	160-Pin PQFP	MC	LAB	84-Pin J-Lead	100-Pin PQFP	160-Pin PQFP
1	A	11	2	158	17	B	18	11	15
2	A	–	–	–	18	B	–	–	–
3	A	10	1	153	19	B	17	10	14
4	A	–	–	–	20	B	–	–	–
5	A	–	–	152	21	B	–	–	13
6	A	–	100	151	22	B	–	9	12
7	A	–	–	–	23	B	–	–	–
8	A	9	99	150	24	B	16	8	11
9	A	8	98	149	25	B	15	7	10
10	A	–	–	–	26	B	–	–	–
11	A	5	96	147	27	B	14 *(2)*	6 *(2)*	9 *(2)*
12	A	–	–	–	28	B	–	–	–
13	A	–	–	146	29	B	–	–	7
14	A	–	95	145	30	B	–	4	160
15	A	–	–	–	31	B	–	–	–
16	A	4	94	144	32	B	12	3	159
33	C	–	21	27	49	D	–	–	48
34	C	–	–	–	50	D	–	–	–
35	C	25	19	25	51	D	33	30	44
36	C	–	–	–	52	D	–	–	–
37	C	–	–	24	53	D	–	29	43
38	C	24	18	23	54	D	31	27	41
39	C	–	–	–	55	D	–	–	–
40	C	23 *(2)*	17 *(2)*	22 *(2)*	56	D	30	26	33
41	C	–	12	16	57	D	–	–	32
42	C	–	–	–	58	D	–	–	–
43	C	20	14	18	59	D	29	25	31
44	C	–	–	–	60	D	–	–	–
45	C	–	–	19	61	D	–	24	30
46	C	21	15	20	62	D	28	23	29
47	C	–	–	–	63	D	–	–	–
48	C	22	16	21	64	D	27	22	28

Table 15. EPM7160E & EPM7160S I/O Pin-Outs (Part 2 of 3) *Note (1)*

MC	LAB	84-Pin J-Lead	100-Pin PQFP	160-Pin PQFP	MC	LAB	84-Pin J-Lead	100-Pin PQFP	160-Pin PQFP
65	E	–	–	59	81	F	–	–	62
66	E	–	–	–	82	F	–	–	–
67	E	41	39	58	83	F	44	42	63
68	E	–	–	–	84	F	–	–	–
69	E	–	38	57	85	F	–	43	64
70	E	40	37	56	86	F	45	44	65
71	E	–	–	–	87	F	–	–	–
72	E	37	35	54	88	F	48	46	67
73	E	–	–	53	89	F	–	–	68
74	E	–	–	–	90	F	–	–	–
75	E	36	34	52	91	F	49	47	69
76	E	–	–	–	92	F	–	–	–
77	E	–	33	51	93	F	–	48	70
78	E	35	32	50	94	F	50	49	71
79	E	–	–	–	95	F	–	–	–
80	E	34	31	49	96	F	51	50	72
97	G	–	–	73	113	H	–	60	94
98	G	–	–	–	114	H	–	–	–
99	G	52	51	77	115	H	60	62	96
100	G	–	–	–	116	H	–	–	–
101	G	–	52	78	117	H	–	–	97
102	G	54	54	80	118	H	61	63	98
103	G	–	–	–	119	H	–	–	–
104	G	55	55	88	120	H	62 *(2)*	64 *(2)*	99 *(2)*
105	G	–	–	89	121	H	–	69	105
106	G	–	–	–	122	H	–	–	–
107	G	56	56	90	123	H	65	67	103
108	G	–	–	–	124	H	–	–	–
109	G	–	57	91	125	H	–	–	102
110	G	57	58	92	126	H	64	66	101
111	G	–	–	–	127	H	–	–	–
112	G	58	59	93	128	H	63	65	100

Table 15. EPM7160E & EPM7160S I/O Pin-Outs (Part 3 of 3) *Note (1)*

MC	LAB	84-Pin J-Lead	100-Pin PQFP	160-Pin PQFP	MC	LAB	84-Pin J-Lead	100-Pin PQFP	160-Pin PQFP
129	I	67	70	106	145	J	74	79	123
130	I	–	–	–	146	J	–	–	–
131	I	68	71	107	147	J	75	80	128
132	I	–	–	–	148	J	–	–	–
133	I	–	–	108	149	J	–	–	129
134	I	–	72	109	150	J	–	81	130
135	I	–	–	–	151	J	–	–	–
136	I	69	73	110	152	J	76	82	131
137	I	70	74	111	153	J	77	83	132
138	I	–	–	–	154	J	–	–	–
139	I	71 *(2)*	75 *(2)*	112 *(2)*	155	J	80	85	134
140	I	–	–	–	156	J	–	–	–
141	I	–	–	114	157	J	–	–	135
142	I	–	77	121	158	J	–	86	136
143	I	–	–	–	159	J	–	–	–
144	I	73	78	122	160	J	81	87	137

Notes to tables:

(1) Information on MAX 7000S devices is preliminary.

(2) For MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for boundary-scan testing or with ISP, this pin is not available as a user I/O pin.

Table 16. EPM7192E & EPM7192S Dedicated Pin-Outs *Note (1)*

Dedicated Pin	160-Pin PGA	160-Pin PQFP
INPUT/GCLK1	M8	139
INPUT/GCLRn	N8	141
INPUT/OE1	P8	140
INPUT/OE2/GCLK2	R8	142
TDI *(2)*	P9	146
TMS *(2)*	G15	23
TCK *(2)*	G2	98
TDO *(2)*	R7	135
GND	C4, C6, C11, D7, D9, D13, G4, H12, J4, M7, M9, M13, N4, N11	3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148
VCCINT (5.0 V only)	C7, C9, N7, N9	56, 65, 137, 144
VCCIO (3.3 V or 5.0 V)	C5, C10, C12, D3, G12, H4, J12, M3, N5, N12	10, 25, 40, 55, 74, 89, 103, 118, 133, 155
No Connect (N.C.)	A1, A2, A14, A15, R1, R2, R14, R15	1, 11, 39,54, 67, 82, 110, 120
Total User I/O Pins	120	120

Table 17. EPM7192E & EPM7192S I/O Pin-Outs (Part 1 of 2) *Note (1)*

MC	LAB	160-Pin PGA	160-Pin PQFP	MC	LAB	160-Pin PGA	160-Pin PQFP	MC	LAB	160-Pin PGA	160-Pin PQFP
1	A	M12	156	17	B	L14	8	33	C	H14	21
2	A	–	–	18	B	–	–	34	C	–	–
3	A	P11	154	19	B	M14	7	35	C	J13	20
4	A	–	–	20	B	–	–	36	C	–	–
5	A	P12	153	21	B	M15	6	37	C	H15	19
6	A	P10	152	22	B	N14	5	38	C	J15	17
7	A	–	–	23	B	–	–	39	C	–	–
8	A	R12	151	24	B	N15	4	40	C	J14	16
9	A	N10	150	25	B	P15	2	41	C	K15	15
10	A	–	–	26	B	–	–	42	C	–	–
11	A	R11	149	27	B	N13	160	43	C	K13	14
12	A	–	–	28	B	–	–	44	C	–	–
13	A	R10	147	29	B	P14	159	45	C	L15	13
14	A	P9 *(2)*	146 *(2)*	30	B	P13	158	46	C	K14	12
15	A	–	–	31	B	–	–	47	C	–	–
16	A	R9	145	32	B	R13	157	48	C	L13	9
49	D	D15	33	65	E	B12	45	81	F	D8	60
50	D	–	–	66	E	–	–	82	F	–	–
51	D	E15	31	67	E	B13	44	83	F	A9	59
52	D	–	–	68	E	–	–	84	F	–	–
53	D	E14	30	69	E	C13	43	85	F	C8	58
54	D	F15	29	70	E	B14	42	86	F	B9	53
55	D	–	–	71	E	–	–	87	F	–	–
56	D	F13	28	72	E	C14	41	88	F	A10	52
57	D	G14	27	73	E	D12	38	89	F	B10	51
58	D	–	–	74	E	–	–	90	F	–	–
59	D	F14	26	75	E	B15	37	91	F	A11	50
60	D	–	–	76	E	–	–	92	F	–	–
61	D	G13	24	77	E	D14	36	93	F	B11	49
62	D	G15 *(2)*	23 *(2)*	78	E	C15	35	94	F	A12	48
63	D	–	–	79	E	–	–	95	F	–	–
64	D	H13	22	80	E	E13	34	96	F	A13	46

Table 17. EPM7192E & EPM7192S I/O Pin-Outs (Part 2 of 2) *Note (1)*

MC	LAB	160-Pin PGA	160-Pin PQFP	MC	LAB	160-Pin PGA	160-Pin PQFP	MC	LAB	160-Pin PGA	160-Pin PQFP
97	G	A8	61	113	H	A3	76	129	I	E3	88
98	G	–	–	114	H	–	–	130	I	–	–
99	G	B8	62	115	H	B4	77	131	I	F3	90
100	G	–	–	116	H	–	–	132	I	–	–
101	G	A7	63	117	H	B3	78	133	I	E2	91
102	G	A6	68	118	H	C3	79	134	I	F2	92
103	G	–	–	119	H	–	–	135	I	–	–
104	G	B7	69	120	H	B2	80	136	I	E1	93
105	G	A5	70	121	H	B1	83	137	I	G3	94
106	G	–	–	122	H	–	–	138	I	–	–
107	G	B6	71	123	H	C2	84	139	I	F1	95
108	G	–	–	124	H	–	–	140	I	–	–
109	G	A4	72	125	H	C1	85	141	I	G1	97
110	G	B5	73	126	H	D2	86	142	I	G2 *(2)*	98 *(2)*
111	G	–	–	127	H	–	–	143	I	–	–
112	G	D4	75	128	H	D1	87	144	I	H1	99
145	J	H2	100	161	K	L2	113	177	L	R3	125
146	J	–	–	162	K	–	–	178	L	–	–
147	J	J1	101	163	K	N1	114	179	L	R4	127
148	J	–	–	164	K	–	–	180	L	–	–
149	J	H3	102	165	K	L3	115	181	L	M4	128
150	J	J3	104	166	K	P1	116	182	L	R5	129
151	J	–	–	167	K	–	–	183	L	–	–
152	J	K1	105	168	K	M2	117	184	L	P5	130
153	J	J2	106	169	K	N2	119	185	L	R6	131
154	J	–	–	170	K	–	–	186	L	–	–
155	J	K2	107	171	K	P2	121	187	L	P6	132
156	J	–	–	172	K	–	–	188	L	–	–
157	J	K3	108	173	K	N3	122	189	L	N6	134
158	J	L1	109	174	K	P3	123	190	L	R7 *(2)*	135 *(2)*
159	J	–	–	175	K	–	–	191	L	–	–
160	J	M1	112	176	K	P4	124	192	L	P7	136

Notes to tables:

(1) Information on MAX 7000S devices is preliminary.

(2) For MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

Table 18. EPM7256E & EPM7256S Dedicated Pin-Outs *Note (1)*

Dedicated Pin	160-Pin PQFP *(2)*	192-Pin PGA	208-Pin RQFP
INPUT/GCLK1	139	P9	184
INPUT/GCLRn	141	R9	182
INPUT/OE1	140	T9	183
INPUT/OE2/GCLK2	142	U9	181
TDI *(3)*	146	U10	176
TMS *(3)*	23	H15	127
TCK *(3)*	98	H3	30
TDO *(3)*	135	U8	189
GND	3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148	C7, C13, D4, D8, D10, G14, H4, K14, L4, P8, P10, P15, R4, R11	14, 32, 50, 72, 75, 82, 94, 116, 134, 152, 174, 180, 185, 200
VCCINT (5.0 V only)	56, 65, 137, 144	D7, D11, P7, P11	74, 83, 179, 186
VCCIO (3.3 V or 5.0 V)	10, 25, 40, 55, 74, 89, 103, 118, 133, 155	C5, C11, D14, G4, H14, K4, L14, P3, R5, R14	5, 23, 41, 63, 85, 107, 125, 143, 165, 191
No Connect (N.C.)	–	–	1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208.
Total User I/O Pins	128	160	160

Table 19. EPM7256E & EPM7256S I/O Pin-Outs (Part 1 of 4) *Note (1)*

MC	LAB	160-Pin PQFP *(2)*	192-Pin PGA	208-Pin RQFP	MC	LAB	160-Pin PQFP *(2)*	192-Pin PGA	208-Pin RQFP
1	A	2	U17	153	17	B	12	N17	141
2	A	–	–	–	18	B	–	–	–
3	A	1	R16	154	19	B	11	M16	142
4	A	–	–	–	20	B	–	–	–
5	A	160	P14	159	21	B	9	M15	144
6	A	–	U16	160	22	B	–	P17	145
7	A	–	–	–	23	B	–	–	–
8	A	159	R15	161	24	B	8	N16	146
9	A	158	U15	162	25	B	7	R17	147
10	A	–	–	–	26	B	–	–	–
11	A	157	T15	163	27	B	6	P16	148
12	A	–	–	–	28	B	–	–	–
13	A	156	U14	164	29	B	5	T17	149
14	A	–	U13	166	30	B	–	N15	150
15	A	–	–	–	31	B	–	–	–
16	A	154	T14	167	32	B	4	T16	151
33	C	39	B17	108	49	D	49	A14	92
34	C	–	–	–	50	D	–	–	–
35	C	38	C15	109	51	D	48	B12	93
36	C	–	–	–	52	D	–	–	–
37	C	37	C17	110	53	D	46	B13	95
38	C	–	C16	111	54	D	–	A15	96
39	C	–	–	–	55	D	–	–	–
40	C	36	D17	112	56	D	45	B14	97
41	C	35	D15	113	57	D	44	A16	98
42	C	–	–	–	58	D	–	–	–
43	C	34	E17	114	59	D	43	C14	99
44	C	–	–	–	60	D	–	–	–
45	C	33	D16	115	61	D	42	B16	100
46	C	–	E15	117	62	D	–	B15	101
47	C	–	–	–	63	D	–	–	–
48	C	31	F16	118	64	D	41	A17	102

Table 19. EPM7256E & EPM7256S I/O Pin-Outs (Part 2 of 4) *Note (1)*

MC	LAB	160-Pin PQFP *(2)*	192-Pin PGA	208-Pin RQFP	MC	LAB	160-Pin PQFP *(2)*	192-Pin PGA	208-Pin RQFP
65	E	153	U12	168	81	F	21	J16	130
66	E	–	–	–	82	F	–	–	–
67	E	152	R13	169	83	F	20	J15	131
68	E	–	–	–	84	F	–	–	–
69	E	151	U11	170	85	F	19	K17	132
70	E	–	T13	171	86	F	–	J14	133
71	E	–	–	–	87	F	–	–	–
72	E	150	T11	172	88	F	17	K16	135
73	E	149	T12	173	89	F	16	K15	136
74	E	–	–	–	90	F	–	–	–
75	E	147	R12	175	91	F	15	L17	137
76	E	–	–	–	92	F	–	–	–
77	E	146 *(3)*	U10 *(3)*	176 *(3)*	93	F	14	L16	138
78	E	–	R10	177	94	F	–	M17	139
79	E	–	–	–	95	F	–	–	–
80	E	145	T10	178	96	F	13	L15	140
97	G	30	E16	119	113	H	60	C9	79
98	G	–	–	–	114	H	–	–	–
99	G	29	F17	120	115	H	59	D9	80
100	G	–	–	–	116	H	–	–	–
101	G	28	F15	121	117	H	58	C10	81
102	G	–	G16	122	118	H	–	A10	84
103	G	–	–	–	119	H	–	–	–
104	G	27	G15	123	120	H	54	A11	86
105	G	26	G17	124	121	H	53	B10	87
106	G	–	–	–	122	H	–	–	–
107	G	24	H17	126	123	H	52	A12	88
108	G	–	–	–	124	H	–	–	–
109	G	23 *(3)*	H15 *(3)*	127 *(3)*	125	H	51	B11	89
110	G	–	J17	128	126	H	–	A13	90
111	G	–	–	–	127	H	–	–	–
112	G	22	H16	129	128	H	50	C12	91

Table 19. EPM7256E & EPM7256S I/O Pin-Outs (Part 3 of 4) *Note (1)*

MC	LAB	160-Pin PQFP *(2)*	192-Pin PGA	208-Pin RQFP	MC	LAB	160-Pin PQFP *(2)*	192-Pin PGA	208-Pin RQFP
129	I	128	U6	197	145	J	100	J2	27
130	I	–	–	–	146	J	–	–	–
131	I	129	T5	196	147	J	101	J3	26
132	I	–	–	–	148	J	–	–	–
133	I	130	U7	195	149	J	102	K1	25
134	I	–	T6	194	150	J	–	J4	24
135	I	–	–	–	151	J	–	–	–
136	I	131	T7	193	152	J	104	K2	22
137	I	132	R6	192	153	J	105	K3	21
138	I	–	–	–	154	J	–	–	–
139	I	134	R7	190	155	J	106	L1	20
140	I	–	–	–	156	J	–	–	–
141	I	135 *(3)*	U8 *(3)*	189 *(3)*	157	J	107	L2	19
142	I	–	R8	188	158	J	–	M1	18
143	I	–	–	–	159	J	–	–	–
144	I	136	T8	187	160	J	108	L3	17
161	K	91	F3	38	177	L	61	B9	78
162	K	–	–	–	178	L	–	–	–
163	K	92	F1	37	179	L	62	C8	77
164	K	–	–	–	180	L	–	–	–
165	K	93	E2	36	181	L	63	A9	76
166	K	–	G2	35	182	L	–	A8	73
167	K	–	–	–	183	L	–	–	–
168	K	94	G3	34	184	L	67	A7	71
169	K	95	G1	33	185	L	68	B8	70
170	K	–	–	–	186	L	–	–	–
171	K	97	H1	31	187	L	69	A6	69
172	K	–	–	–	188	L	–	–	–
173	K	98 *(3)*	H3 *(3)*	30 *(3)*	189	L	70	B7	68
174	K	–	J1	29	190	L	–	A5	67
175	K	–	–	–	191	L	–	–	–
176	K	99	H2	28	192	L	71	C6	66

Table 19. EPM7256E & EPM7256S I/O Pin-Outs (Part 4 of 4) *Note (1)*

MC	LAB	160-Pin PQFP *(2)*	192-Pin PGA	208-Pin RQFP	MC	LAB	160-Pin PQFP *(2)*	192-Pin PGA	208-Pin RQFP
193	M	119	U1	4	209	N	109	N1	16
194	M	–	–	–	210	N	–	–	–
195	M	120	R2	3	211	N	110	M2	15
196	M	–	–	–	212	N	–	–	–
197	M	121	R3	206	213	N	112	M3	13
198	M	–	U2	205	214	N	–	P1	12
199	M	–	–	–	215	N	–	–	–
200	M	122	P4	204	216	N	113	N2	11
201	M	123	U3	203	217	N	114	R1	10
202	M	–	–	–	218	N	–	–	–
203	M	124	T3	202	219	N	115	P2	9
204	M	–	–	–	220	N	–	–	–
205	M	125	U4	201	221	N	116	T1	8
206	M	–	U5	199	222	N	–	N3	7
207	M	–	–	–	223	N	–	–	–
208	M	127	T4	198	224	N	117	T2	6
225	O	82	B1	49	241	P	72	A4	65
226	O	–	–	–	242	P	–	–	–
227	O	83	C3	48	243	P	73	B6	64
228	O	–	–	–	244	P	–	–	–
229	O	84	C1	47	245	P	75	B5	62
230	O	–	D3	46	246	P	–	A3	61
231	O	–	–	–	247	P	–	–	–
232	O	85	D1	45	248	P	76	B4	60
233	O	86	C2	44	249	P	77	A2	59
234	O	–	–	–	250	P	–	–	–
235	O	87	E1	43	251	P	78	C4	58
236	O	–	–	–	252	P	–	–	–
237	O	88	E3	42	253	P	79	B2	57
238	O	–	D2	40	254	P	–	B3	56
239	O	–	–	–	255	P	–	–	–
240	O	90	F2	39	256	P	80	A1	55

Notes to tables:

(1) Information on MAX 7000S devices is preliminary.

(2) Be sure to perform a complete thermal analysis before committing a design to this device package. See the *Operating Requirements for Altera Devices Data Sheet* in this data book for more information.

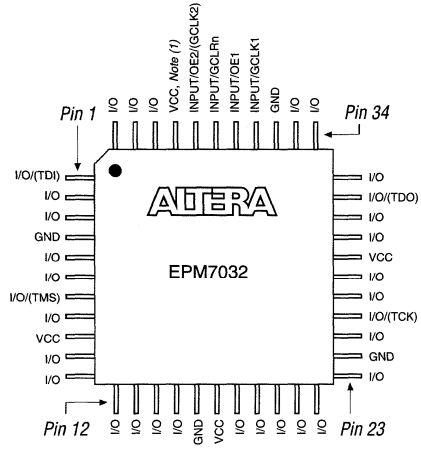
(3) For MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

Pin-Out Diagrams

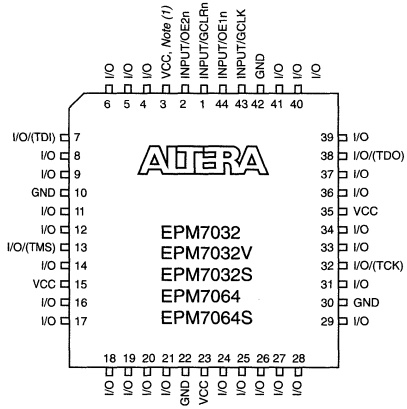
Figures 17 through 23 show the package pin-out diagrams for MAX 7000 devices.

Figure 17. 44-Pin Package Pin-Out Diagram

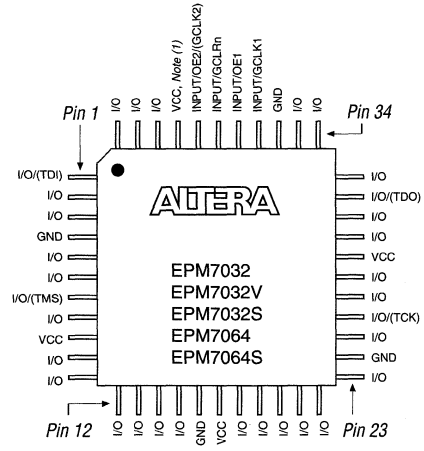
Package outlines not drawn to scale. Pin functions shown in parentheses are for MAX 7000S devices only.



44-Pin PQFP



44-Pin J-Lead



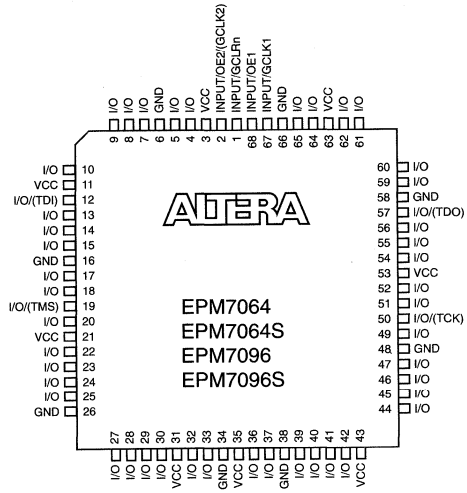
44-Pin TQFP

Note:

(1) This pin is a power-down pin (PDn) for the EPM7032V device.

Figure 18. 68-Pin Package Pin-Out Diagram

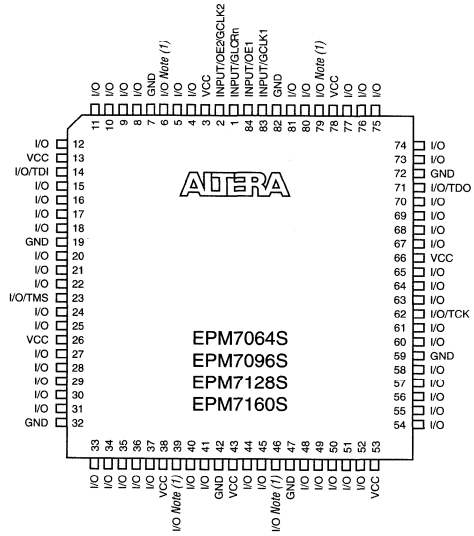
Package outlines not drawn to scale. Pin functions shown in parentheses are for MAX 7000S devices only.



68-Pin J-Lead

Figure 19. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale. Pin functions in parentheses are for MAX 7000S devices only.



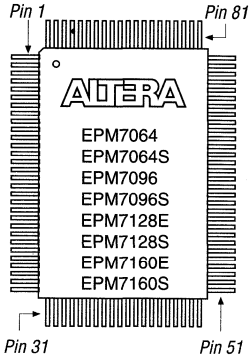
84-Pin J-Lead

Note:

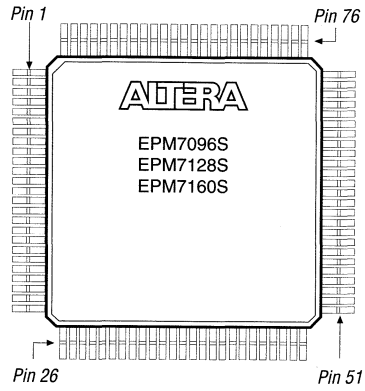
(1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7096S, EPM7160E, and EPM7160S devices.

Figure 20. 100-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



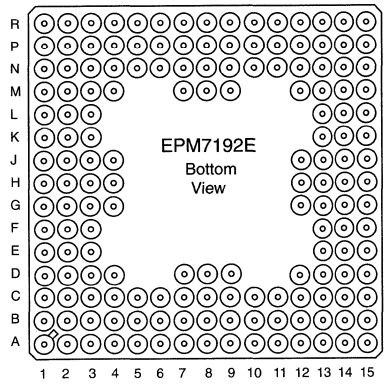
100-Pin PQFP



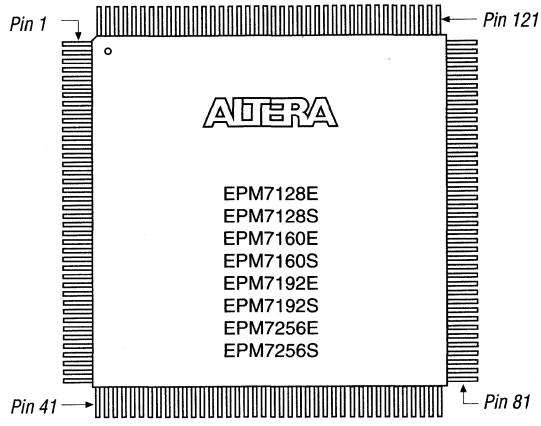
100-Pin TQFP

Figure 21. 160-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



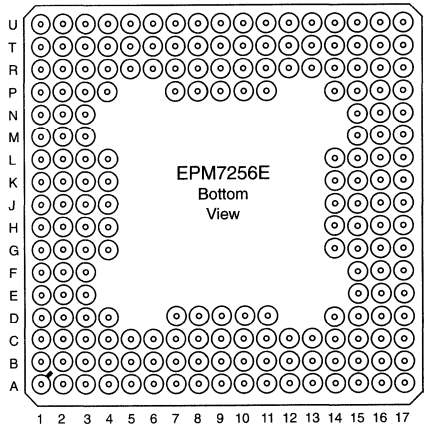
160-Pin PGA



160-Pin PQFP

Figure 22. 192-Pin Package Pin-Out Diagram

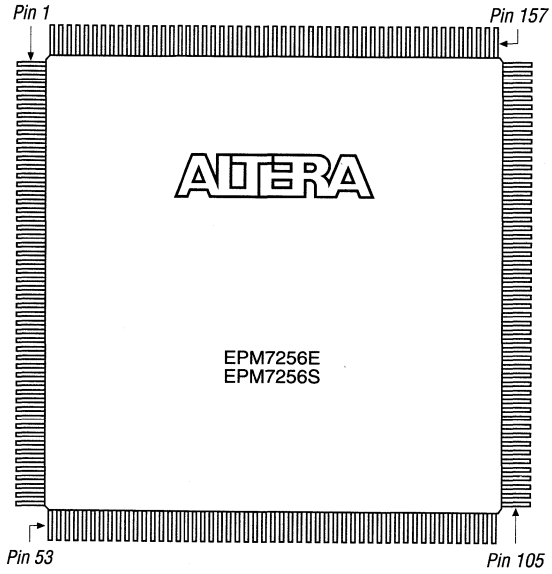
Package outline not drawn to scale.



192-Pin PGA

Figure 23. 208-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



208-Pin RQFP

Notes:

June 1996

FLASHlogic Programmable Logic Device Family Data Sheet


ALTERA
FLASHlogic
EPX880QC132-10
ALTERA
FLASHlogic
ALTERA
FLASHlogic
EPX8160QC208-10
PCI

FLASHlogic

Programmable Logic Device Family

June 1996, ver. 2 Data Sheet

Features...

- High-performance programmable logic device (PLD) family
  - SRAM-based logic with shadow FLASH memory elements fabricated on advanced CMOS technology
  - Logic densities from 1,600 to 3,200 usable gates (see Table 1)
  - Combinatorial speeds with t_{PD} as low as 10 ns
  - Counter frequencies of up to 80 MHz
- 8 to 16 logic array blocks (LABs) linked by a 100%-connectable programmable interconnect array (PIA) for improved fitting of complex designs
- 24V10 macrocell features available
  - Dual feedback on all I/O pins
  - Product-term allocation matrix supporting up to 16 product terms per macrocell
  - Programmable registers providing D, T, SR, and JK flipflop functionality with clear, preset, and clock controls
  - Fast 12-bit identity compare option
- Fully compliant with *PCI Local Bus Specification*, version 2.1

Table 1. FLASHlogic Device Features

Feature	EPX880	EPX8160
Usable gates	1,600	3,200
Maximum SRAM bits	10,240	20,480
Macrocells	80	160
Logic array blocks (LABs)	8	16
Package options (maximum user I/O pins)	84-pin PLCC (62) 132-pin PQFP (104)	208-pin PQFP (172)
t_{PD} (ns)	10	10
t_{CO} (ns)	6	6
f_{CNT} (MHz)	80	80

... and More Features

- LABs can be configured as either one of the following:
  - 24V10 logic block with 10 macrocells
  - 128 × 10 SRAM block
- 3.3-V or 5.0-V I/O on all devices (selectable in each LAB)
- Low power consumption (1 mA/MHz in standby mode; 1.5 to 2.5 mA/MHz in active mode)
- 84 to 208 pins available in plastic J-lead (PLCC) and plastic quad flat pack (PQFP) packages (see Table 1)
- Open-drain output option
- Joint Test Action Group (JTAG) IEEE 1149.1-compatible test port
  - Boundary-scan testing (BST) support
  - In-circuit reconfigurability (ICR) support
  - In-system programmability (ISP) support
- Programmable security bit for protection of proprietary designs
- Supported by industry-standard design and programming tools from Altera and other vendors

General Description

FLASHlogic devices are SRAM-based devices with shadow FLASH memory elements. Fabricated on advanced CMOS technology, FLASHlogic devices provide from 1,600 to 3,200 usable gates, pin-to-pin delays as fast as 10 ns, and counter speeds of up to 80 MHz. Table 2 shows the available speed grades for FLASHlogic devices.

Table 2. FLASHlogic Speed Grades

Device	Available Speed Grades	
	-10	-12
EPX880	✓	✓
EPX8160	✓	✓

FLASHlogic devices have a unique combination of features that is ideal for a variety of applications, including communications and bus interface controllers. They provide low power consumption and user-selectable 5.0-V and 3.3-V outputs, making FLASHlogic devices useful for mixed-voltage applications such as portable and embedded systems.

The FLASHlogic device architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. In addition, FLASHlogic devices easily integrate multiple programmable logic devices ranging from PALs, GALs, and 22V10s to MACH, pLSI, and FPGA devices. With speed, density, and I/O resources comparable to commonly used masked gate arrays, FLASHlogic devices are ideal for gate array prototyping and PC applications. In addition, FLASHlogic devices in the -10 speed grade are PCI-compliant.

FLASHlogic devices are available in plastic J-lead chip carrier (PLCC) and plastic quad flat pack (PQFP) packages.

FLASHlogic devices contain 8 to 16 LABs linked by a PIA. Each LAB can be defined as either a 24V10 logic block of 10 macrocells or a 128 × 10 SRAM block. When defined as a 24V10 logic block, all 10 macrocells have a programmable-AND/allocatable-OR array and a configurable register with independently programmable clock, clear, and preset functions. To build complex logic functions, product-term allocation allows up to 16 product terms for a single macrocell.

FLASHlogic devices provide dedicated pins compliant with the JTAG IEEE 1149.1-1990 specification. The JTAG pins support BST, ICR, and ISP. ICR and ISP offer the designer greater flexibility in prototyping new designs. These features make FLASHlogic devices ideal for applications in which the final configuration is not fixed.

FLASHlogic devices are supported by industry-standard PC- and workstation-based EDA tools, including the Altera PLDshell Plus development system. The MAX+PLUS II development software also provides programming and configuration support for FLASHlogic devices.

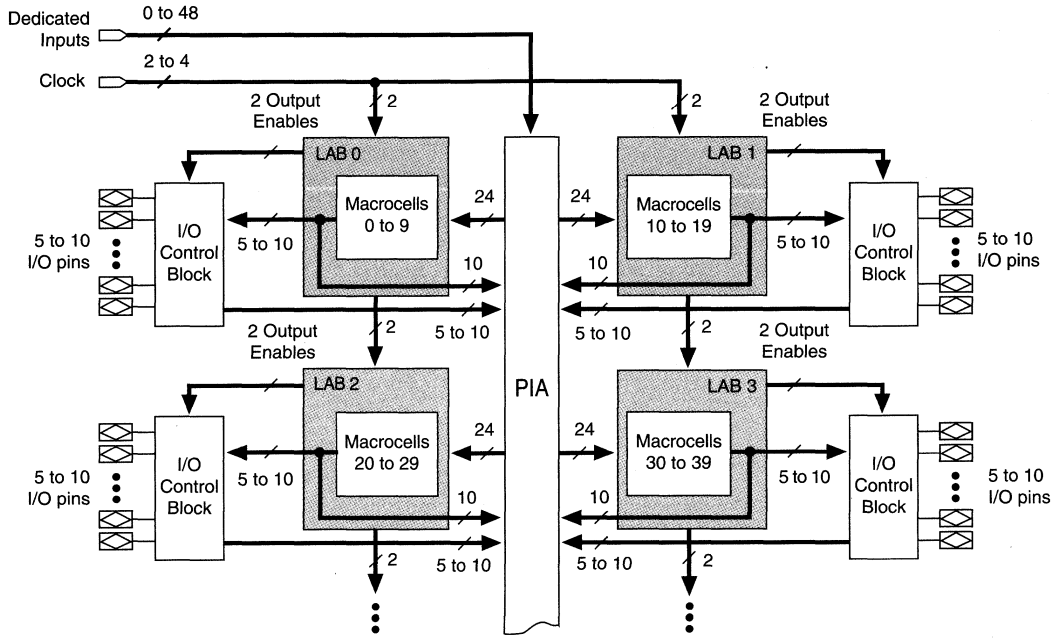
Functional Description

The FLASHlogic device architecture includes the following elements:

- Logic array blocks (LABs)
  - 24V10 configuration
  - SRAM configuration
- Programmable interconnect array (PIA)
- I/O control blocks

Figure 1 shows the block diagram of the FLASHlogic device architecture, which consists of LABs linked by a 100%-connectable PIA.

Figure 1. FLASHlogic Device Block Diagram



Logic Array Blocks

The FLASHlogic device architecture is based on the linking of high-performance, flexible logic array modules called logic array blocks (LABs). Each LAB can be configured as a 24V10 logic block or as a 128 × 10 SRAM block. The LABs are linked via the PIA, which is fed by all dedicated inputs, I/O pins, and either macrocells (in 24V10 configuration) or SRAM outputs (in SRAM configuration). Each LAB is fed by 24 signals from the PIA and 2 global clocks.

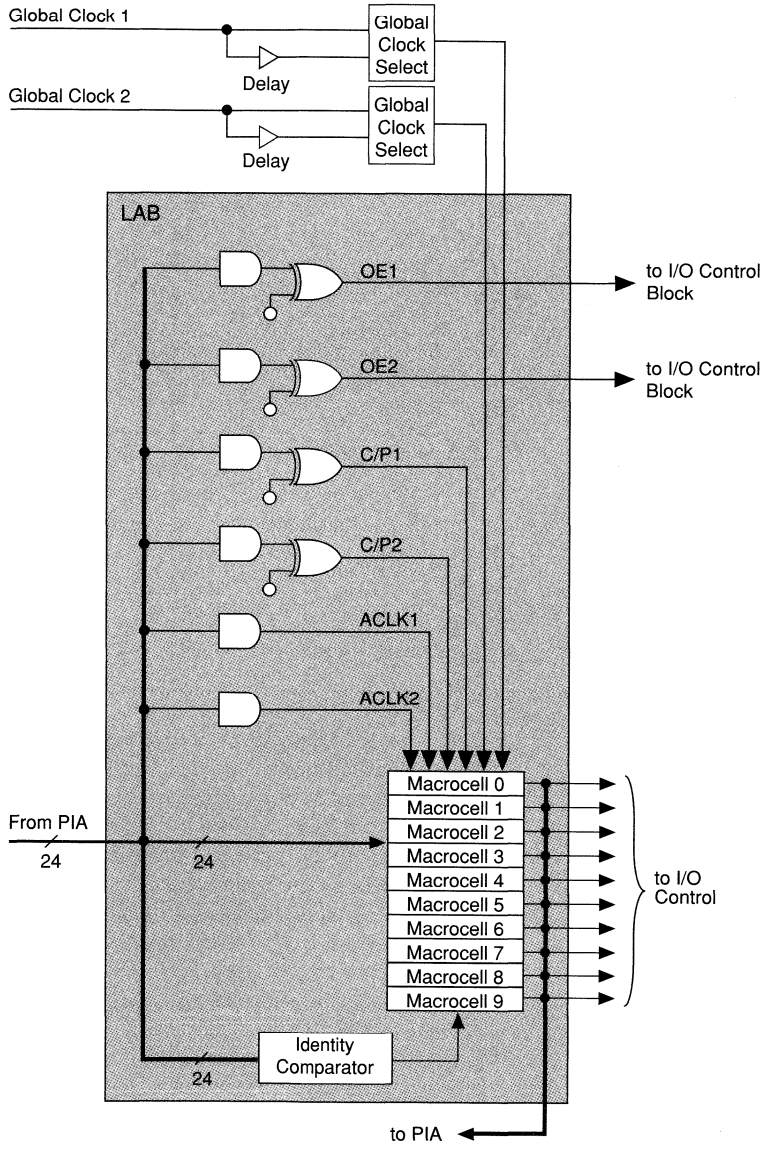
24V10 Configuration

When a LAB is configured as a 24V10 logic block, each block contains the following elements:

- 10 macrocells
- A 12-bit identity comparator
- 2 global clocks
- Control logic for array clocks, and for clear, preset and output enable signals

Figure 2 shows a diagram of a LAB configured as a 24V10 logic block.

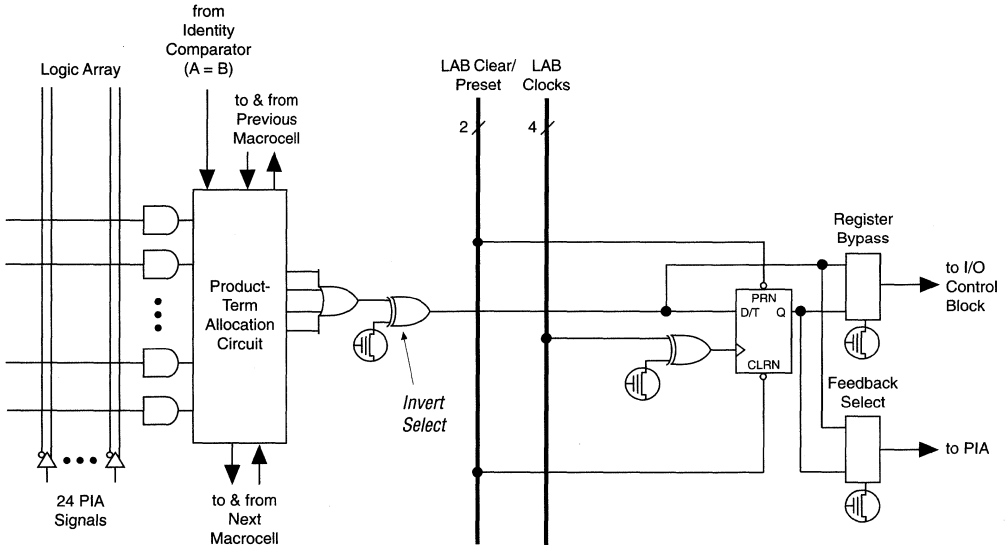
Figure 2. LAB in 24V10 Configuration



Macrocells

Each FLASHlogic macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term allocation circuit, and the programmable register. See Figure 3.

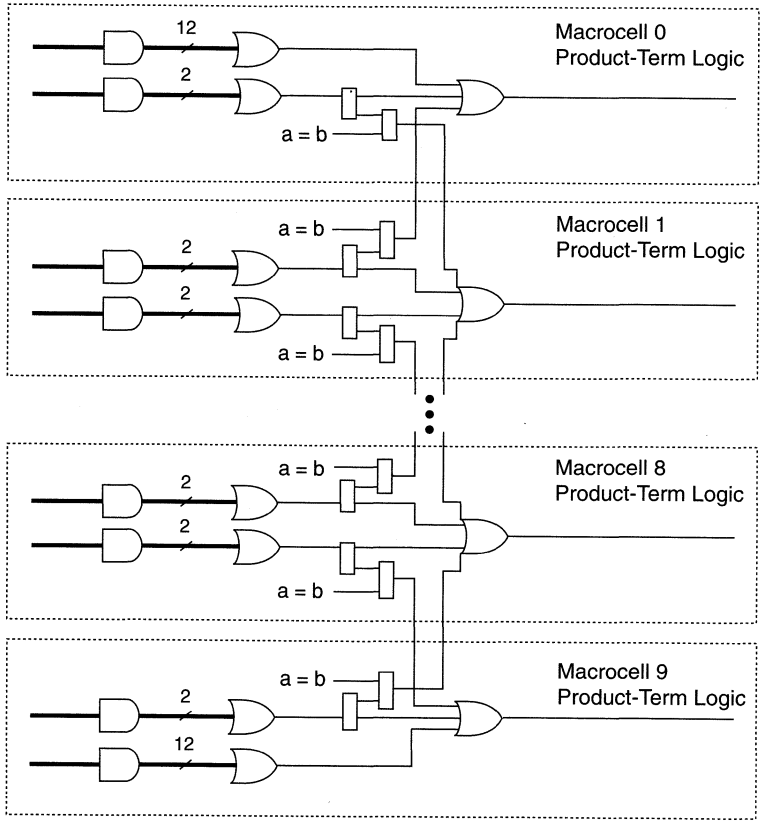
Figure 3. FLASHlogic Device Macrocell



Combinatorial logic is implemented in the logic array, which provides 2 sets of 2 product terms per macrocell. Macrocells 0 and 9 each have 14 product terms, and macrocells 2 through 8 each have 4 product terms. Each macrocell can borrow product terms from adjacent macrocells to increase the total number of product terms per macrocell up to a maximum of 8. The macrocells located at the ends of each LAB have additional product terms and support up to 16 product-term equations. The performance of each macrocell is uniform regardless of whether 2 or 16 product terms are used. Figure 4 shows the flexible product-term allocation circuit.

In registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock, preset, and clear controls. If necessary, the register can be bypassed for combinatorial operation.

Figure 4. LAB Product-Term Allocation



Each LAB supports four clock signals—two global clocks and two array clock signals. The EPX8160 has 4 global clock pins: CLK1 and CLK2 are for LABs 0 through 7, and CLK3 and CLK4 are for LABs 8 through 15. Global clocking is provided by either of two global clock signals or two delayed global clock signals. Array clocking is provided by two LAB product terms. Each register in the LAB can be clocked by the true or the complement of any two of the four clock signals.

Each programmable register can be clocked in three different modes:

- Global mode, by either of two global clock signals. This mode achieves the fastest clock-to-output performance.
- Delayed global mode, by either of two global clock signals with an added local delay (within the LAB).
- Array mode, by either of two array clocks implemented with a product term. In this mode, the register can be clocked by signals from buried macrocells.

These clocking modes give FLASHlogic devices increased timing flexibility, enabling the designer to vary the setup, hold, and clock-to-output times of each register. See Table 3. These clocking modes are particularly useful for integrating devices with short-setup-time microprocessors, such as a Pentium microprocessor.

Table 3. EPX880-10 & EPX8160-10 Sample Clocking Modes

Clock Mode	Setup Time	Hold Time	Clock-to-Output Time	Unit
Global	6.5	0	6	ns
Delayed global	5	2	8	ns
Array	2	5	12	ns

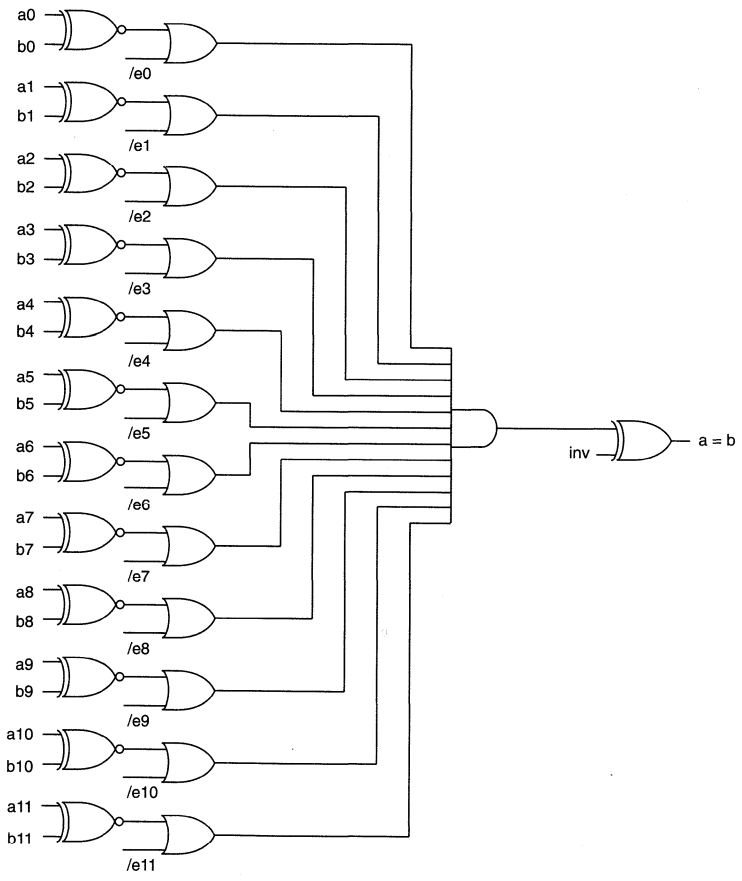
Each register also supports array preset and clear functions. These functions are driven by product terms and can be inverted. See Figure 2 on page 269 for a diagram of this logic.

Comparator Circuit

Each LAB also provides a comparator circuit that compares up to 12 pairs of inputs within the t_{PD} of the device. The product-term allocation matrix allows any one of the 10 macrocells in the LAB to use the output of the comparator circuit. See Figure 5.

Figure 5. 12-Bit Identity Compare Logic

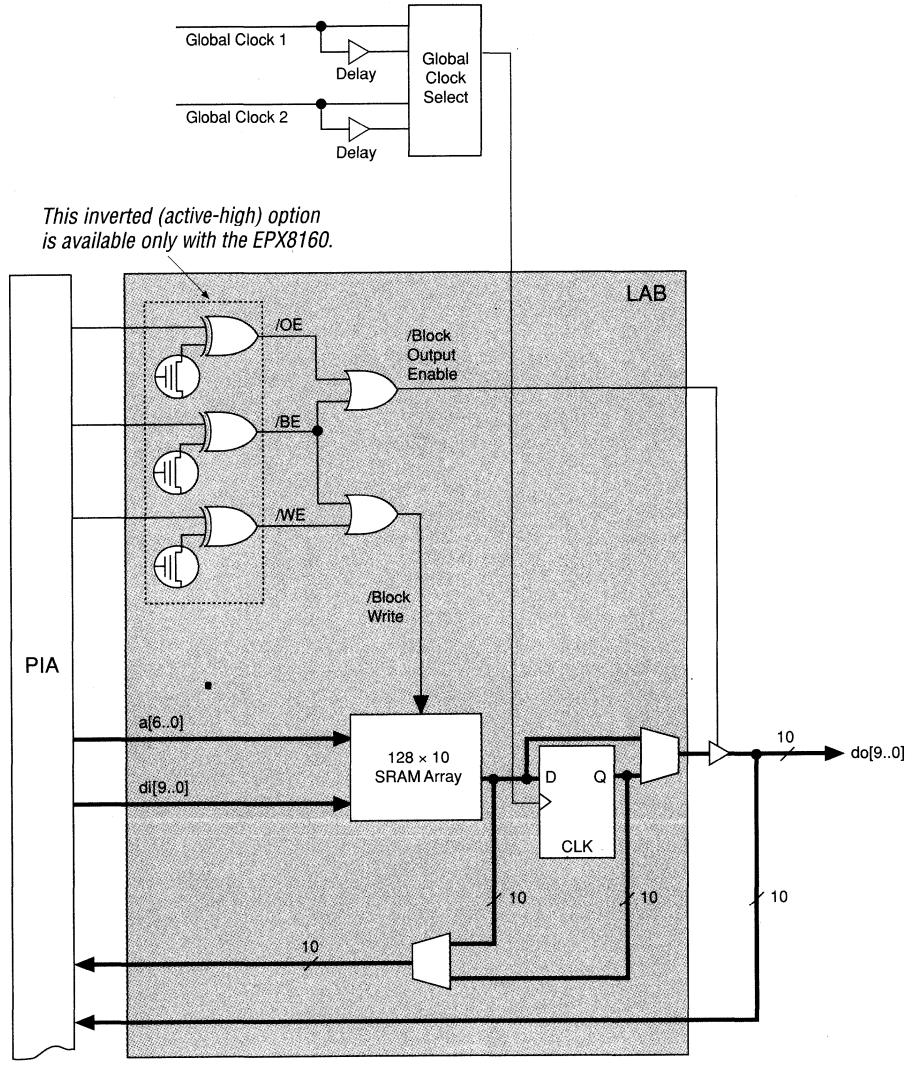
The an and bn signals represent a fan-in pair. The /en signal represents an architecture control bit.



SRAM Configuration

Each FLASHlogic LAB can be configured as a 128 × 10 (128 words by 10 bits) SRAM block, as shown in Figure 6. The SRAM block can be defined with either a bidirectional I/O data bus or with separate input and output data buses.

Figure 6. LAB in SRAM Configuration



The SRAM is accessed using a subset of the 24-signal fan-in from the PIA: 7 bits are for address information; 10 bits are for input data; 3 bits are for block enable (/BE), write enable (/WE), and output enable (/OE) controls, as shown in Table 4.

Table 4. SRAM Functions

Inputs			Cycle	I/O Pins
/BE	/WE	/OE		
1	X	X	None	Disabled
0	1	1	Read	Disabled
0	1	0	Read	Enabled
0	0	1	Write	Disabled
0	0	0	Write	Enabled

During power-up, the SRAM memory elements are initialized by on-chip, nonvolatile configuration cells. During operation, the SRAM contains a copy of the information contained in the nonvolatile configuration FLASH cells unless other data is written to these SRAM blocks. Therefore, the SRAM block can emulate read-only memory (ROM).

When an LAB is configured as SRAM, all product terms are used as SRAM blocks and cannot be used for regular macrocell logic. Multiple LABs can be cascaded to create larger SRAM blocks to increase the width or depth of the memory.

Programmable Interconnect Array

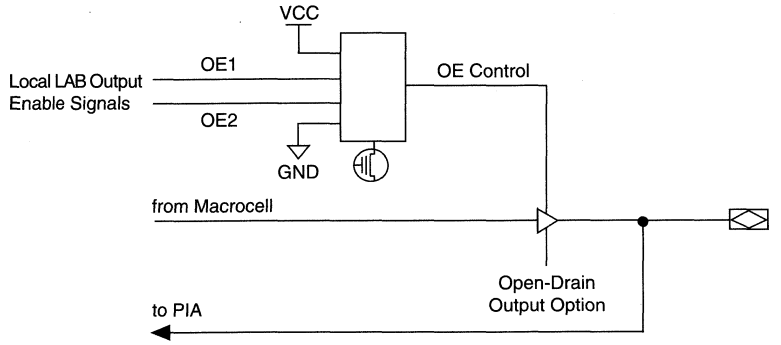
Signals are routed between LABs by the 100%-connectable programmable interconnect array (PIA). This global bus connects any signal source to any destination on the device. All dedicated pins, I/O pins, and macrocell outputs feed into the PIA and are accessible to all LABs. The high degree of connectivity and efficient resource management between LABs minimizes routing problems during design debugging.

The routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent. In contrast, the FLASHlogic PIA has a fixed delay. Therefore, the PIA eliminates skew between signals, making timing and performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is either individually controlled by one of the two local LAB output enable signals generated within each LAB or directly connected to GND or V_{CC}. Figure 7 shows the I/O control block for FLASHlogic devices.

Figure 7. FLASHlogic Device I/O Control Block



When the tri-state buffer control is connected to GND, the output is tri-stated (high-impedance), and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The FLASHlogic architecture provides dual I/O feedback in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Input Configuration

Device inputs, as well as I/O pins that are used as inputs, can be optimized for minimum standby current during either CMOS or TTL operation by using the `CMOS_LEVEL` keyword (for 5.0-V CMOS inputs) and the `TTL_LEVEL` keyword (for TTL or 3.3-V CMOS inputs) available in the PLDasm design language supported by PLDshell Plus. `TTL_LEVEL` is the default condition for PLDasm.

Output Configuration

FLASHlogic device outputs can be configured to meet a variety of system-level requirements.

3.3-V or 5.0-V Operation

The pins in an I/O control block can operate at 3.3 V or 5.0 V. This functionality enables the designer to mix 3.3-V outputs and 5.0-V inputs if the appropriate V_{CCO} pins are tied to a 3.3-V power supply. FLASHlogic devices require a V_{CC} of 5.0 V for normal operation. However, the V_{CCO} pin associated with each LAB pair can be connected to either a 5.0-V or 3.3-V power supply to control the output voltages of the I/O pins of that LAB pair. This feature allows FLASHlogic devices to be used in mixed-voltage systems. For example, the devices can be used as an interface between a 3.3-V CPU and 5.0-V peripheral logic.

Power sequencing is required when any or all LABs operate at 3.3-V levels. Thus, the voltage levels of the 5.0-V source must be greater than or equal to the 3.3-V source during power-up and power-down.

Open-Drain Output Option

FLASHlogic devices can be configured to provide an optional open-drain output for each I/O pin. If desired, complex equations can be implemented using multiple open-drain outputs with an externally supplied pull-up resistor to emulate an additional OR plane.

CMOS-Compatible Outputs

A weak pull-up resistor is provided for CMOS-compatible outputs. This resistor is always active in both 3.3-V and 5.0-V modes.

I/O Pull-Up Resistor

EPX8160 devices contain active-weak pull-up resistors on the I/O pins that hold the I/O at a logic high during power-up, reconfiguration, and erase/program cycles. This resistor is disabled during normal device operation to reduce power consumption. Dedicated inputs do not have active pull-up resistors.

High Drive Outputs

EPX880 and EPX8160 output buffers are designed specifically for applications requiring high drive current. These buffers enable the devices to drive a bus (including PCI), and concurrently provide 10-ns pin-to-pin performance, which eliminates the need for external buffers and their associated delays.

PCI Compliance

EPX880 and EPX8160 5.0-V output buffers are designed to meet the current-vs.-voltage specifications for PCI. EPX880-10 and EPX8160-10 devices also offer a predictable, 10-ns pin-to-pin propagation delay, a 6-ns clock-to-signal valid delay, and a 6.5-ns synchronous setup time to meet the timing demands of PCI applications. To support bidirectional PCI signals, two output enable product terms are provided in each LAB, for a total of 16 product terms for EPX880 devices and 32 product terms for EPX8160 devices.

Go to *Application Note 41 (PCI Bus Applications in Altera Devices)* for more information on using EPX8160 devices in PCI applications.

JTAG Operation

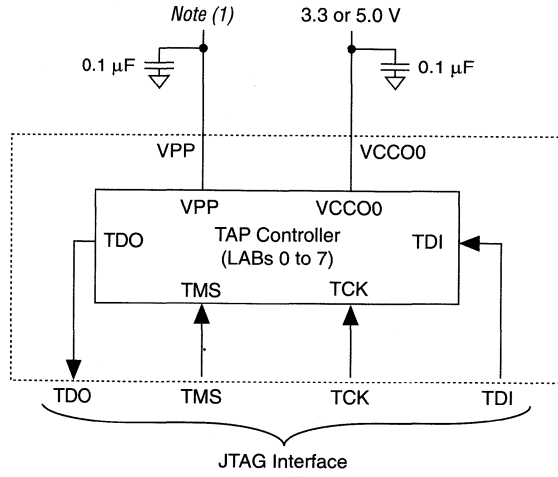
FLASHlogic devices support JTAG IEEE Std. 1149.1-1990 boundary-scan testing (BST). The JTAG BST architecture enables fault-isolation testing of board designs at the device level, enhances production testing and field repair, and is ideal for fault-tolerant applications.

FLASHlogic BST support consists of an instruction register, a data register, scan cells, and associated logic, all of which are accessed through the test access port (TAP). The TAP interface consists of three inputs—test mode select (TMS), test data input (TDI), and test clock input (TCK)—and one output, test data output (TDO).

An EPX880 device contains one JTAG TAP controller. An EPX8160 device contains two JTAG TAP controllers, each of which can operate independently or simultaneously for reconfiguration, reprogramming, and boundary-scan testing. Figure 8 shows the internal connection of the JTAG TAP controllers.

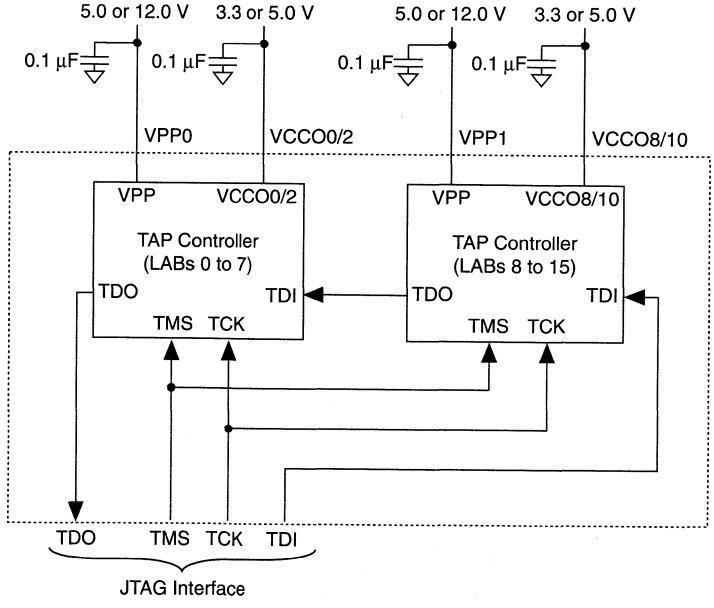
Figure 8. JTAG TAP Controller Connections

EPX880



Note:
(1) 5.0 or 12.0 V for EPX880 devices.

EPX8160



In FLASHlogic devices, the boundary-scan I/O pins are linked to form a shift register chain for all active pins. This chain provides a path that can be used to shift boundary-scan data into and out of the device.

For example, a continuity test can be performed between two JTAG devices on a circuit board by placing a known value on the output buffers of one device and observing the input buffers of the other device. The same technique can also be used to perform in-circuit functional testing of FLASHlogic devices for prototyping new system designs.

The 4-pin JTAG test interface is also used for standard programming, ICR, and ISP.

Boundary-Scan Instructions

The FLASHlogic boundary-scan instruction register (IR) supports the JTAG instructions used for the Program/Verify modes. See Table 5.

Table 5. Boundary-Scan Instructions

Name	Instruction Code (MSB..LSB)	Description
EXTEST	00000	The EXTEST instruction drives the output pins to the values contained in the boundary-scan cells. The instruction tests the external circuitry used for printed circuit board interconnects.
BYPASS	11111	The BYPASS instruction selects the one-bit bypass register (BPR) to be connected to TDI and TDO, which allows BST data to pass synchronously through the selected device to adjacent devices during normal device operation.
SAMPLE/PRELOAD	00001	The SAMPLE/PRELOAD instruction allows a snapshot of the values of the device pins to be captured and examined during normal device operation, and to preload data onto the device pins that are driven to the system circuit board when executing the EXTEST instruction.
IDCODE	00010	The IDCODE instruction selects the ID code register and places it between TDI and TDO, allowing the ID code to be serially shifted out of TDO.
UESCODE	10110	The UESCODE instruction selects the user electronic signature (UES) register and places it between TDI and TDO, allowing the UES register to be serially shifted out of TDO.
HIZ	11101	The HIZ instruction sets all I/O pins to a high-impedance state.

Go to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)* for more information about JTAG operation.

ICR & ISP

FLASHlogic devices support in-circuit reconfigurability (ICR). Using the 4-pin JTAG test port, a new configuration can be downloaded to the SRAM by simply shifting the new data into the device. Device reconfiguration can be repeated as many times as desired during prototyping. During ICR, all I/O pins on the device are tri-stated.

Once the design is finalized, it can be programmed into the nonvolatile shadow FLASH cells. FLASHlogic devices support in-system programmability (ISP), allowing devices to be programmed while mounted on a printed circuit board. ISP allows devices to be programmed in-system using the JTAG test port and the programming voltage pins (V_{PP}). FLASH-based devices can be programmed up to 100 times. During ISP, all I/O pins on the device are tri-stated.

During ICR and ISP, the I/O pins of FLASHlogic devices are tri-stated. In addition, the I/O pins for an EPX8160 device have a weak pull-up transistor. Refer to the "Pin Descriptions" on page 298 section of this data sheet for more information.

For more information on ICR and ISP, go to the following documents:

- *Product Information Bulletin 19 (ICR & ISP: In-Circuit Reconfigurability & In-System Programmability)*
- *Application Note 45 (Configuring FLASHlogic Devices)*
- *Application Brief 145 (Designing for In-System Programmability in MAX 7000S Devices)*

Design Security

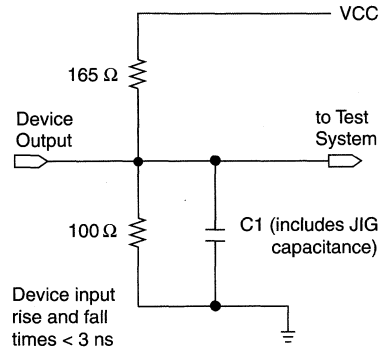
FLASHlogic devices contain a programmable security bit that controls access to the data programmed into the device. Once this security bit is set, the design cannot be read from the nonvolatile cells or the SRAM. The state of the nonvolatile security bit at power-up determines whether data programmed into the device can be accessed and changed by in-circuit reconfiguration.

Generic Testing

FLASHlogic devices are fully functionally tested. Complete testing of each programmable FLASH bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9. Test patterns can be used and erased during early stages of the device production flow.

Figure 9. FLASHlogic AC Test Conditions

Power-supply transients can affect AC measurements. For accurate measurements, avoid simultaneous transitions of multiple outputs. Do not perform threshold tests under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, they can significantly reduce observable noise immunity.



Software Support

FLASHlogic devices are supported by industry-standard PC- and workstation-based EDA tools, including the Altera PLDshell Plus development system and the FLASHlogic Download Cable. In addition, MAX+PLUS II provides programming and configuration support. See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book for more information.

Go to the *PLDshell Plus/PLDasm User's Guide* for information on programming and configuring FLASHlogic devices using PLDshell Plus.

Table 6 lists the third-party vendors that provide software support.

Table 6. Third-Party Software Support

Vendor	Software	Description
Data I/O Corporation	ABEL	Design software that describes and implements logic designs.
	Synario 2.0	Integrated text and graphic design and simulation environment.
Logical Devices, Inc.	CUPL	High-level, universal design software package.
MINC, Inc.	PLDesigner-XL(R)	Design tool for all types of programmable logic with automatic device selection, automatic partitioning, and functional simulation.
OrCAD Systems Corporation	PLD Tools (PLD) and Schematic Design Tool (SDT)	Design tools that Include schematic entry, test vector generation, and multiple forms of input.
	Verification and Simulation Tool (VST)	Series of software tools for performing timing-based simulation of designs.
Viewlogic Systems, Inc.	Workview, PRO Series, and Powerview	Integrated schematic capture and simulation environments.

Simulation models are provided by the following vendors:

- Synopsys Logic Modeling SmartModel—Device model support for behavioral simulation through a variety of simulators.
- Viewlogic ViewSim—Simulation model for Viewlogic verification tools.

Device Programming

FLASHlogic devices can be programmed with MAX+PLUS II software on 486- and Pentium-based PCs using an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. See the *Altera Programming Hardware Data Sheet* in this data book for more information.

FLASHlogic devices can also be programmed in-system with the MAX+PLUS II software using the BitBlaster serial download cable, and with the PLDshell Plus software using the Altera FLASHlogic Download Cable. Data I/O and other programming hardware manufacturers also provide programming support for FLASHlogic devices. See *Programming Hardware Manufacturers* in this data book for more information.

FLASHlogic Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (2)*	–2.0	7.0	V
V_{PP}	Programming supply voltage: EPX880 & EPX8160		–2.0	12.6	V
V_I	DC input voltage		–0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–10	85	° C
T_J	Junction temperature	Plastic packages, under bias		135	

FLASHlogic Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage: 5.0 V		4.75	5.25	V
V_{CCO}	Output supply voltage: 5.0 V		4.75	5.25	V
V_{CCO}	Output supply voltage: 3.3 V		3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CCO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			500	ns
t_F	Input fall time			500	ns

FLASHlogic Device DC Operating Conditions *Note (3)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V TTL high-level output current	EPX880 & EPX8160: I_{OH} = –16.0 mA DC, V_{CCO} = min., *Note (4)*	2.4		V
	5.0-V CMOS high-level output current	EPX880 & EPX8160: I_{OH} = –100 µA DC, V_{CCO} = min., *Note (4)*	V_{CCO} – 0.2		V
	3.3-V high-level output current	EPX880 & EPX8160: I_{OH} = –100 µA DC, V_{CCO} = min., *Note (4)*	V_{CCO} – 0.2		V
V_{OL}	5.0-V low-level output current	EPX880 & EPX8160: I_{OL} = 24 mA DC, V_{CCO} = min., *Note (4)*		0.45	V
	3.3-V low-level output current	EPX880 & EPX8160: I_{OL} = 12 mA DC, V_{CCO} = min., *Note (4)*		0.2	V
I_I	Input leakage current	V_{CCO} = max., GND < V_{IN} < V_{CCO}, *Note (5)*	–10	10	µA
I_{OZ}	Output leakage current	EPX880 & EPX8160: V_{CCO} = max., V_{OUT} = V_{CCO}	–50	50	µA
		EPX880 & EPX8160: V_{CCO} = max., V_{OUT} = GND	–100	100	µA
I_{SC}	Output short circuit current, *Note (6)*	V_{CCO} = max., V_{OUT} = 0.5 V	–30	–120	mA

FLASHlogic Device Programming Conditions *Notes (3), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PP}	Programming voltage: EPX880 & EPX8160		11.4	12	12.6	V
I_{PP1}	V_{PP} read current, IC current, or standby current	$V_{PP} > V_{CC}$		90	200	µA
		$V_{PP} \leq V_{CC}$		15	40	µA
I_{PP2}	V_{PP} programming or program verify current: EPX880 & EPX8160	$V_{PP} = V_{PPH}$ Programming in progress		30	60	mA
I_{PP3}	V_{PP} erase and erase verify current	$V_{PP} = V_{PPH}$		30	60	mA
E_{CNT}	Erase and reprogram count limit				100	–

FLASHlogic Device Capacitance *Notes (8), (9)*

Symbol	Parameter	Conditions	Typ	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 2 V, f = 1.0 MHz	10	12	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 2 V, f = 1.0 MHz	12	15	pF
C_{CLK}	Clock pin capacitance	V_{OUT} = 2 V, f = 1.0 MHz	15	18	pF
C_{VPP}	V_{PP} pin capacitance	f = 1.0 MHz	12	15	pF

FLASHlogic Device I_{CC} Supply Current Values *Note (8)*

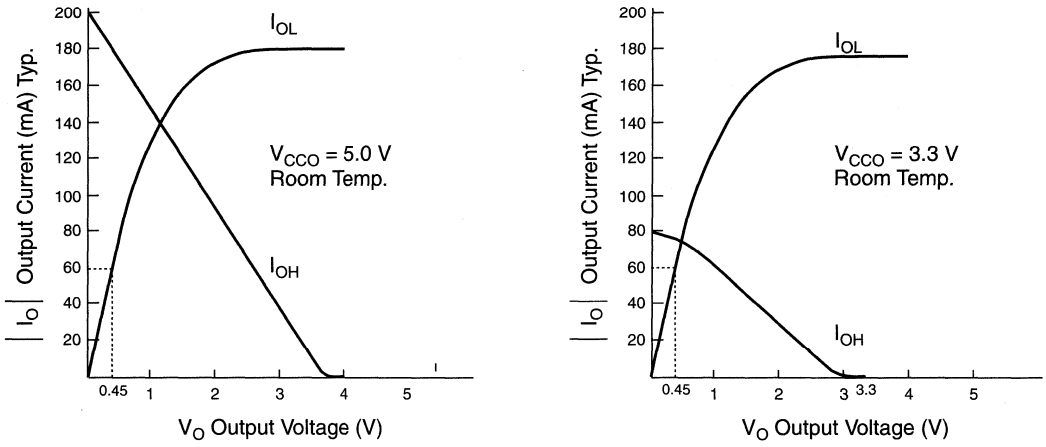
Symbol	Parameter	Conditions	EPX880	EPX8160	Unit
I_{CC1}	V_{CC} supply current (standby, typical)	V_{CC} = max., $V_{IN} = V_{CC}$ or GND, standby mode, *Note (10)*	1	1	mA
I_{CC}	V_{CC} supply current (active, typical)	$V_{IN} = V_{CC}$ or GND, no load, *Note (10)*	1.5	2.5	mA/ MHz

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods of less than 20 ns under no-load conditions.
(3) Operating conditions: T_A = 0° C to 70° C, V_{CC} = 5.0 V ± 5% for commercial use.
T_A = –40° C to 85° C, V_{CC} = 5.0 V ± 5% for industrial use.
(4) The I_{OH} parameter refers to high-level TTL output current. The I_{OL} parameter refers to low-level TTL output current.
(5) Input leakage current on JTAG pins is tested at ± 20 µA.
(6) No more than 1 output should be tested at a time. The duration of the test should not exceed 1 second.
(7) Typical values are for T_A = 25° C, V_{CC} = 5.0 V, V_{PP} = 12.0 V.
(8) Typical values are for T_A = 25° C, V_{CC} = 5.0 V.
(9) Capacitance is measured at 25° C, and is sample-tested only.
(10) Measured with a 20-bit, loadable, enabled, up/down counter programmed into each LAB pair.

Figure 10 shows the typical output drive characteristics for FLASHlogic devices.

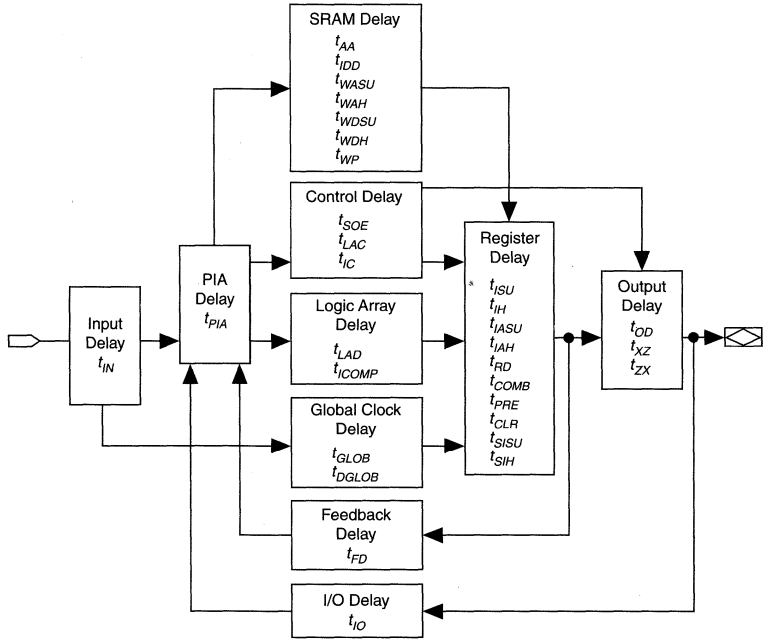
Figure 10. Output Drive Characteristics of FLASHlogic Devices



Timing Model

FLASHlogic devices have fixed internal delays that allow the user to determine the worst-case timing for any design. Device timing can be analyzed with a variety of industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 11.

Figure 11. FLASHlogic Timing Model



Industry-standard EDA tools provide timing simulation, point-to-point delay prediction, and detailed analysis for system-level performance evaluation. External timing parameters represent pin-to-pin timing delays. Switching waveforms for these timing parameters (including SRAM read and SRAM write cycles) are shown in Figure 12.

Go to *Application Note 79 (Understanding FLASHlogic Timing)* for more information on FLASHlogic timing parameters.

Figure 12. Switching Waveforms (Part 1 of 3)

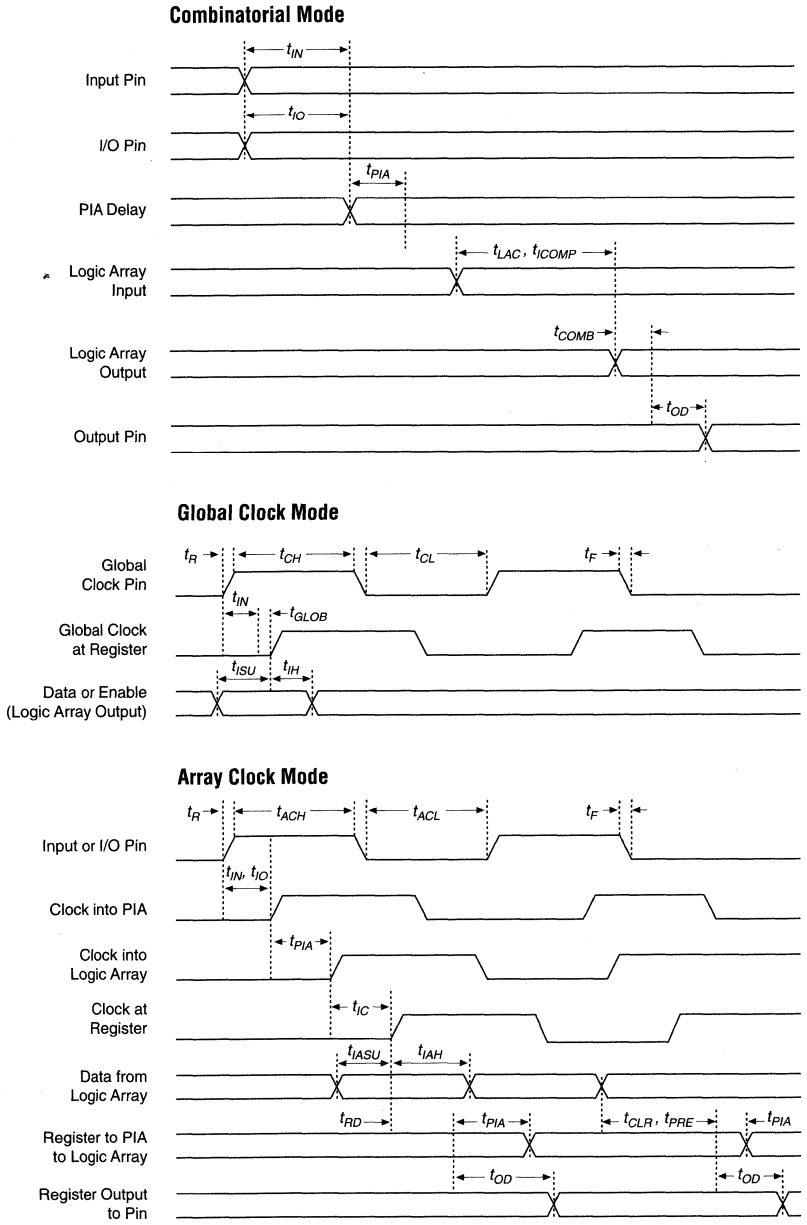
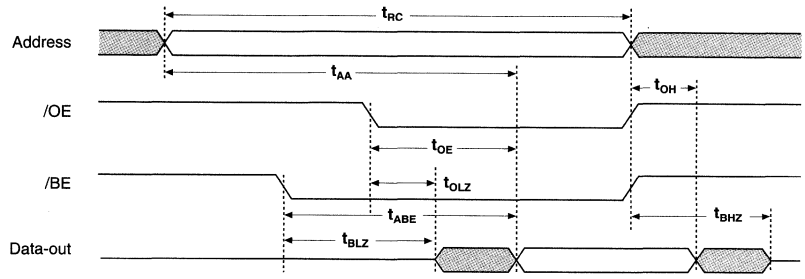
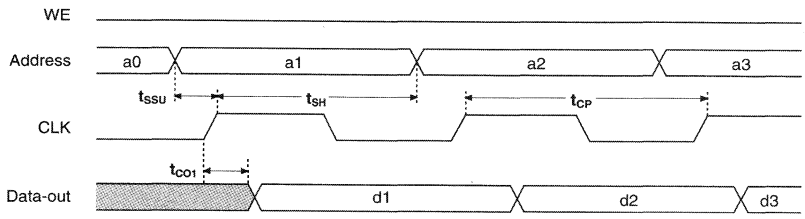


Figure 12. Switching Waveforms (Part 2 of 3)

SRAM Read Cycle



Register SRAM Read



SRAM Write Cycle 1 (/WE-Controlled Timing)

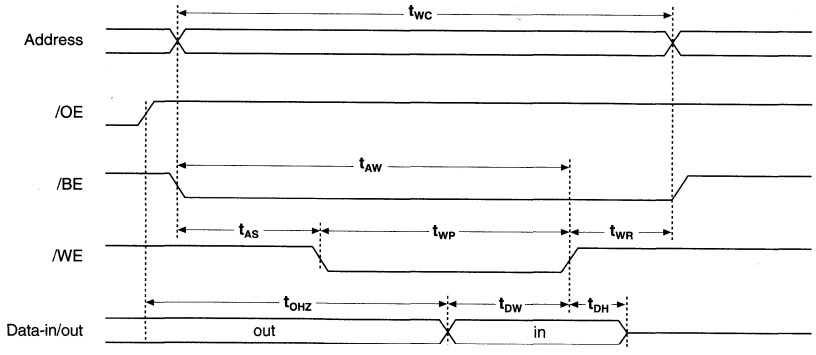
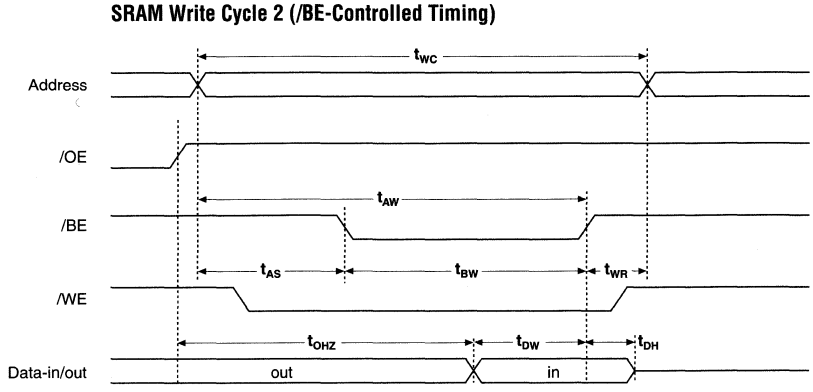


Figure 12. Switching Waveforms (Part 3 of 3)



FLASHlogic Device AC Operating Conditions

External Timing Parameters Combinatorial Mode			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to nonregistered output	C1 = 35 pF		10		12	ns
t_{PD2}	I/O to nonregistered output	CF = 35 pF		10		12	ns
t_{PZX}	Input or I/O to output enable	C1 = 35 pF		12		14	ns
t_{PXZ}	Input or I/O to output disable	C1 = 5 pF		12		14	ns
t_{CLR}	Array output clear time			15		18	ns
t_{COMP}	Comparator input or I/O feedback to output valid			10		12	ns

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Register Mode—Global Clock							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (1)*	100		83.3		MHz
t_{SU}	Input setup time		6.5		8		ns
t_{H}	Input hold time		0		0		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CP}	Clock period		10		12		ns
t_{CO}	Clock-to-output delay	C1 = 35 pF		6		7.5	
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (2)*	1		1		ns
t_{CNT}	Minimum clock period			12.5		15.5	
f_{CNT}	Maximum internal frequency	*Note (3)*	80		64.5		MHz

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Register Mode—Delayed Global Clock							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (1)*	95.2		80		MHz
t_{DSU}	Input setup time		5		6		ns
t_{DH}	Input hold time		2		2		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CP}	Clock period		10.5		12.5		ns
t_{DCO}	Clock-to-output delay	C1 = 35 pF		8		9.5	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (2)*	1		1		ns
t_{DCNT}	Minimum clock period			13		15.5	ns
f_{DCNT}	Maximum internal frequency	*Note (3)*	76.9		64.5		MHz

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Register Mode—Array Clock							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{AMAX}	Maximum frequency	*Note (1)*	80		66.7		MHz
t_{ASU}	Input setup time		2		2.5		ns
t_{AH}	Input hold time		5		6		ns
t_{ACH}	Clock high time		5		5.5		ns
t_{ACL}	Clock low time		5		5.5		ns
t_{ACP}	Clock period		12.5		15		ns
t_{ACO}	Clock-to-output delay	C1 = 35 pF		12		14.5	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (2)*	1		1		ns
t_{ACNT}	Minimum clock period			14		17	ns
f_{ACNT}	Maximum internal frequency	*Note (3)*	71.4		58.8		MHz

External TIming Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
SRAM Read *Note (4)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{RC}	Read cycle time		15		18		ns
t_{AA}	Address access time			15		18	ns
t_{ABE}	Block enable access time			12		15	ns
t_{OE}	Output enable to output delay	*Note (5)*		12		15	ns
t_{OH}	Output hold from address change		2		3		ns
t_{BLZ}	Block enable to output in low impedance	*Note (5)*	3		4		ns
t_{BHZ}	Block disable to output in high impedance	C1 = 5 pF *Note (5)*		12		15	ns
t_{OLZ}	Output enable to output in low impedance	*Note (5)*	3		4		ns

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Register SRAM Read—Global *Note (4)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{SSU}	Input or I/O setup time to clock		11		13		ns
t_{SH}	Input or I/O hold time from clock		0		0		ns
t_{CO1}	Clock-to-output delay			6		7.5	ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CP}	Clock period		15		17		ns

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Register SRAM Read—Delayed Global *Note (4)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{SSU}	Input or I/O setup time to clock		10		11		ns
t_{SH}	Input or I/O hold time from clock		2		2		ns
t_{CO1}	Clock-to-output valid			8		9.5	ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CP}	Clock period		15.5		17.5		ns

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
SRAM Write *Note (4)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{WC}	Write cycle time		15		18		ns
t_{BW}	Block enable to end of write		10		12		ns
t_{AW}	Address valid to end of write		13		15		ns
t_{AS}	Address set-up time		3		4		ns
t_{WP}	Write pulse width		10		12		ns
t_{WR}	Write recovery time		2		3		ns
t_{DW}	Data valid to end of write		10		12		ns
t_{DH}	Data hold time		2		3		ns
t_{OHZ}	Output disable to valid data-in	C1 = 5 pF *Notes (5), (6)*	12		15		ns

Internal Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Combinatorial & Register Mode							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad & buffer delay			1		1	ns
t_{IO}	I/O input pad & buffer delay			1		1	ns
t_{FD}	Register feedback delay			2		2	ns
t_{LAD}	Logic array delay			6		8	ns
t_{ICOMP}	Identity comparator delay			6		8	ns
t_{LAC}	Logic control array delay			8		10.5	ns
t_{SOE}	SRAM output enable delay			8		11.5	ns
t_{OD}	Output buffer & pad delay			1		1	ns
t_{ZX}	Output buffer enable delay			2		1.5	ns
t_{XZ}	Output buffer disable delay			2		1.5	ns
t_{ISU}	Register setup time, *Note (7)*		2.5 (3)		3.5 (3.5)		ns
t_{IH}	Register hold time, *Note (7)*		5 (4)		4.5 (4.5)		ns
t_{IASU}	Array clock register setup time		4		2.5		ns
t_{IAH}	Array clock register hold time		2.5		6		ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{GLOB}	Global clock delay			3		4.5	ns
t_{DGLOB}	Delayed global clock delay			5		6.5	ns
t_{IC}	Array clock delay			8		10.5	ns
t_{PRE}	Register preset time			4		4.5	ns
t_{CLR}	Register clear time			4		4.5	ns
t_{PIA}	Programmable interconnect array delay			1		1	ns

Internal Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
SRAM Mode							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{AA}	SRAM address access delay			11		14	ns
t_{DD}	SRAM data-in to data-out delay						ns
t_{WASU}	SRAM write address setup time		3		4		ns
t_{WAH}	SRAM write address hold time		2		3		ns
t_{WDSU}	SRAM write data setup time		10		12		ns
t_{WDH}	SRAM write data hold time		2		3		ns
t_{SISU}	SRAM internal register setup time, *Note (7)*		2 (3)		2.5 (2.5)		ns
t_{SIH}	SRAM internal register hold time		9		10.5		ns
t_{WP}	SRAM write pulse width		10		12		ns

Notes to tables:

(1) The f_{MAX} values represent the highest frequency for pipelined data.
(2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(3) Measured with a 10-bit loadable, enabled, up/down binary counter programmed into each LAB.
(4) Operating conditions: $T_A = 0°$ C to 70° C, $V_{CC} = 5.0$ V ± 5% for commercial use.
$T_A = -40°$ C to 85° C, $V_{CC} = 5.0$ V ± 5% for industrial use.
(5) These signals are measured at ± 0.5 V from steady-state voltage as driven by specified output load. Enable values are measured starting from 1.5 V on output.
(6) These specifications do not apply when separate data-in and data-out buses are used.
(7) When using the delay clock, calculate the timing with the values in parentheses.

Power Consumption

Supply power (P) versus frequency (f_{MAX} in MHz) for FLASHlogic devices is calculated with the following equation:

$$P = P_{INT} + P_{IO}$$

$$P = I_{CCACTIVE} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines provided in *Application Note 74 (Evaluating Power for Altera Devices)* in this data book.

The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = A \times MC + C \times MC \times f_{MAX} \times tog_{LC}$$

The parameters in this equation are as follows:

MC = Number of macrocells used in the design
f_{MAX} = Highest clock frequency to the device
tog_{LC} = Average ratio of logic cells toggling at each clock (typically 0.125)
A, C = Constants, shown in Table 7

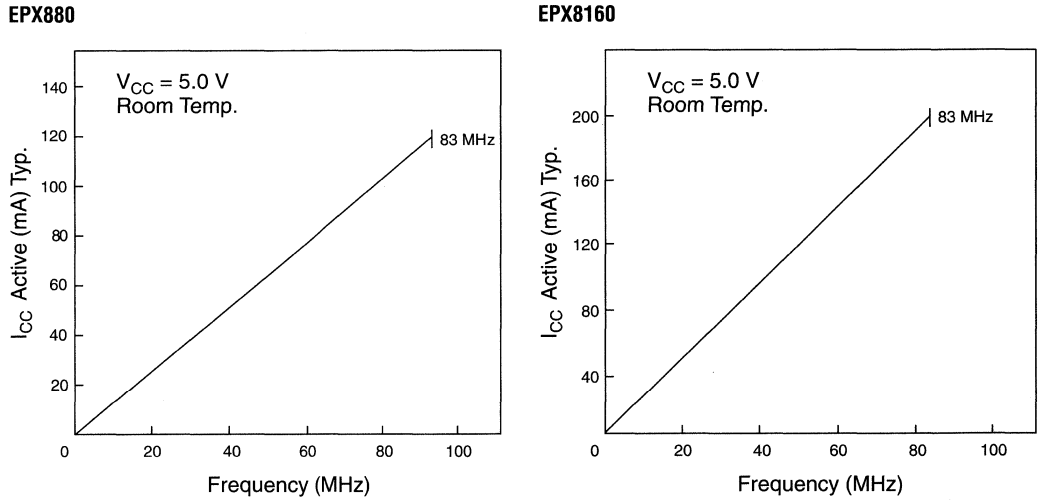
Table 7. FLASHlogic I_{CC} Equation Constants

Device	Constant A	Constant C
EPX880	0.0125	0.150
EPX8160	0.0062	0.125

The formula for calculating $I_{CCACTIVE}$ provides an estimate based on typical conditions using a typical pattern of a 20-bit, loadable, enabled, up/down binary counter with no output load in each pair of LABs. Actual I_{CC} values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 13 shows typical I_{CC} supply current versus frequency curves for FLASHlogic devices.

Figure 13. I_{CC} vs. Frequency for FLASHlogic Devices



Power-Up Cycle

Because V_{CC} rise times can vary significantly from one application to another, the device power-up cycle time varies. For a monotonic V_{CC} rise (1 ms/V minimum), the power-up cycle begins when V_{CC} reaches its minimum value and ends 100 µs after V_{CC} reaches the minimum value.

Internal power-up reset circuits ensure that all flipflops are reset to a logic low after the device has powered up. Also, the JTAG TAP controller is put into the test-logic-reset state. During power-up, EPX880 I/O pins are tri-stated; EPX8160 I/O pins are held high by an active-weak pull-up resistor. Upon completion of the power-up cycle, the outputs on an unprogrammed EPX880 device are placed in a high-impedance state. The outputs on an unprogrammed EPX8160 device are placed in a high-impedance state if V_{PP} is held below 2.0 V; the outputs are tri-stated if V_{PP} is held above 2.0 V.

Power-On Reset (POR)

FLASHlogic device configuration data can be reloaded from FLASH memory at any time by issuing a JTAG RESET instruction. For EPX880 and EPX8160 devices, the device configuration data from FLASH memory can also be reloaded by holding V_{PP} at a logic low (0.8 V maximum) for a minimum of 300 ns. By holding V_{PP} low during power-up, the power-up cycle can be delayed. The power-up cycle is completed within a delay of t_{RESET} after V_{PP} reaches 2.0 V (see Table 8). During normal operation, V_{PP} must be held at a logic high (2.4 V minimum) or tied to the V_{PP} supply (12.0 V) for EPX8160 devices.

Table 8. Reset Characteristics

Symbol	Parameter	Value	Conditions
t_{RESET}	JTAG reset time	150 µs maximum	Software control $V_{PP} \geq 2.0$ V

During reconfiguration or reprogramming, the JTAG RESET instruction is automatically issued by the PENGN or JED2JTAG software utilities provided with PLDshell Plus. It is not necessary to pull V_{PP} low for a reconfiguration or reprogram cycle.

For more information on configuring or programming FLASHlogic devices using the JTAG interface, go to the following documents:

- *Application Note 45 (Configuring FLASHlogic Devices)*
- *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices*

Pin Descriptions

Table 9 describes the pin names and descriptions for FLASHlogic devices.

Table 9. Pins Descriptions

Pin Name	Description
VCC, *Note (1)*	Supply voltage. Must be connected to 5.0 V.
GND	Ground connection.
VPP, *Note (1)*	Programming voltage. When programming FLASHlogic devices, 12.0 V must be supplied to this pin. When the EPX880 and EPX8160 devices are not in programming mode, VPP must be connected to VCC or VPP. The EPX880 and EPX8160 devices will reset themselves if VPP is held below 0.8 V for a minimum of 300 ns.
IN*n*	Input-only pins. These pins are not available in all packages. Unused inputs should be connected to VCC or GND.
TDI	Test data input. This pin is the boundary-scan serial data input to FLASHlogic devices. JTAG instructions and data are shifted into FLASHlogic devices on the TDI input pin on the rising edge of TCK. TDI can be left floating if unused.
TDO	Test data output. This is the boundary-scan serial data output from FLASHlogic devices. JTAG instructions and data are shifted out of FLASHlogic devices on the TDO output pin on the falling edge of TCK.
TCK	Test clock input. This input provides the boundary-scan clock for FLASHlogic devices. TCK clocks shift information and data into and out of the FLASHlogic devices during boundary-scan or programming modes. The maximum operating frequency of the BST clock is 8 MHz. TCK can be left floating if unused.
TMS	Test control input. This input provides the BST mode select for FLASHlogic devices. TMS can be left floating if unused.
VCCO*n*, *Note (1)*	Supply voltage for the outputs of the LABs. Connecting these pins to 5.0 V causes the LAB to output 5.0-V signals. Connecting these pins to 3.3 V causes the LAB to output 3.3-V signals. These pins must always be connected to the desired output drive voltage.
CLK*n*	Global clock signals.
I/O*n*	Pins configurable as inputs or outputs. Unused I/O pins should be connected as shown in the Report File. The reserved pins must be left unconnected. During ICR and ISP, the I/O pins of FLASHlogic devices are tri-stated. In addition, the I/O pins for an EPX8160 device has a weak pull-up transistor.

Note:
(1) Proper power decoupling is required on all power pins. A 0.1-µF decoupling capacitor is recommended between each power pin and ground.

Device Pin-Outs

Tables 10 through 13 show the pin names and numbers for the pins in each device FLASHlogic device package.

Table 10. EPX880 Pin-Outs

Pin Name	84-Pin PLCC	132-Pin PQFP
CLK1	3	118
CLK2	45	52
TDI	11	132
TDO	10	131
TMS	52	65
TCK	53	66
VPP	4	119
VCCIO0	25	117
VCCIO1	2	116
VCCIO2	24	19
VCCIO3	67	86
VCCIO4	25	20
VCCIO5	66	85
VCCIO6	44	50
VCCIO7	67	51
VCCINT	26, 68	21, 87
GND	17, 23, 29, 38, 46, 59, 65, 71, 80	11, 17, 18, 27, 44, 53, 59, 77, 83, 84, 93, 110, 125
Dedicated Inputs	–	1, 2, 3, 4, 5, 33, 34, 35, 36, 37, 38, 67, 68, 69, 70, 71, 99, 100, 101, 102, 103, 104

Table 11. EPX880 I/O Pin-Outs (Part 1 of 2) *Note (1)*

LAB	MC	84-Pin J-Lead	132-Pin PQFP	LAB	MC	84-Pin J-Lead	132-Pin PQFP
0	0	5	120	1	10	1	115
0	1	–	121	1	11	84	114
0	2	–	122	1	12	83	113
0	3	6	123	1	13	82	112
0	4	–	124	1	14	81	111
0	5	7	126	1	15	79	109
0	6	–	127	1	16	78	108
0	7	8	128	1	17	77	107
0	8	–	129	1	18	76	106
0	9	9	130	1	19	75	105
2	20	22	16	3	30	69	88
2	21	21	15	3	31	–	89
2	22	20	14	3	32	–	90
2	23	19	13	3	33	70	91
2	24	18	12	3	34	–	92
2	25	16	10	3	35	72	94
2	26	15	9	3	36	–	95
2	27	14	8	3	37	73	96
2	28	13	7	3	38	–	97
2	29	12	6	3	39	74	98

Table 11. EPX880 I/O Pin-Outs (Part 2 of 2) *Note (1)*

LAB	MC	84-Pin J-Lead	132-Pin PQFP	LAB	MC	84-Pin J-Lead	132-Pin PQFP
4	40	27	22	5	50	64	82
4	41	–	23	5	51	63	81
4	42	–	24	5	52	62	80
4	43	28	25	5	53	61	79
4	44	–	26	5	54	60	78
4	45	30	28	5	55	58	76
4	46	–	29	5	56	57	75
4	47	31	30	5	57	56	74
4	48	–	31	5	58	55	73
4	49	32	32	5	59	54	72
6	60	43	49	7	70	47	54
6	61	42	48	7	71	–	55
6	62	41	47	7	72	–	56
6	63	40	46	7	73	48	57
6	64	39	45	7	74	–	58
6	65	37	43	7	75	49	60
6	66	36	42	7	76	–	61
6	67	35	41	7	77	50	62
6	68	34	40	7	78	–	63
6	69	33	39	7	79	51	64

Note:
(1) A dash (–) indicates that the macrocell is buried.

Table 12. EPX8160 Pin-Outs

Pin Name	208-Pin PQFP
CLK1	184
CLK2	181
CLK3	77
CLK4	80
TDI	1
TDO	208
TMS	105
TCK	104
VPP0	182
VPP1	79
VCCIO0/VCCIO2	204
VCCIO1/VCCIO3	161
VCCIO4/VCCIO6	13
VCCIO5/VCCIO7	144
VCCIO8/VCCIO10	57
VCCIO9/VCCIO11	100
VCCIO12/VCCIO14	40
VCCIO13/VCCIO15	117
VCCINT	14, 39, 118, 143
GND	7, 15, 21, 32, 38, 46, 67, 78, 90, 111, 119, 125, 136, 142, 150, 171,183, 194
Dedicated Inputs	52, 53, 54, 55, 56, 59, 61, 63, 65, 69, 71, 73, 75, 82, 84, 86, 88, 92, 94, 96, 98, 101, 102, 103, 156, 157, 158, 159, 160, 163, 165, 167, 169, 173, 175, 177, 179, 186, 188, 190, 192, 196, 198, 200, 202, 205, 206, 207

Table 13. EPX8160 I/O Pin-Outs (Part 1 of 3) *Note (1)*

LAB	MC	208-Pin PQFP	LAB	MC	208-Pin PQFP
0	0	185	1	10	180
0	1	187	1	11	178
0	2	189	1	12	176
0	3	191	1	13	174
0	4	193	1	14	172
0	5	195	1	15	170
0	6	197	1	16	168
0	7	199	1	17	166
0	8	201	1	18	164
0	9	203	1	19	162
2	20	6	3	30	151
2	21	–	3	31	–
2	22	–	3	32	–
2	23	5	3	33	152
2	24	–	3	34	–
2	25	4	3	35	153
2	26	–	3	36	–
2	27	3	3	37	154
2	28	–	3	38	–
2	29	2	3	39	155
4	40	8	5	50	149
4	41	9	5	51	148
4	42	10	5	52	147
4	43	11	5	53	146
4	44	12	5	54	145
4	45	16	5	55	141
4	46	17	5	56	140
4	47	18	5	57	139
4	48	19	5	58	138
4	49	20	5	59	137

Table 13. EPX8160 I/O Pin-Outs (Part 2 of 3) *Note (1)*

LAB	MC	208-Pin PQFP	LAB	MC	208-Pin PQFP
6	60	26	7	70	131
6	61	–	7	71	–
6	62	–	7	72	–
6	63	25	7	73	132
6	64	–	7	74	–
6	65	24	7	75	133
6	66	–	7	76	–
6	67	23	7	77	134
6	68	–	7	78	–
6	69	22	7	79	135
8	80	76	9	90	81
8	81	74	9	91	83
8	82	72	9	92	85
8	83	70	9	93	87
8	84	68	9	94	89
8	85	66	9	95	91
8	86	64	9	96	93
8	87	62	9	97	95
8	88	60	9	98	97
8	89	58	9	99	99
10	100	47	11	110	110
10	101	–	11	111	–
10	102	–	11	112	–
10	103	48	11	113	109
10	104	–	11	114	–
10	105	49	11	115	108
10	106	–	11	116	–
10	107	50	11	117	107
10	108	–	11	118	–
10	109	51	11	119	106

Table 13. EPX8160 I/O Pin-Outs (Part 3 of 3) *Note (1)*

LAB	MC	208-Pin PQFP	LAB	MC	208-Pin PQFP
12	120	45	13	130	112
12	121	44	13	131	113
12	122	43	13	132	114
12	123	42	13	133	115
12	124	41	13	134	116
12	125	37	13	135	120
12	126	36	13	136	121
12	127	35	13	137	122
12	128	34	13	138	123
12	129	33	13	139	124
14	140	27	15	150	130
14	141	–	15	151	–
14	142	–	15	152	–
14	143	28	15	153	129
14	144	–	15	154	–
14	145	29	15	155	128
14	146	–	15	156	–
14	147	30	15	157	127
14	148	–	15	158	–
14	149	31	15	159	126

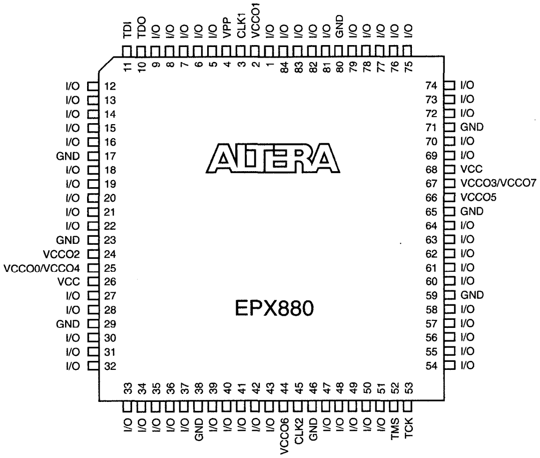
Note:
(1) A dash (–) indicates that the macrocell is buried.

Pin-Out Diagrams

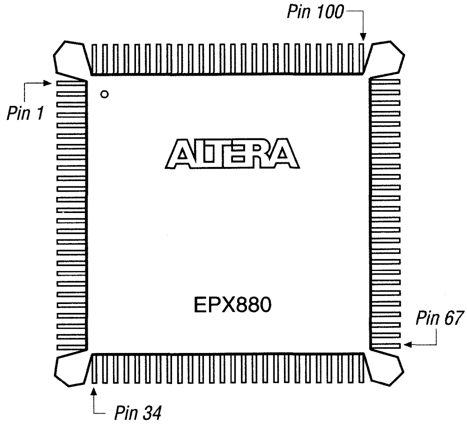
Figures 14 and 15 show the package pin-out diagrams for FLASHlogic devices.

Figure 14. EPX880 Package Pin-Out Diagram

Package outlines not drawn to scale. See Tables 10 and 11 for pin-out information.



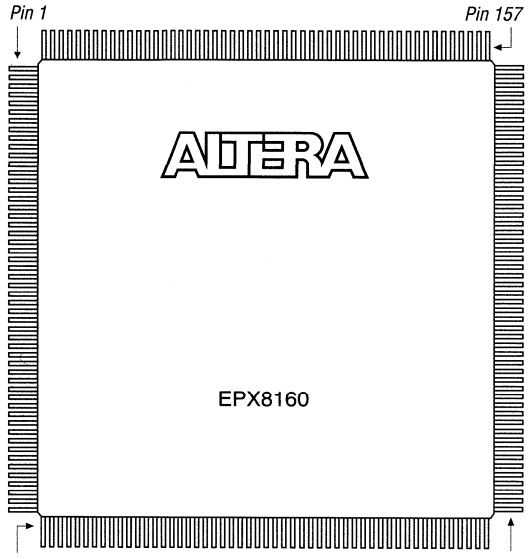
84-Pin J-Lead



132-Pin PQFP

Figure 15. EPX8160 Package Pin-Out Diagram

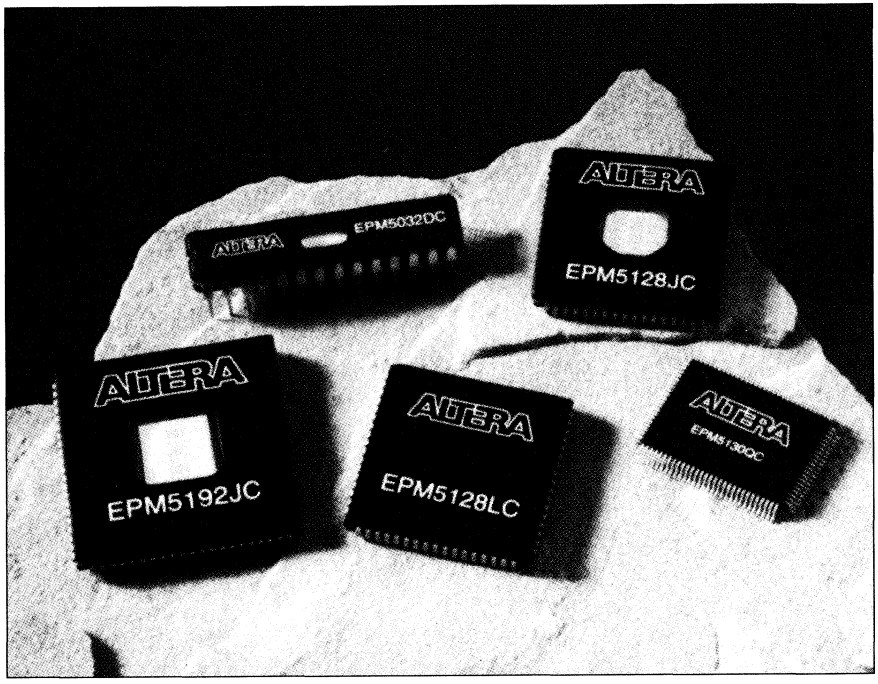
Package outline not drawn to scale. See Tables 12 and 13 for pin-out information.



Notes:

June 1996

MAX 5000 Programmable Logic Device Family Data Sheet


ALTERA
EPM5032DC
ALTERA
EPM5128JC
ALTERA
EPM5192JC
ALTERA
EPM5128LC
ALTERA
EPM5130QC

MAX 5000

Programmable Logic Device Family

June 1996, ver. 3 — Data Sheet

Features...

- Advanced Multiple Array MatriX (MAX) 5000 architecture combining speed and ease-of-use of PAL devices with the density of programmable gate arrays
- Complete family of high-performance, erasable CMOS EPROM EPLDs for designs ranging from fast 28-pin address decoders to 100-pin LSI custom peripherals
- 600 to 3,750 usable gates (see Table 1)
- Fast, 15-ns combinatorial delays and 83.3-MHz counter frequencies
- Configurable expander product-term distribution allowing more than 32 product terms in a single macrocell
- 28 to 100 pins available in DIP, J-lead, PGA, SOIC, and QFP packages
- Programmable registers providing D, T, JK, and SR flipflop functionality with individual clear, preset, and clock controls
- Programmable security bit for protection of proprietary designs
- Software design support featuring Altera's MAX+PLUS II development system on 486- or Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations

Table 1. MAX 5000 Device Features

Feature	EPM5032	EPM5064	EPM5128	EPM5130	EPM5192
Usable gates	600	1,250	2,500	2,500	3,750
Macrocells	32	64	128	128	192
Logic array blocks (LABs)	1	4	8	8	12
Expanders	64	128	256	256	384
Routing	Global	PIA	PIA	PIA	PIA
Maximum user I/O pins	24	36	60	68, 84	72
t_{PD} (ns)	15	25	25	25	25
t_{ASU} (ns)	4	4	4	4	4
t_{CO} (ns)	10	14	14	14	14
f_{CNT} (MHz)	76.9	50	50	50	50

...and More Features

- Programming support with Altera's Master Programming Unit (MPU) or programming hardware from other manufacturers
- Additional design entry and simulation support provided by EDIF, LPM, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar, Mentor Graphics, MINC, OrCAD, Synopsys, VeriBest, and Viewlogic

General Description

The MAX 5000 family combines innovative architecture and advanced process technologies to offer optimum performance, flexibility, and the highest logic-to-pin ratio of any general-purpose programmable logic device (PLD) family. The MAX 5000 family provides 600 to 3,750 usable gates, pin-to-pin delays as fast as 15 ns, and counter frequencies of up to 83.3 MHz. See Table 2.

Table 2. MAX 5000 Timing Parameter Availability

Device	Speed (t_{PD1})				
	15 ns	20 ns	25 ns	30 ns	35 ns
EPM5032	✓	✓	✓		
EPM5064			✓	✓	✓
EPM5128			✓	✓	✓
EPM5130			✓		✓
EPM5192			✓		✓

The MAX 5000 architecture supports 100% TTL emulation and high-density integration of multiple SSI, MSI, and LSI logic functions. For example, an EPM5192 device can replace over 100 74-series devices; it can integrate complete subsystems into a single package, saving board area and reducing power consumption. MAX 5000 EPLDs are available in a wide range of packages (see Table 3), including the following:

- Windowed ceramic and plastic dual in-line (CerDIP and PDIP)
- Windowed ceramic and plastic J-lead chip carrier (JLCC and PLCC)
- Windowed ceramic pin-grid array (PGA)
- Plastic small-outline integrated circuit (SOIC)
- Ceramic and plastic quad flat pack (CQFP and PQFP)

Table 3. MAX 5000 Pin Count & Package Options *Note (1)*

Device	Pin Count				
	28	44	68	84	100
EPM5032	CerDIP PDIP JLCC PLCC SOIC				
EPM5064		JLCC PLCC			
EPM5128			JLCC PLCC PGA		
EPM5130				JLCC PLCC	PGA PQFP
EPM5192				JLCC PLCC PGA	

Note:
(1) Contact Altera for up to date information on package availability.

MAX 5000 EPLDs have between 32 and 192 macrocells that are combined into groups called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register that provides D, T, JK, or SR operation with independent programmable clock, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with shareable expander product terms ("shared expanders") to provide more than 32 product terms per macrocell.

The MAX 5000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, IBM RISC System/6000 workstations.

For more information, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Functional Description

This section provides a functional description of MAX 5000 EPLDs, which have the following architectural features:

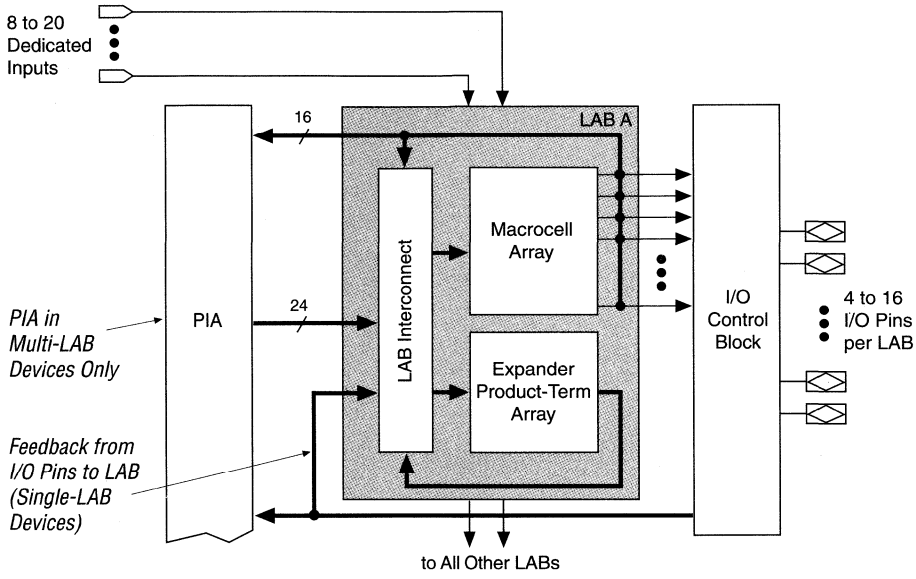
- Logic array blocks
- Macrocells
- Clocking options
- Expander product terms
- Programmable interconnect array
- I/O control blocks

The MAX 5000 architecture is based on the concept of linking high-performance, flexible logic array modules called logic array blocks (LABs). Multiple LABs are linked via the programmable interconnect array (PIA), a global bus that is fed by all I/O pins and macrocells. In addition to these basic elements, the MAX 5000 architecture includes 8 to 20 dedicated inputs, each of which can be used as a high-speed, general-purpose input. Alternatively, one of the dedicated inputs can be used as a high-speed global clock for registers.

Logic Array Blocks

MAX 5000 EPLDs contain 1 to 12 LABs. The EPM5032 has a single LAB, while the EPM5064, EPM5128, EPM5130, and EPM5192 contain multiple LABs. Each LAB consists of a macrocell array and an expander product-term array. See Figure 1. The number of macrocells and expanders in the arrays varies with each device.

Figure 1. MAX 5000 Architecture

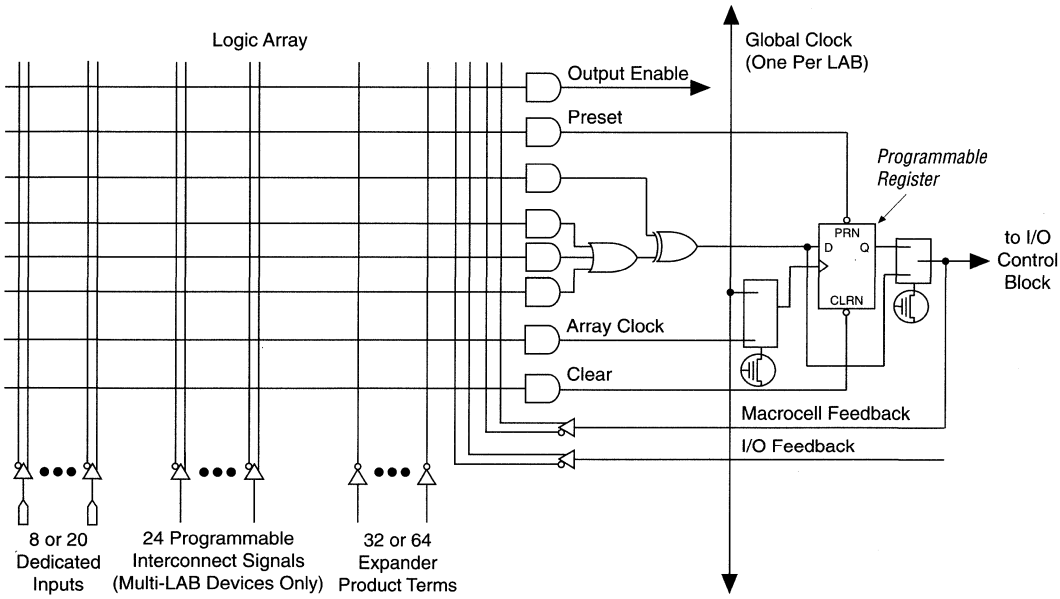


Macrocells are the primary resource for logic implementation. Additional logic capability is available from expanders, which can be used to supplement the capabilities of any macrocell. The expander product-term array consists of a group of unallocated, inverted product terms that can be used and shared by all macrocells in the LAB to create combinatorial and registered logic. These flexible macrocells and shareable expanders facilitate variable product-term designs without the inflexibility of fixed product-term architectures. All macrocell outputs are globally routed within an LAB via the LAB interconnect. The outputs of the macrocells also feed the I/O control block, which consists of groups of programmable tri-state buffers and I/O pins. In the EPM5064, EPM5128, EPM5130, and EPM5192 devices, multiple LABs are connected by a PIA. All macrocells feed the PIA to provide efficient routing for high-fan-in designs.

Macrocells

The MAX 5000 macrocell consists of a programmable logic array and an independently configurable register (see Figure 2). The register can be programmed to emulate D, T, JK, or SR operation, as a flow-through latch, or bypassed for combinatorial operation. Combinatorial logic is implemented in the programmable logic array, in which three product terms that are ORed together feed one input to an XOR gate. The second input to the XOR gate is used for complex XOR arithmetic logic functions and for De Morgan's inversion. The output of the XOR gate feeds the programmable register or bypasses it for combinatorial operation.

Figure 2. MAX 5000 Device Macrocell



Additional product terms—called secondary product terms—are used to control the output enable, preset, clear, and clock signals. Preset and clear product terms drive the active-low asynchronous preset and asynchronous clear inputs to the configurable flipflop. The clock product term allows each register to have an independent clock and supports positive- and negative-edge-triggered operation. Macrocells that drive an output pin can use the output enable product term to control the active-high tri-state buffer in the I/O control block.

The MAX 5000 macrocell configurability makes it possible to efficiently integrate complete subsystems into a single device.

Clocking Options

Each LAB supports either global or array clocking. Global clocking is provided by a dedicated clock signal (CLK) that offers fast clock-to-output delay times. Since each LAB has one global clock, all flipflop clocks within the LAB can be positive-edge-triggered from the CLK pin. If the CLK pin is not used as a global clock, it can be used as a high-speed dedicated input.

In the array clocking mode, each flipflop is clocked by a product term. Any input pin or internal logic can be used as a clock source. Array clocking allows each flipflop to be configured for positive- or negative-edge-triggered operation, giving the macrocell increased flexibility. Systems that require multiple clocks are easily integrated into MAX 5000 EPLDs.

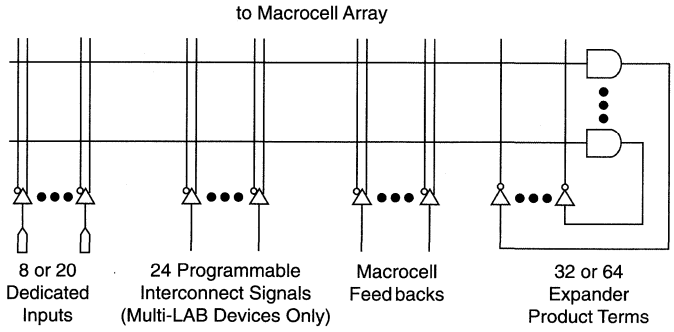
Each flipflop in an LAB can be clocked by a different array-generated clock; however, global and array clocking modes cannot be mixed in the same LAB.

Expander Product Terms

While most logic functions can be implemented with the product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although additional macrocells can be used to supply the needed logic resources, the MAX 5000 architecture can also use shared expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Each LAB has 32 shared expanders (except for the EPM5032 device, which has 64). The expanders can be viewed as a pool of uncommitted product terms. The expander product-term array (see Figure 3) contains unallocated, inverted product terms that feed the macrocell array. Expanders can be used and shared by all product terms in the LAB. Wherever extra logic is needed (including register control functions), expanders can be used to implement the logic. These expanders provide the flexibility to implement register- and product-term-intensive designs in MAX 5000 EPLDs.

Figure 3. Expander Product Terms



Expanders are fed by all signals in the LAB. One expander can feed all macrocells in the LAB or multiple product terms in the same macrocell. Since expanders also feed the secondary product terms of each macrocell, complex logic functions can be implemented without using additional macrocells. Expanders can also be cross-coupled to build additional flipflops, latches, or input registers. A small delay (t_{SEXP}) is incurred when shared expanders are used.

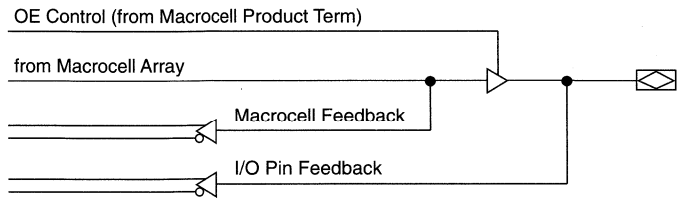
Programmable Interconnect Array

The higher-density MAX 5000 devices—EPM5064, EPM5128, EPM5130, and EPM5192—use a programmable interconnect array (PIA) to route signals between the various LABs. The PIA, which is fed by all macrocell and I/O pin feedbacks, routes only the signals required for implementing logic in an LAB. While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 5000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

Each LAB has an I/O control block that allows each I/O pin to be individually configured for input, output, or bidirectional operation. See Figure 4. The I/O control block is fed by the macrocell array. A dedicated macrocell product term controls a tri-state buffer, which drives the I/O pin.

Figure 4. I/O Control Block



The MAX 5000 architecture provides dual I/O feedback in which macrocell and I/O pin feedbacks are independent, allowing maximum flexibility. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic. Using an I/O pin as an input in single-LAB devices reduces the number of available expanders by two. In multi-LAB devices, I/O pins feed the PIA directly.

Design Security

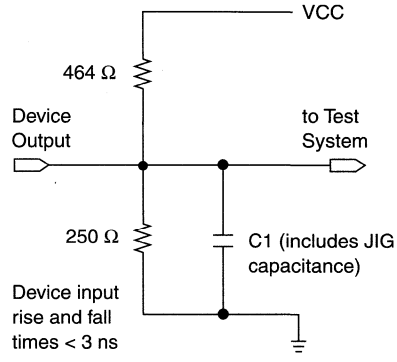
All MAX 5000 EPLDs contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM cells is invisible. The security bit that controls this function, as well as all other program data, is reset when an EPLD is erased.

Generic Testing

MAX 5000 EPLDs are fully functionally tested. Complete testing of each programmable EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those in Figure 5.

Figure 5. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Test patterns can be used and then erased during early stages of the device production flow. EPROM-based EPLDs in one-time-programmable windowless packages also contain on-board logic test circuitry to allow verification of function and AC specifications during the production flow.

Device Programming

All MAX 5000 EPLDs can be programmed on 486- and Pentium-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU checks continuity to ensure adequate electrical contact between the adapter and the device.

For more information, see *Altera Programming Hardware Data Sheet* in this data book.

MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test a programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 5000 EPLD with the simulation results. (This feature requires a device adapter with the "PLM-" prefix.)

Data I/O and other programming hardware manufacturers also offer programming support for Altera devices.

For more information, see *Programming Hardware Manufacturers* in this data book.

QFP Carrier & Development Socket

MAX 5000 devices in 100-pin QFP packages are shipped in special plastic carriers to protect the fragile QFP leads. Each carrier can be used with a prototype development socket and programming hardware available from Altera or Data I/O. This carrier technology makes it possible to program, test, erase, and reprogram devices without exposing the leads to mechanical stress.

For detailed information and carrier dimensions, refer to the *QFP Carrier & Development Socket Data Sheet* in this data book.

MAX 5000 Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	135	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		Plastic packages, under bias		135	° C

MAX 5000 Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (3), (4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

MAX 5000 Device DC Operating Conditions *Note (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (3)*	2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (6)*	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC, *Note (6)*			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA

EPM5032 MAX 5000 Device Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

EPM5064, EPM5128, EPM5130 & EPM5192 MAX 5000 Device Capacitance

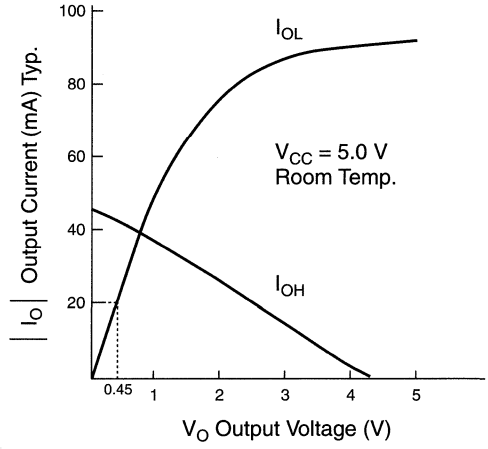
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range versions.
(4) Maximum V_{CC} rise time for MAX 5000 devices is 10 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.

Figure 6 shows typical output drive characteristics of MAX 5000 devices.

Figure 6. Output Drive Characteristics of MAX 5000 Devices

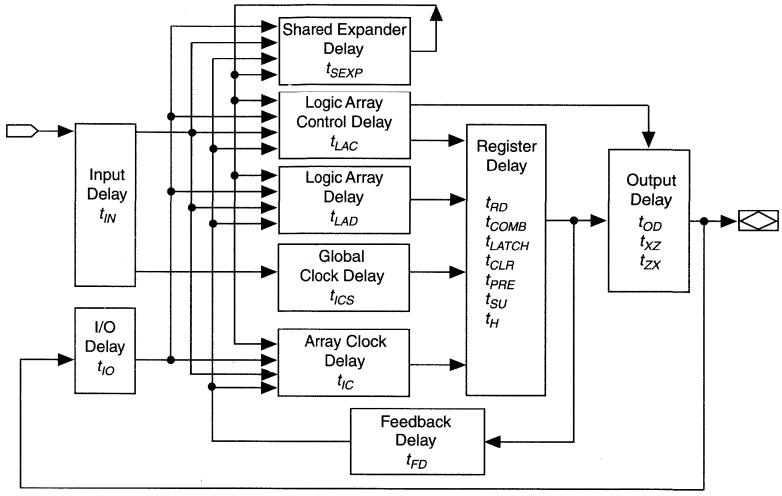


Timing Model

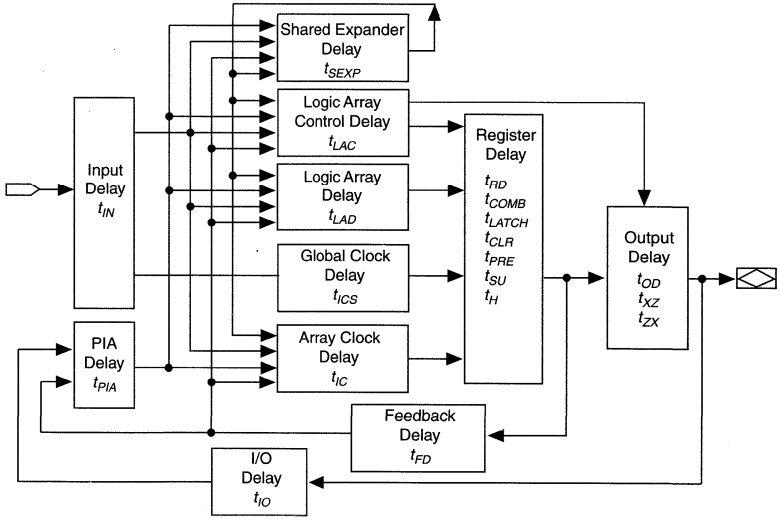
MAX 5000 EPLD timing can be analyzed with the MAX+PLUS II software, with a variety of other industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 7. MAX 5000 EPLDs have fixed internal delays that allow the user to determine the worst-case timing for any design. MAX+PLUS II provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 7. MAX 5000 Timing Model

Single-LAB EPLDs



Multi-LAB EPLDs



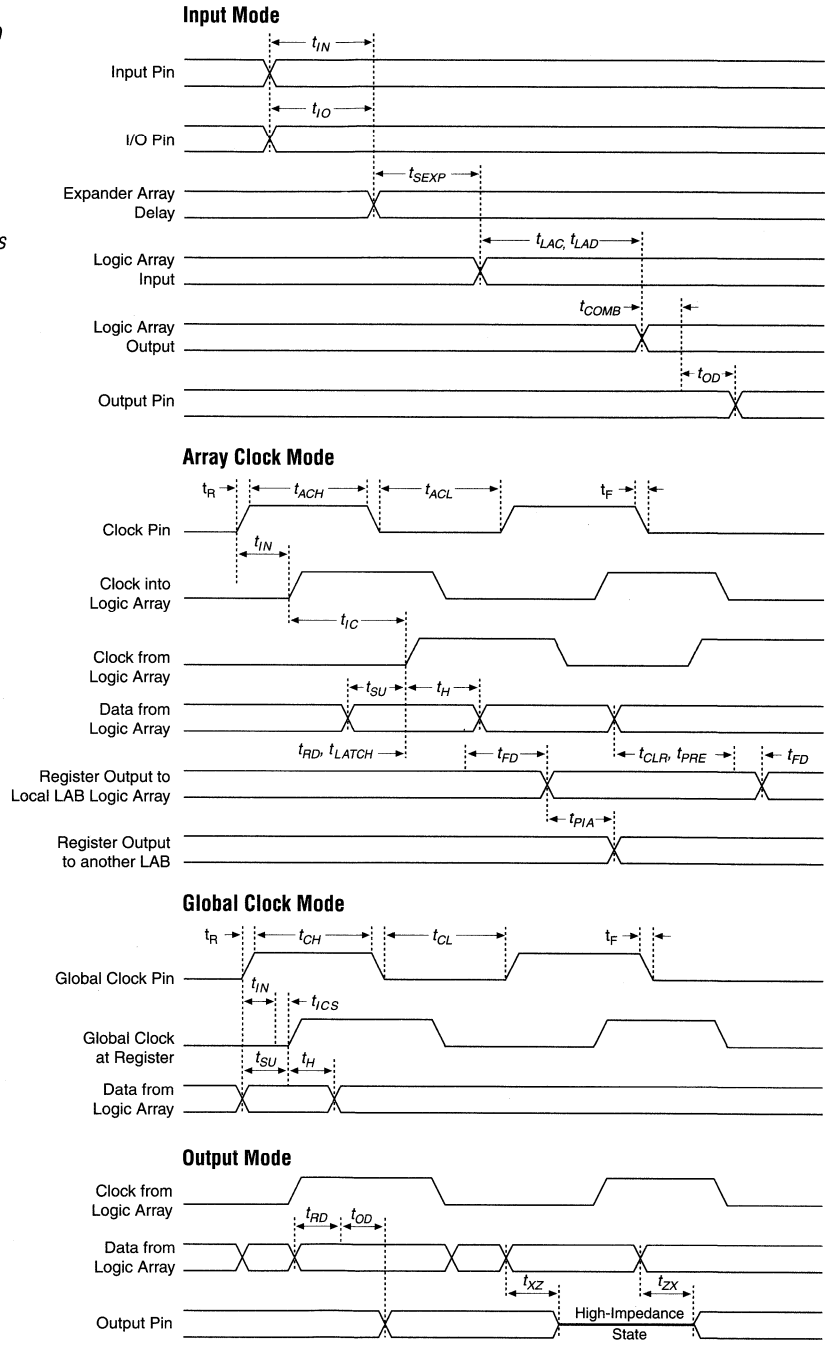
Timing information can be derived from the timing model and parameters for a particular EPLD. External timing parameters are calculated with the sum of internal parameters and represent pin-to-pin timing delays. Figure 8 shows the internal timing relationship for internal and external delay parameters.

For more information on EPLD timing, refer to *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book.

Figure 8. Switching Waveforms

In multi-LAB EPLDs, I/O pins that are used as inputs traverse the PIA.

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



EPM5032 AC Operating Conditions *Note (1)*

External Timing Parameters			EPM5032-15		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20		25	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		15		20		25	ns
t_{SU}	Global clock setup time		9		12		15		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		10		12		15	ns
t_{CH}	Global clock high time		6		7		8		ns
t_{CL}	Global clock low time		6		7		8		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		5		6		8		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		18		22	ns
t_{ACH}	Array clock high time	*Note (3)*	6		7		9		ns
t_{ACL}	Array clock low time		7		9		11		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(2)*	1		1		1		ns
t_{CNT}	Min. global clock period			13		16		20	ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	76.9		62.5		50		MHz
t_{ACNT}	Min. array clock period			13		16		20	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	76.9		62.5		50		MHz
f_{MAX}	Max. clock frequency	*Note (5)*	83.3		71.4		62.5		MHz

Internal Timing Parameters *Note (6)*			EPM5032-15		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		5		7	ns
t_{IO}	I/O input pad and buffer delay			3		5		7	ns
t_{SEXP}	Expander array delay			8		10		15	ns
t_{LAD}	Logic array delay			7		10		13	ns
t_{LAC}	Logic control array delay			4		4		4	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		4	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		7		7		7	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		7	ns
t_{SU}	Register setup time		4		4		5		ns
t_{LATCH}	Flow-through latch delay			1		1		1	ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{H}	Register hold time		5		8		10		ns
t_{IC}	Array clock delay			7		8		10	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		1	ns
t_{PRE}	Register preset time			5		6		9	ns
t_{CLR}	Register clear time			5		6		9	ns

EPM5064, EPM5128, EPM5130 & EPM5192 AC Operating Conditions *Note (1)*

External Timing Parameters			EPM5064-1 EPM5128-1 EPM5130-1 EPM5192-1		EPM5064-2 EPM5128-2		EPM5064 EPM5128 EPM5130 EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (3)*	11		14		16		ns
t_{ACL}	Array clock low time	*Note (3)*	9		11		14		ns
t_{CNT}	Min. global clock period			20		25		30	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (2)*	2		2		2		ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	50		40		33.3		MHz
t_{ACNT}	Min. array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	50		40		33.3		MHz
f_{MAX}	Max. clock frequency	*Note (3)*	62.5		50		40		MHz

Internal Timing Parameters *Note (6)*			EPM5064-1 EPM5128-1 EPM5130-1 EPM5192-1		EPM5064-2 EPM5128-2		EPM5064 EPM5128 EPM5130 EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{SEXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Programmable interconnect array delay			14		16		20	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization. This parameter applies for both global and array clocking.

(3) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.

(4) For EPM5032 devices, this parameter is measured with a 32-bit counter programmed into each LAB. For EPM5064, EPM5128, EPM5130, and EPM5192 devices, this parameter is measured with a 16-bit counter programmed into each LAB. I_{CC} is characterized at 0° C.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

(6) For information on internal timing parameters, refer to *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book.

Figure 9 shows typical supply current versus frequency for MAX 5000 devices.

Figure 9. I_{CC} vs. Frequency for MAX 5000 Devices (Part 1 of 2)

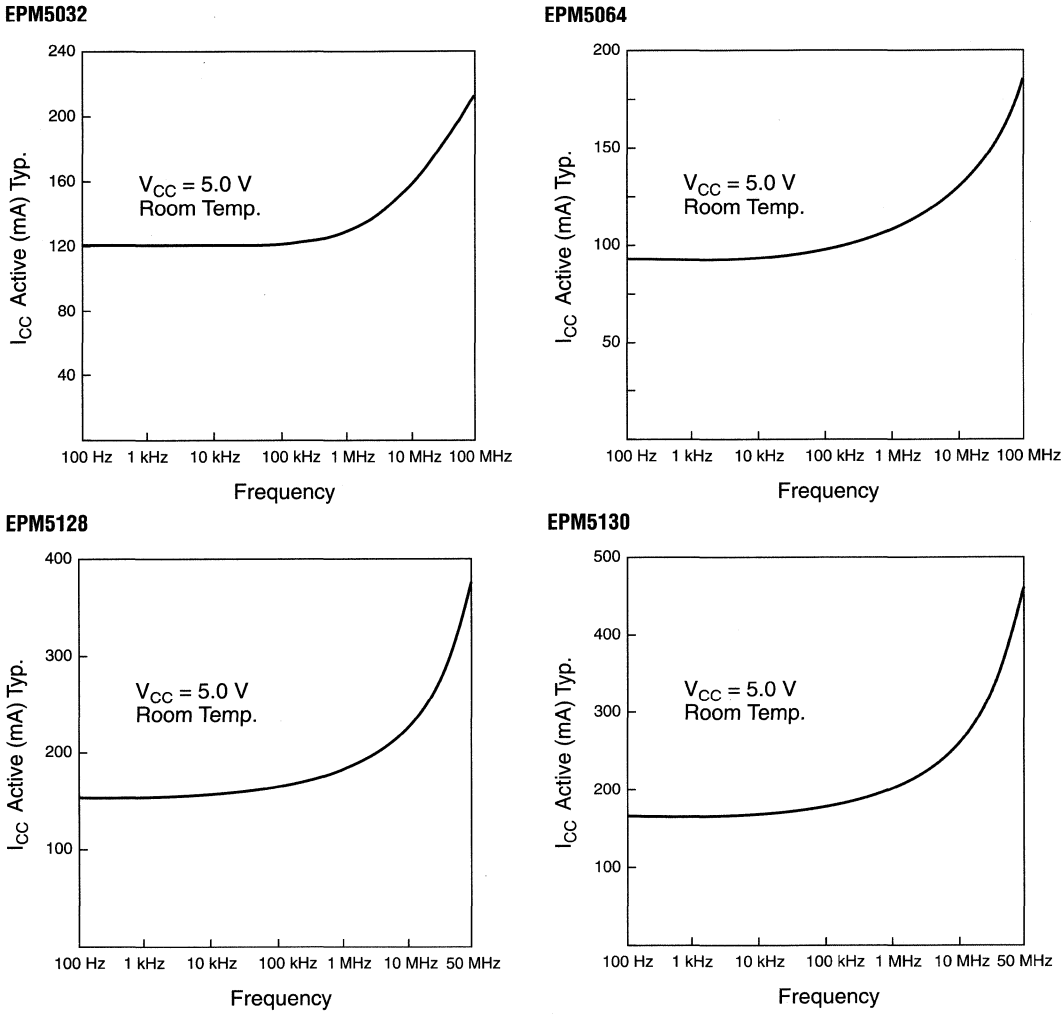
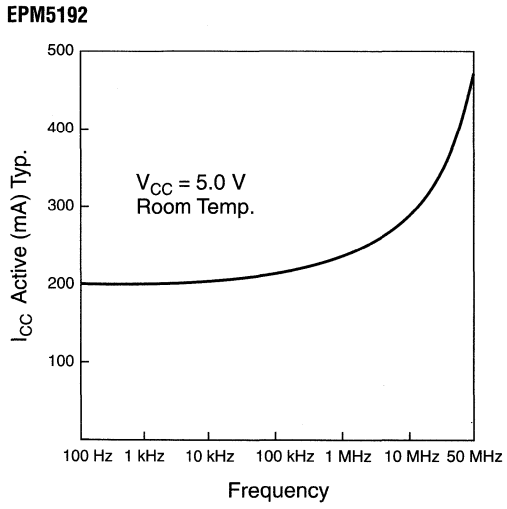


Figure 9. I_{CC} vs. Frequency for MAX 5000 Devices (Part 2 of 2)



Device Pin-Outs

Tables 4 through 13 show the pin names and numbers for the pins in each MAX 5000 device package.

Table 4. EPM5032 Dedicated Pin-Outs

Pin Name	28-Pin J-Lead	28-Pin DIP	28-Pin SOIC
INPUT/CLK	9	2	2
INPUT	6, 7, 8, 20, 21, 22, 23	1, 13, 14, 15, 16, 27, 28	1, 13, 14, 15, 16, 27, 28
GND	15, 28	8, 21	8, 21
VCC	1, 14	7, 22	7, 22

Table 5. EPM5032 I/O Pin-Outs

MC	28-Pin J-Lead	28-Pin DIP	28-Pin SOIC	MC	28-Pin J-Lead	28-Pin DIP	28-Pin SOIC
1	10	3	3	17	24	17	17
2	–	–	–	18	–	–	–
3	11	4	4	19	25	18	18
4	–	–	–	20	–	–	–
5	12	5	5	21	26	19	19
6	–	–	–	22	–	–	–
7	13	6	6	23	27	20	20
8	–	–	–	24	–	–	–
9	16	9	9	25	2	23	23
10	–	–	–	26	–	–	–
11	17	10	10	27	3	24	24
12	–	–	–	28	–	–	–
13	18	11	11	29	4	25	25
14	–	–	–	30	–	–	–
15	19	12	12	31	5	26	26
16	–	–	–	32	–	–	–

Table 6. EPM5064 Dedicated Pin-Outs

Pin Name	44-Pin J-Lead
INPUT/CLK	34
INPUT	9, 11, 12, 13, 31, 33, 35
GND	10, 21, 32, 43
VCC	3, 14, 25, 36

Table 7. EPM5064 I/O Pin-Outs

MC	LAB	44-Pin J-Lead	MC	LAB	44-Pin J-Lead
1	A	2	17	B	15
2	A	4	18	B	16
3	A	5	19	B	17
4	A	6	20	B	18
5	A	7	21	B	19
6	A	8	22	B	20
7	A	–	23	B	22
8	A	–	24	B	23
9	A	–	25	B	–
10	A	–	26	B	–
11	A	–	27	B	–
12	A	–	28	B	–
13	A	–	29	B	–
14	A	–	30	B	–
15	A	–	31	B	–
16	A	–	32	B	–
33	C	24	49	D	37
34	C	26	50	D	38
35	C	27	51	D	39
36	C	28	52	D	40
37	C	29	53	D	41
38	C	30	54	D	42
39	C	–	55	D	44
40	C	–	56	D	1
41	C	–	57	D	–
42	C	–	58	D	–
43	C	–	59	D	–
44	C	–	60	D	–
45	C	–	61	D	–
46	C	–	62	D	–
47	C	–	63	D	–
48	C	–	64	D	–

Table 8. EPM5128 Dedicated Pin-Outs

Pin Name	68-Pin J-Lead	68-Pin PGA
INPUT/CLK	1	B6
INPUT	2, 32, 34, 35, 36, 66, 68	A6, L4, L5, L6, K6, A8, A7
GND	16, 33, 50, 67	B7, E2, G10, K5
VCC	3, 20, 37, 54	B5, E10, G2, K7

Table 9. EPM5128 I/O Pin-Outs (Part 1 of 3)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
1	A	4	A5	17	B	12	C2
2	A	5	B4	18	B	13	C1
3	A	6	A4	19	B	14	D2
4	A	7	B3	20	B	15	D1
5	A	8	A3	21	B	17	E1
6	A	9	A2	22	B	–	–
7	A	10	B2	23	B	–	–
8	A	11	B1	24	B	–	–
9	A	–	–	25	B	–	–
10	A	–	–	26	B	–	–
11	A	–	–	27	B	–	–
12	A	–	–	28	B	–	–
13	A	–	–	29	B	–	–
14	A	–	–	30	B	–	–
15	A	–	–	31	B	–	–
16	A	–	–	32	B	–	–

Table 9. EPM5128 I/O Pin-Outs (Part 2 of 3)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
33	C	18	F2	49	D	24	J2
34	C	19	F1	50	D	25	J1
35	C	21	G1	51	D	26	K1
36	C	22	H2	52	D	27	K2
37	C	23	H1	53	D	28	L2
38	C	–	–	54	D	29	K3
39	C	–	–	55	D	30	L3
40	C	–	–	56	D	31	K4
41	C	–	–	57	D	–	–
42	C	–	–	58	D	–	–
43	C	–	–	59	D	–	–
44	C	–	–	60	D	–	–
45	C	–	–	61	D	–	–
46	C	–	–	62	D	–	–
47	C	–	–	63	D	–	–
48	C	–	–	64	D	–	–
65	E	38	L7	81	F	46	J10
66	E	39	K8	82	F	47	J11
67	E	40	L8	83	F	48	H10
68	E	41	K9	84	F	49	H11
69	E	42	L9	85	F	51	G11
70	E	43	L10	86	F	–	–
71	E	44	K10	87	F	–	–
72	E	45	K11	88	F	–	–
73	E	–	–	89	F	–	–
74	E	–	–	90	F	–	–
75	E	–	–	91	F	–	–
76	E	–	–	92	F	–	–
77	E	–	–	93	F	–	–
78	E	–	–	94	F	–	–
79	E	–	–	95	F	–	–
80	E	–	–	96	F	–	–

Table 9. EPM5128 I/O Pin-Outs (Part 3 of 3)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
97	G	52	F10	113	H	58	C10
98	G	53	F11	114	H	59	C11
99	G	55	E11	115	H	60	B11
100	G	56	D10	116	H	61	B10
101	G	57	D11	117	H	62	A10
102	G	–	–	118	H	63	B9
103	G	–	–	119	H	64	A9
104	G	–	–	120	H	65	B8
105	G	–	–	121	H	–	–
106	G	–	–	122	H	–	–
107	G	–	–	123	H	–	–
108	G	–	–	124	H	–	–
109	G	–	–	125	H	–	–
110	G	–	–	126	H	–	–
111	G	–	–	127	H	–	–
112	G	–	–	128	H	–	–

Table 10. EPM5130 Dedicated Pin-Outs

Pin Name	84-Pin J-Lead	100-Pin PGA	100-Pin PQFP
INPUT/CLK	1	C7	16
INPUT	2, 5, 6, 7, 36, 37, 38, 41, 42, 43, 44, 47, 48, 49, 78, 79, 80, 83, 84	A5, A7, A8, A9, A10, B5, B7, B9, C6, L7, L8, M5, M7, M9, N4, N5, N6, N7, N9	9, 10, 11, 14, 15, 16, 17, 20, 21, 22, 59, 60, 61, 64, 65, 66, 67, 70, 71, 72
GND	19, 20, 39, 40, 61, 62, 81, 82	B8, C8, F2, F3, H11, H12, L6, M6	12, 13, 37, 38, 62, 63, 87, 88
VCC	3, 4, 23, 24, 45, 46, 65, 66	A6, B6, F12, F13, H1, H2, M8, N8	18, 19, 43, 44, 68, 69, 93, 94

Table 11. EPM5130 I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin PQFP	MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin PQFP
1	A	8	B13	1	17	B	14	A4	23
2	A	9	C12	2	18	B	15	B4	24
3	A	10	A13	3	19	B	16	A3	25
4	A	11	B12	4	20	B	17	A2	26
5	A	12	A12	5	21	B	18	B3	27
6	A	13	B11	6	22	B	21	A1	28
7	A	–	A11	7	23	B	–	B2	29
8	A	–	B10	8	24	B	–	B1	30
9	A	–	–	–	25	B	–	–	–
10	A	–	–	–	26	B	–	–	–
11	A	–	–	–	27	B	–	–	–
12	A	–	–	–	28	B	–	–	–
13	A	–	–	–	29	B	–	–	–
14	A	–	–	–	30	B	–	–	–
15	A	–	–	–	31	B	–	–	–
16	A	–	–	–	32	B	–	–	–
33	C	22	C2	31	49	D	30	G3	41
34	C	25	C1	32	50	D	31	G1	42
35	C	26	D2	33	51	D	32	H3	45
36	C	27	D1	34	52	D	33	J1	46
37	C	28	E2	35	53	D	34	J2	47
38	C	29	E1	36	54	D	35	K1	48
39	C	–	F1	39	55	D	–	K2	49
40	C	–	G2	40	56	D	–	L1	50
41	C	–	–	–	57	D	–	–	–
42	C	–	–	–	58	D	–	–	–
43	C	–	–	–	59	D	–	–	–
44	C	–	–	–	60	D	–	–	–
45	C	–	–	–	61	D	–	–	–
46	C	–	–	–	62	D	–	–	–
47	C	–	–	–	63	D	–	–	–
48	C	–	–	–	64	D	–	–	–

Table 11. EPM5130 I/O Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin PQFP	MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin PQFP
65	E	50	M1	51	81	F	56	N10	73
66	E	51	L2	52	82	F	57	M10	74
67	E	52	N1	53	83	F	58	N11	75
68	E	53	M2	54	84	F	59	N12	76
69	E	54	N2	55	85	F	60	M11	77
70	E	55	M3	56	86	F	63	N13	78
71	E	–	N3	57	87	F	–	M12	79
72	E	–	M4	58	88	F	–	M13	80
73	E	–	–	–	89	F	–	–	–
74	E	–	–	–	90	F	–	–	–
75	E	–	–	–	91	F	–	–	–
76	E	–	–	–	92	F	–	–	–
77	E	–	–	–	93	F	–	–	–
78	E	–	–	–	94	F	–	–	–
79	E	–	–	–	95	F	–	–	–
80	E	–	–	–	96	F	–	–	–
97	G	64	L12	81	113	H	72	G11	91
98	G	67	L13	82	114	H	73	G13	92
99	G	68	K12	83	115	H	74	F11	95
100	G	69	K13	84	116	H	75	E13	96
101	G	70	J12	85	117	H	76	E12	97
102	G	71	J13	86	118	H	77	D13	98
103	G	–	H13	89	119	H	–	D12	99
104	G	–	G12	90	120	H	–	C13	100
105	G	–	–	–	121	H	–	–	–
106	G	–	–	–	122	H	–	–	–
107	G	–	–	–	123	H	–	–	–
108	G	–	–	–	124	H	–	–	–
109	G	–	–	–	125	H	–	–	–
110	G	–	–	–	126	H	–	–	–
111	G	–	–	–	127	H	–	–	–
112	G	–	–	–	128	H	–	–	–

Table 12. EPM5192 Dedicated Pin-Outs

Pin Name	84-Pin J-Lead	84-Pin PGA
INPUT/CLK	1	A6
INPUT	2, 41, 42, 43, 44, 83, 84	A5, K6, J6, J7, L7, C7, C6
GND	18, 19, 39, 40, 60, 61, 81, 82	A7, B7, E1, E2, G10, G11, K5, L5
VCC	3, 24, 45, 66	B5, E10, G2, K7

Table 13. EPM5192 I/O Pin-Outs (Part 1 of 4)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
1	A	4	C5	17	B	12	C2
2	A	5	A4	18	B	13	B1
3	A	6	B4	19	B	14	C1
4	A	7	A3	20	B	15	D2
5	A	8	A2	21	B	–	–
6	A	9	B3	22	B	–	–
7	A	10	A1	23	B	–	–
8	A	11	B2	24	B	–	–
9	A	–	–	25	B	–	–
10	A	–	–	26	B	–	–
11	A	–	–	27	B	–	–
12	A	–	–	28	B	–	–
13	A	–	–	29	B	–	–
14	A	–	–	30	B	–	–
15	A	–	–	31	B	–	–
16	A	–	–	32	B	–	–

Table 13. EPM5192 I/O Pin-Outs (Part 2 of 4)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
33	C	16	D1	49	D	22	G3
34	C	17	E3	50	D	23	G1
35	C	20	F2	51	D	25	F1
36	C	21	F3	52	D	26	H1
37	C	–	–	53	D	–	–
38	C	–	–	54	D	–	–
39	C	–	–	55	D	–	–
40	C	–	–	56	D	–	–
41	C	–	–	57	D	–	–
42	C	–	–	58	D	–	–
43	C	–	–	59	D	–	–
44	C	–	–	60	D	–	–
45	C	–	–	61	D	–	–
46	C	–	–	62	D	–	–
47	C	–	–	63	D	–	–
48	C	–	–	64	D	–	–
65	E	27	H2	81	F	31	L1
66	E	28	J1	82	F	32	K2
67	E	29	K1	83	F	33	K3
68	E	30	J2	84	F	34	L2
69	E	–	–	85	F	35	L3
70	E	–	–	86	F	36	K4
71	E	–	–	87	F	37	L4
72	E	–	–	88	F	38	J5
73	E	–	–	89	F	–	–
74	E	–	–	90	F	–	–
75	E	–	–	91	F	–	–
76	E	–	–	92	F	–	–
77	E	–	–	93	F	–	–
78	E	–	–	94	F	–	–
79	E	–	–	95	F	–	–
80	E	–	–	96	F	–	–

Table 13. EPM5192 I/O Pin-Outs (Part 3 of 4)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
97	G	46	L6	113	H	54	J10
98	G	47	L8	114	H	55	K11
99	G	48	K8	115	H	56	J11
100	G	49	L9	116	H	57	H10
101	G	50	L10	117	H	–	–
102	G	51	K9	118	H	–	–
103	G	52	L11	119	H	–	–
104	G	53	K10	120	H	–	–
105	G	–	–	121	H	–	–
106	G	–	–	122	H	–	–
107	G	–	–	123	H	–	–
108	G	–	–	124	H	–	–
109	G	–	–	125	H	–	–
110	G	–	–	126	H	–	–
111	G	–	–	127	H	–	–
112	G	–	–	128	H	–	–
129	I	58	H11	145	J	64	F11
130	I	59	F10	146	J	65	E11
131	I	62	G9	147	J	67	E9
132	I	63	F9	148	J	68	D11
133	I	–	–	149	J	–	–
134	I	–	–	150	J	–	–
135	I	–	–	151	J	–	–
136	I	–	–	152	J	–	–
137	I	–	–	153	J	–	–
138	I	–	–	154	J	–	–
139	I	–	–	155	J	–	–
140	I	–	–	156	J	–	–
141	I	–	–	157	J	–	–
142	I	–	–	158	J	–	–
143	I	–	–	159	J	–	–
144	I	–	–	160	J	–	–

Table 13. EPM5192 I/O Pin-Outs (Part 4 of 4)

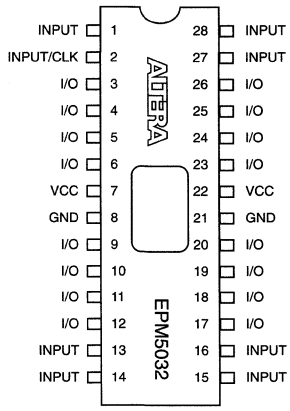
MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
161	K	69	D10	177	L	73	A11
162	K	70	C11	178	L	74	B10
163	K	71	B11	179	L	75	B9
164	K	72	C10	180	L	76	A10
165	K	–	–	181	L	77	A9
166	K	–	–	182	L	78	B8
167	K	–	–	183	L	79	A8
168	K	–	–	184	L	80	B6
169	K	–	–	185	L	–	–
170	K	–	–	186	L	–	–
171	K	–	–	187	L	–	–
172	K	–	–	188	L	–	–
173	K	–	–	189	L	–	–
174	K	–	–	190	L	–	–
175	K	–	–	191	L	–	–
176	K	–	–	192	L	–	–

Pin-Out Diagrams

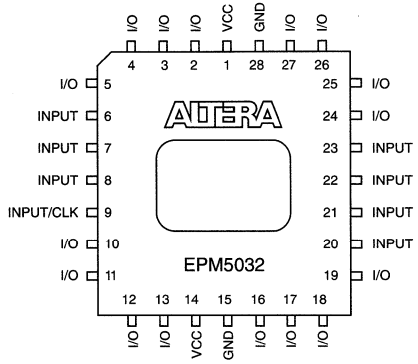
Figures 10 through 14 show the package pin-out diagrams of MAX 5000 devices.

Figure 10. EPM5032 Package Pin-Out Diagrams

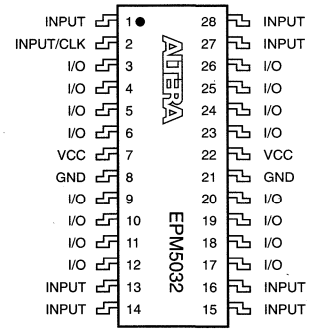
Package outlines not drawn to scale. Windows in ceramic packages only.



28-Pin DIP



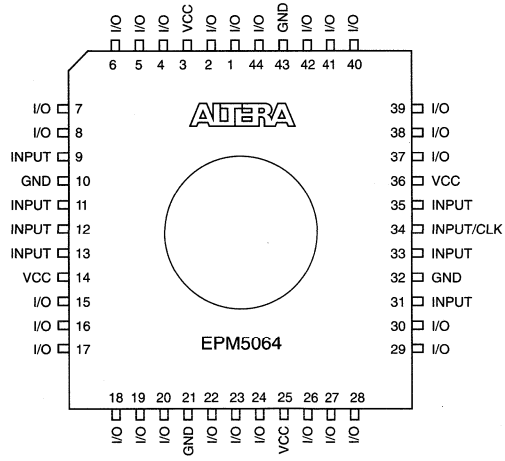
28-Pin J-Lead



28-Pin SOIC

Figure 11. EPM5064 Package Pin-Out Diagrams

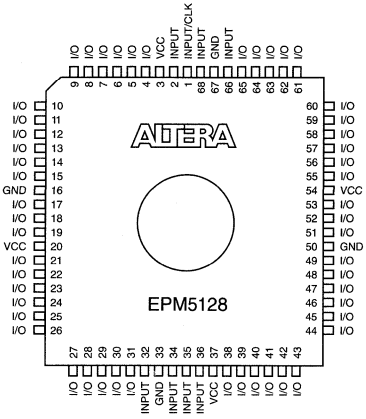
Package outline not drawn to scale. Windows in ceramic packages only.



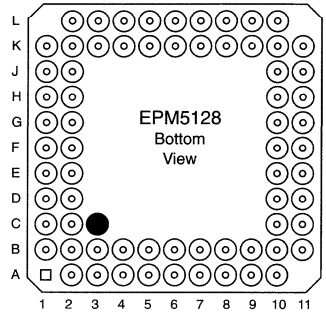
44-Pin J-Lead

Figure 12. EPM5128 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



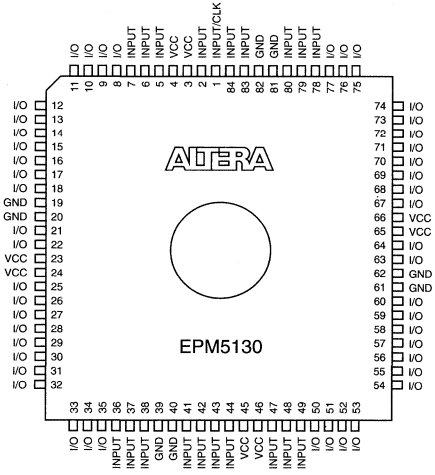
68-Pin J-Lead



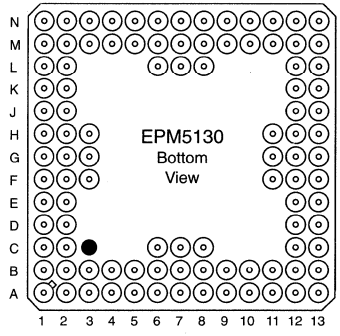
68-Pin PGA

Figure 13. EPM5130 Package Pin-Out Diagrams

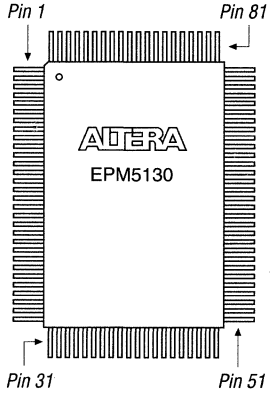
Package outlines not drawn to scale. Windows in ceramic packages only.



84-Pin J-Lead



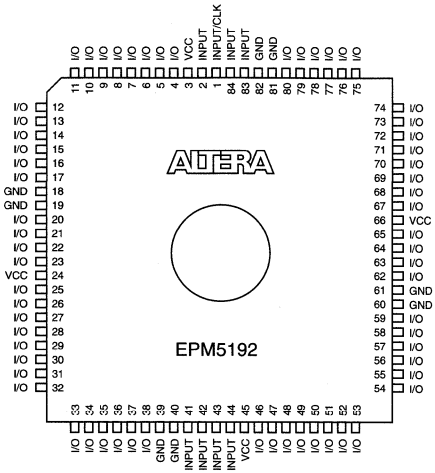
100-Pin PGA



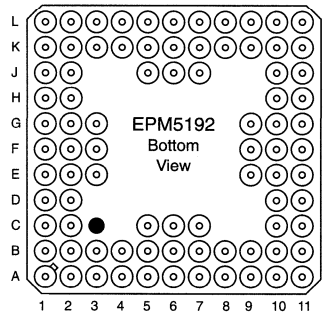
100-Pin PQFP

Figure 14. EPM5192 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



84-Pin J-Lead



84-Pin PGA

Notes:

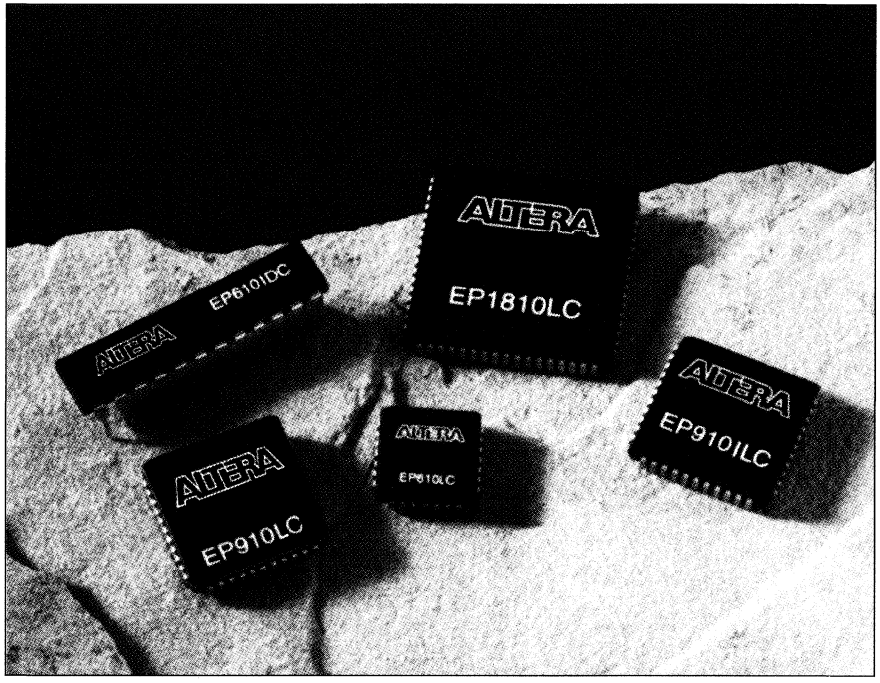
June 1996

Classic EPLD Family Data Sheet

EP610 EPLD

EP910 EPLD

EP1810 EPLD


ALTERA
EP1810LC
ALTERA
EP9101LC
ALTERA
EP9101DC
ALTERA
EP910LC
ALTERA
EP810LC

Classic
EPLD Family

June 1996, ver. 3 — Data Sheet

Features

- Complete device family with logic densities of up to 900 usable gates (see Table 1)
- Device erasure and reprogramming with advanced, non-volatile EPROM configuration elements
- Fast pin-to-pin logic delays as low as 10 ns and counter frequencies as high as 100 MHz
- 24 to 68 pins available in dual in-line package (DIP), ceramic and plastic J-lead chip carrier (JLCC and PLCC), pin-grid array (PGA), small-outline integrated circuit (SOIC), and one-time-programmable (OTP) packages
- Programmable security bit for protection of proprietary designs
- 100% generically testable to provide 100% programming yield
- Programmable registers providing D, T, JK, and SR flipflops with individual clear and clock controls
- Software design support featuring Altera's MAX+PLUS II development system on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations; Altera's PLDshell Plus software; and third-party development systems
- Programming support with Altera's Master Programming Unit (MPU); programming hardware from Data I/O and others
- Additional design entry and simulation support provided by EDIF, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar, Mentor Graphics, MINC, OrCAD, Synopsys, VeriBest, and Viewlogic

Table 1. Classic Device Features

Feature	EP610 & EP610I	EP910 & EP910I	EP1810
Usable gates	300	450	900
Macrocells	16	24	48
Maximum user I/O pins	22	38	64
t_{PD} (ns)	10	12	20
f_{CNT} (MHz)	100	76.9	50

General Description

The Altera Classic device family offers the industry's most comprehensive solution to high-speed, low-power logic integration. Fabricated on advanced CMOS technology, Classic devices also have a Turbo-only version, which is described in this data sheet.

Classic devices support 100% TTL emulation and can easily integrate multiple PAL- and GAL-type devices with densities ranging from 300 to 900 usable gates. The Classic family provides pin-to-pin logic delays as low as 10 ns and counter frequencies as high as 100 MHz. Classic devices are available in a wide range of packages, including ceramic and plastic dual in-line (CerDIP and PDIP), plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), and plastic small-outline integrated circuit (SOIC) packages.

Unlike equivalent bipolar devices, EPROM-based Classic devices can reduce active power consumption without sacrificing performance. This reduced power consumption makes the Classic family well suited for a wide range of low-power applications. Classic devices are 100% generically tested and can be erased with UV light. Designs and design changes can be implemented quickly, eliminating the need for post-programming testing.

Classic devices use sum-of-products logic and a programmable register. The sum-of-products logic provides a programmable-AND/fixed-OR structure that can implement logic with up to eight product terms. The programmable register can be individually programmed for D, T, SR, or JK flipflop operation or can be bypassed for combinatorial operation. In addition, macrocell registers can be individually clocked either by a global clock or by any input or feedback path to the AND array. Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to implement a variety of logic functions simultaneously.

Classic devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

For more information, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Functional Description

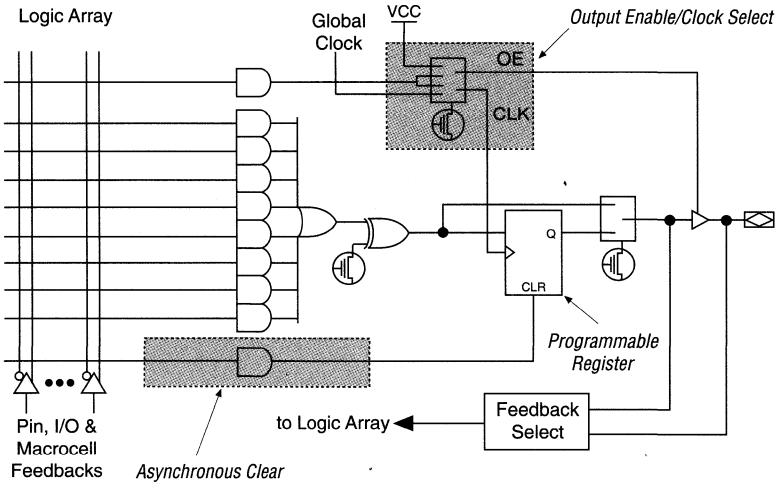
The Classic architecture includes the following elements:

- Macrocells
- Programmable registers
- Output enable/clock select
- Feedback selection

Macrocells

Classic macrocells, shown in Figure 1, can be individually configured for both sequential and combinatorial logic operation. Eight product terms form a programmable-AND array that feeds an OR gate for combinatorial logic implementation. An additional product term is used for asynchronous clear control of the internal register; another product term implements either an output enable or a logic-array-generated clock. Inputs to the programmable-AND array come from both the true and complement signals of the dedicated inputs; feedbacks from I/O pins that are configured as inputs; and feedbacks from macrocell outputs. Signals from dedicated inputs are globally routed and can feed the inputs of all device macrocells. The feedback multiplexer controls the routing of feedback signals from macrocells and from I/O pins configured as inputs. For additional information on feedback select configurations, see Figure 3.

Figure 1. Classic Device Macrocell



The eight product terms of the programmable-AND array feed the 8-input OR gate, which then feeds one input to an XOR gate. The other input to the XOR gate is connected to a programmable bit that allows the array output to be inverted. Altera's MAX+PLUS II software uses either the XOR gate to implement active-high or active-low logic, or De Morgan's inversion to reduce the number of product terms to implement a function.

Programmable Registers

To implement registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation. If necessary, the register can be bypassed for combinatorial operation. During design compilation, MAX+PLUS II selects the most efficient register operation for each registered function to minimize the logic resources needed by the design. Registers have an individual asynchronous clear function controlled by a dedicated product term, and are cleared automatically during power-up.

In addition, macrocell registers can be individually clocked by either a global clock or any input or feedback path to the AND array. Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to simultaneously implement a variety of logic functions.

Output Enable/Clock Select

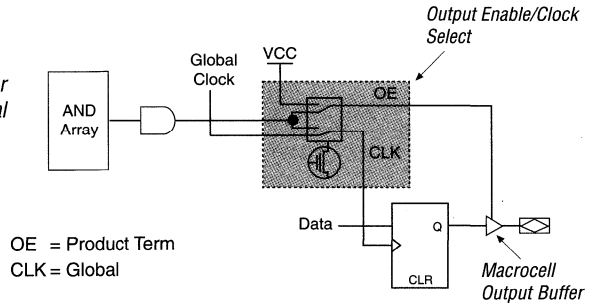
Figure 2 shows the two operating modes (Modes 0 and 1) provided by the output enable/clock (OE/CLK) select. The OE/CLK select, which is controlled by a single programmable bit, can be individually configured for each macrocell. In Mode 0, the tri-state output buffer is controlled by a single product term. If the output enable is high, the output buffer is enabled. If the output enable is low, the output has a high-impedance value. In Mode 0, the macrocell flipflop is clocked by its global clock input signal.

In Mode 1, the output enable buffer is always enabled, and the macrocell register can be triggered by an array clock signal generated by a product term. This mode allows registers to be individually clocked by any signal on the AND array. With both true and complement signals in the AND array, the register can be configured to trigger on a rising or falling edge. This product-term-controlled clock configuration also supports gated clock structures.

Figure 2. Output Enable/Clock Select

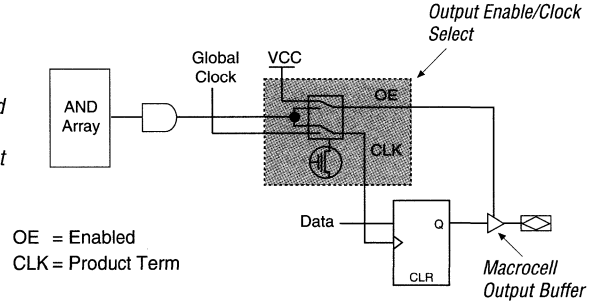
Mode 0

In Mode 0, the register is clocked by the global clock signal. The output is enabled by the logic from the product term.



Mode 1

In Mode 1, the output is permanently enabled and the register is clocked by the product term, which allows gated clocks to be generated.

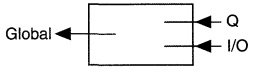


Feedback Selection

Each macrocell in a Classic device provides feedback selection that is controlled by the feedback multiplexer. This feedback selection allows the user to feed either the macrocell output or the I/O pin input associated with the macrocell back into the AND array. The macrocell output can be either the Q output of the programmable register or the combinatorial output of the macrocell. Different devices have different feedback multiplexer configurations. See Figure 3.

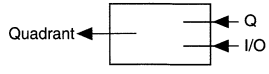
Figure 3. Feedback Multiplexer Configurations

Global Feedback Multiplexer



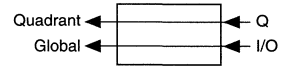
EP610
EP610I
EP910
EP910I

Quadrant Feedback Multiplexer



EP1810
EP1810T

Dual Feedback Multiplexer



EP1810
EP1810T

EP610, EP610I, EP910, and EP910I devices have a global feedback configuration; either the macrocell output (Q) or the I/O pin input (I/O) can feed back to the AND array so that it is accessible to all other macrocells.

EP1810 macrocells can have either of two feedback configurations: quadrant or dual. Most macrocells in EP1810 devices have a quadrant feedback configuration; either the macrocell output or I/O pin input can feed back to other macrocells in the same quadrant. Selected macrocells in EP1810 devices have a dual feedback configuration: the output of the macrocell feeds back to other macrocells in the same quadrant, and the I/O pin input feeds back to all macrocells in the device. If the associated I/O pin is not used, the macrocell output can optionally feed all macrocells in the device. In this case, the output of the macrocell passes through the tri-state buffer and uses the feedback path between the buffer and the I/O pin.

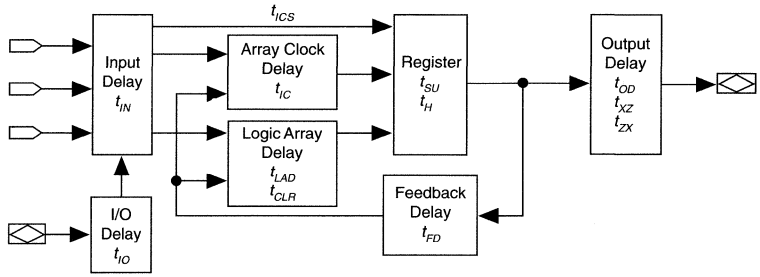
Design Security

Classic devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since data within EPROM configuration elements is invisible. The security bit that controls this function and other program data is reset when a device is erased.

Timing Model

Device timing can be analyzed with the MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 4. Devices have fixed internal delays that allow the user to determine the worst-case timing for any design. The MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 4. Timing Model

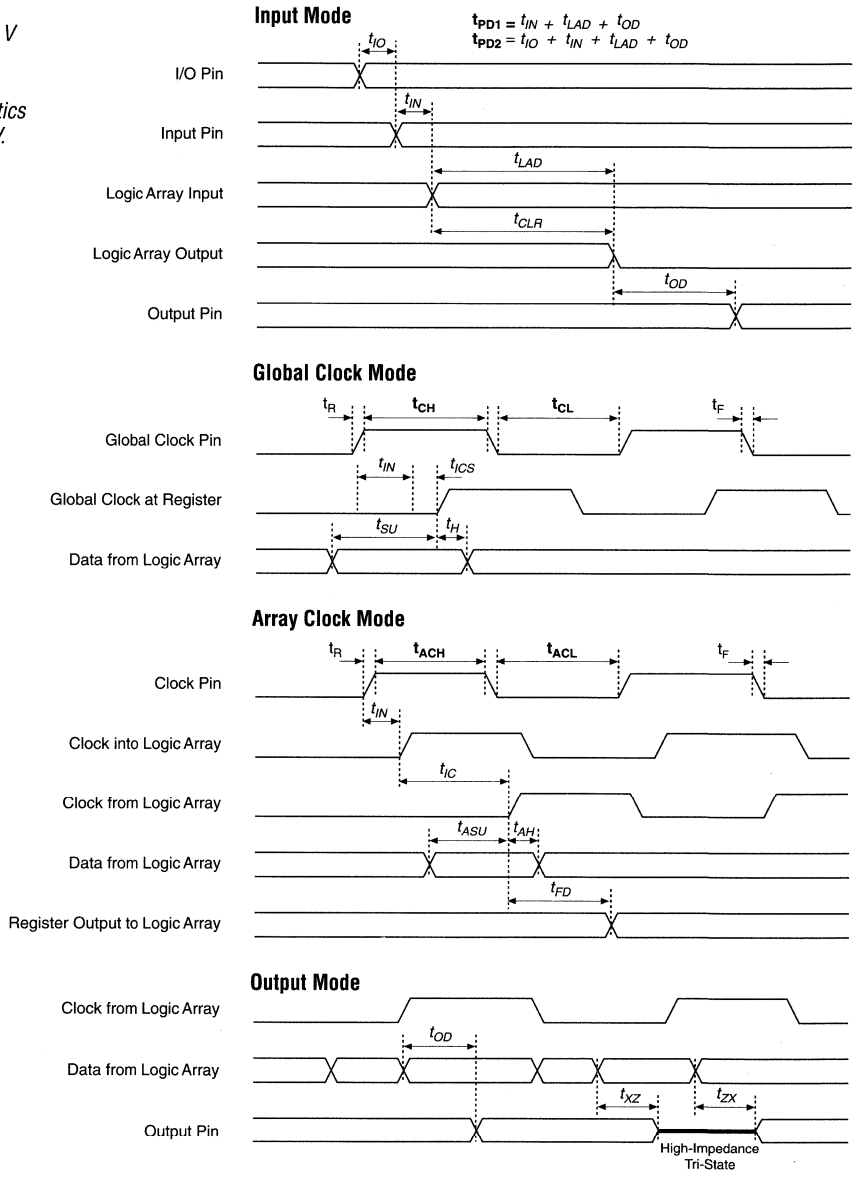


Timing information can be derived from the timing model and parameters for a particular device. External timing parameters represent pin-to-pin timing delays, and can be calculated from the sum of internal parameters. Figure 5 shows the internal timing relationship for internal and external delay parameters.

For more information on device timing, refer to *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book.

Figure 5. Switching Waveforms

t_R & t_F < 3 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low.
All timing characteristics are measured at 1.5 V.



Turbo Bit

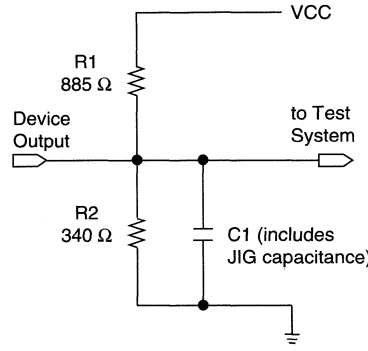
Many Classic devices contain a programmable Turbo Bit to control the automatic power-down feature that enables the low-standby-power mode (I_{CC1}). When the Turbo Bit is turned on, the low-standby-power mode is disabled. All AC values are tested with the Turbo Bit turned on. When the device is operating with the Turbo Bit turned off (non-Turbo mode), a non-Turbo adder must be added to the appropriate AC parameter to determine worst-case timing. The non-Turbo adder is specified in the "AC Operating Conditions" tables for each Classic device that supports the Turbo mode.

Generic Testing

Classic devices are fully functionally tested. Complete testing of each programmable EPROM configuration element and all internal logic elements ensures 100% programming yield. See Figure 6 for AC test measurement conditions.

Figure 6. AC Test Conditions

Power-supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



EPROM-based devices in OTP plastic packages also contain on-board logic test circuitry to allow verification of function and AC specifications during standard production flow.

Device Programming

Classic devices can be programmed on 486- and Pentium-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

Data I/O and other programming hardware manufacturers also offer programming support for Altera devices. See *Programming Hardware Manufacturers* in this data book for more information.

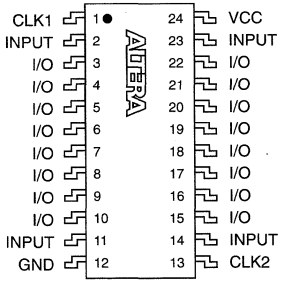
Notes:

Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 10 ns
  - Counter frequencies of up to 100 MHz
  - Pipelined data rates of up to 125 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs and 2 clock pins
- EP610, EP610I, and EP600I devices that are pin-, function-, and programming file-compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 7):
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 24-pin ceramic and plastic dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

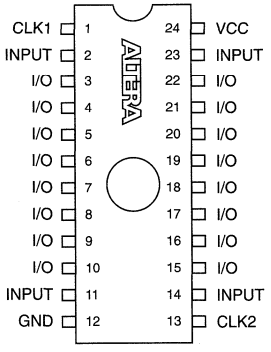
Figure 7. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



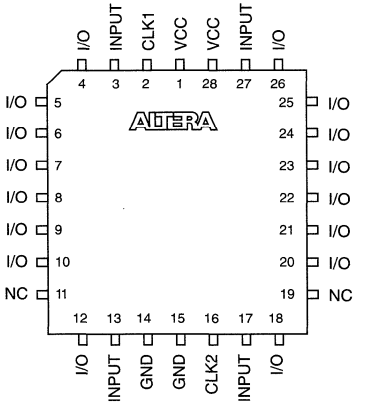
24-Pin SOIC

EP610



24-Pin DIP

EP610
EP610I



28-Pin PLCC

EP610
EP610I

General Description

EP610 devices have 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global clock pins (see Figure 8). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. The CLK1 signal is a dedicated clock input for the registers in macrocells 9 through 16. The CLK2 signal is a dedicated clock input for registers in macrocells 1 through 8.

Figure 8. EP610 Block Diagram

Numbers without parentheses are for both DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

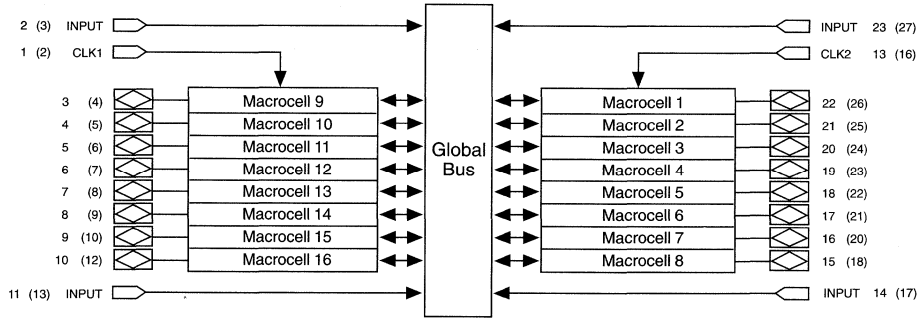


Figure 9 shows the typical supply current (I_{CC}) versus frequency for EP610 devices.

Figure 9. I_{CC} vs. Frequency of EP610 Devices

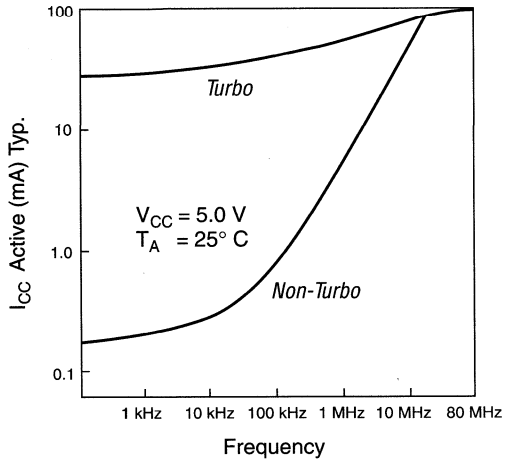
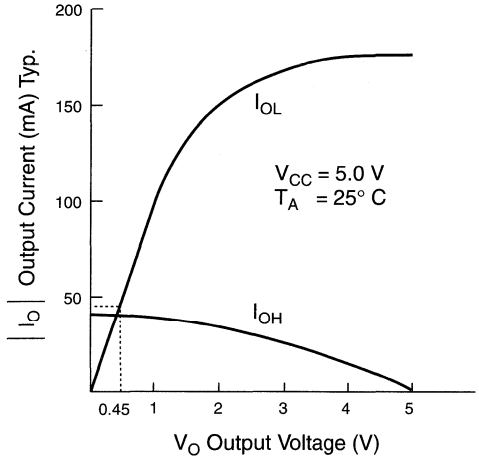


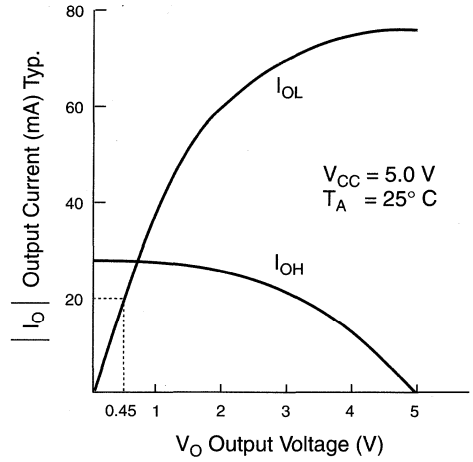
Figure 10 shows the maximum output drive characteristics of EP610 devices.

Figure 10. Output Drive Characteristics of EP610 Devices

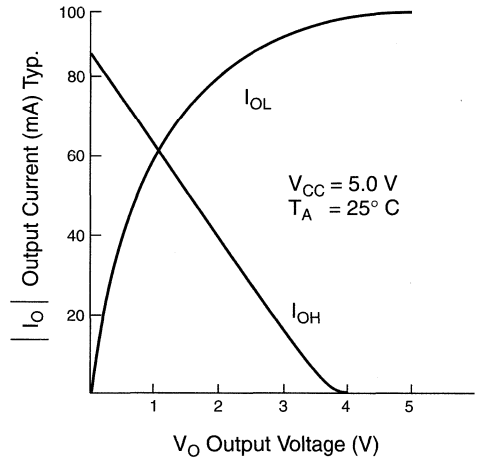
EP610-15 & EP610-20 EPLDs



EP610-25, EP610-30 & EP610-35 EPLDs



EP610I EPLDs



EP610 & EP610I Device Absolute Maximum Ratings *Notes (1), (2)*

			EP610		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	With respect to GND, *Note (3)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	–0.5	V_{CC} + 0.5	V
I_{MAX}	DC V_{CC} or GND current		–175	175			mA
I_{OUT}	DC output current, per pin		–25	25			mA
P_D	Power dissipation			1,000			mW
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135 (125)	–10	85	° C
T_J	Junction temperature	Ceramic packages, under bias		150		150	° C
		Plastic packages, under bias		135		135	° C

EP610 & EP610I Device Recommended Operating Conditions *Notes (2), (4)*

			EP610		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	*Note (5)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	–40	85	° C
t_R	Input rise time	*Note (6)*		100 (50)		500	ns
t_F	Input fall time	*Note (6)*		100 (50)		500	ns

EP610 & EP610I Device DC Operating Conditions *Notes (2), (4)*

Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (8)*	2.4		V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC *Notes (8), (9)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (8)*		0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or GND	–10	10	µA

EP610 & EP610I Device Capacitance *Note (10)*

			EP610I		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		12	pF

EP610 Device I_{CC} Supply Current *Notes (2), (7)*

				EP610			
Symbol	**Parameter**	**Conditions**	**Speed Grade**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or GND, no load *Notes (11), (12), (13)*			20	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or GND, no load f = 1.0 MHz, *Note (13)*			5	10 (15)	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	*Notes (12), (13)*	-15, -20		60	90 (115)	mA
			-25, -30, -35		45	60 (75)	mA

EP610I Device I_{CC} Supply Current *Note (7)*

			EP610I			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or GND, no load, *Notes (11), (12), (13)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (11), (13)*		3	8	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (11), (13)*		65	105	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Numbers in parentheses are for industrial-temperature-range versions.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) For EP610 devices, maximum V_{CC} rise time is 50 ms. For EP610I devices, V_{CC} rise time is unlimited with monotonic rise.
(6) For EP610-15 and EP610-20 EPLDs: t_R and t_F = 40 ns.
For EP610-15 and EP610-20 clocks: t_R and t_F = 20 ns.
(7) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(8) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(9) This parameter does not apply to EP610I devices.
(10) The device capacitance was measured at 25° C and was sample-tested only. The clock-pin capacitance is for dedicated clock inputs only. For EP610-25, EP610-30, and EP610-35: Pin 13 has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and C_{CLK} = 20 pF.
(11) When the Turbo Bit is not set (non-Turbo mode), an EP610 EPLD enters standby mode if no logic transitions occur for 100 ns after the last transition. When the Turbo Bit is not set, an EP610I device enters standby mode if no logic transitions occur for 75 ns after the last transition.
(12) Measured with a device programmed as a 16-bit counter. The I_{CC} was measured at 0° C.
(13) Data path is programmed as a 16-bit counter.

EP610-15 & EP610-20 Device AC Operating Conditions *Notes (1), (2)*

External Timing Parameters			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		17		22	20	ns
t_{PZX}	Input to output enable	C1 = 35 pF		15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (4)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
f_{MAX}	Maximum clock frequency	*Note (5)*	83.3		62.5		0	MHz
t_{SU}	Global clock input setup time		9		11		20	ns
t_{H}	Global clock input hold time		0		0		0	ns
t_{CH}	Global clock high time		6		8		0	ns
t_{CL}	Global clock low time		6		8		0	ns
t_{CO1}	Global clock to output delay			11		13	0	ns
t_{CNT}	Global clock minimum period			12		16	0	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	83.3		62.5		0	MHz
t_{ASU}	Array clock input setup time		6		8		20	ns
t_{AH}	Array clock input hold time		6		8		0	ns
t_{ACH}	Array clock high time		7		9		0	ns
t_{ACL}	Array clock low time		7		9		0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (7)*	1		1		1	ns
t_{ACO1}	Array clock to output delay			15		20	20	ns
t_{ACNT}	Array clock minimum period			14		18	0	ns
f_{ACNT}	Array clock internal maximum frequency	*Note (6)*	71.4		55.6		0	MHz

Internal Timing Parameters			EP610-15		EP610-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			4		4	ns
t_{IO}	I/O input pad and buffer delay			2		2	ns
t_{LAD}	Logic array delay			6		11	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		5		4		ns
t_{H}	Register hold time		4		7		ns
t_{IC}	Array clock delay			6		11	ns
t_{ICS}	Global clock delay			2		4	ns
t_{FD}	Feedback delay			1		1	ns
t_{CLR}	Register clear time			6		11	ns

EP610-25, EP610-30 & EP610-35 AC Operating Conditions *Notes (1), (2)*

External Timing Parameters			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (11)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	30	ns
t_{PD2}	I/O input to non-registered output			27		32		37	30	ns
t_{PZX}	Input to output enable			25		30		35	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (4)*		25		30		35	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27		32		37	30	ns
f_{MAX}	Maximum frequency	*Note (5)*	47.6		41.7		37		0	MHz
t_{SU}	Global clock input setup time		21		24		27		30	ns
t_{H}	Global clock input hold time		0		0		0		0	ns
t_{CH}	Global clock high time		10		11		12		0	ns
t_{CL}	Global clock low time		10		11		12		0	ns
t_{CO1}	Global clock to output delay			15		17		20	0	ns
t_{CNT}	Global clock minimum period			25		30		35	0	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	40		33.3		28.6		0	MHz
t_{ASU}	Array clock input setup time		8		8		8		30	ns
t_{AH}	Array clock input hold time		12		12		12		0	ns
t_{ACH}	Array clock high time		10		11		12		0	ns
t_{ACL}	Array clock low time		10		11		12		0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (7)*	1		1		1			ns
t_{ACO1}	Array clock to output delay			27		32		37	30	ns
t_{ACNT}	Array clock minimum period			25		30		35	0	ns
f_{ACNT}	Max. internal global clock frequency	*Note (6)*	40		33.3		28.6		0	MHz

Internal Timing Parameters			EP610-25		EP610-30		EP610-35		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			8		9		11	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	ns
t_{LAD}	Logic array delay			11		14		15	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		7		9	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		6		7		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		7		9	ns
t_{SU}	Register setup time		11		11		12		ns
t_{H}	Register hold time		10		10		10		ns
t_{IC}	Array clock delay			13		16		17	ns
t_{ICS}	Global clock delay			1		1		0	ns
t_{FD}	Feedback delay			3		5		8	ns
t_{CLR}	Register clear time			13		16		17	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) See *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book for additional internal timing parameters.

(3) The non-Turbo adder must be added to this parameter when the Turbo Bit is off.

(4) Sample-tested only for an output change of 500 mV.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

(6) Measured with a device programmed as a 16-bit counter. I_{CC} is measured at 0° C.

(7) Sample tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.

EP610 Device AC Operating Conditionsl *Notes (1), (2)*

External Timing Parameters			EP610I-10		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output, *Note (4)*	C1 = 35 pF		10	25	ns
t_{PD2}	I/O input to non-registered output, *Note (4)*			10	25	ns
t_{PZX}	Input to output enable			15	25	ns
t_{PXZ}	Input to output disable, *Note (5)*	C1 = 5 pF *Note (4)*		13	25	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		13	25	ns
f_{MAX}	Maximum frequency	*Note (5)*	125		0	MHz
t_{SU}	Global clock input setup time		7		25	ns
t_{H}	Global clock input hold time		0		0	ns
t_{CH}	Global clock high time		5		0	ns
t_{CL}	Global clock low time		5		0	ns
t_{CO1}	Global clock to output delay			6.5	0	ns
t_{CNT}	Global clock minimum period			10	25	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	100		0	MHz
t_{ASU}	Array clock input setup time		1.5		25	ns
t_{AH}	Array clock input hold time		5.5		0	ns
t_{ACH}	Array clock high time		5		0	ns
t_{ACL}	Array clock low time		5		0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (7)*	1		0	ns
t_{ACO1}	Array clock to output delay			12	25	ns
t_{ACNT}	Array clock minimum period	*Note (6)*		10	25	ns
f_{ACNT}	Max. internal array clock frequency	*Note (6)*	100		0	MHz

Internal Timing Parameters			EP610I-10		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			1.5	ns
t_{IO}	I/O input pad and buffer delay			0.0	ns
t_{LAD}	Logic array delay			5.5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		8.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0	ns
t_{SU}	Register setup time		3.5		ns
t_{H}	Register hold time		3.5		ns
t_{IC}	Array clock delay			7.5	ns
t_{ICS}	Global clock delay			2.0	ns
t_{FD}	Feedback delay			1.0	ns
t_{CLR}	Register clear time			8.5	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) See *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book for additional internal timing parameters.

(3) The non-Turbo adder must be added to this parameter when the Turbo Bit is off.

(4) Measured with eight outputs switching.

(5) Sample-tested only for an output change of 500 mV.

(6) Measured with a device programmed as a 16-bit counter.

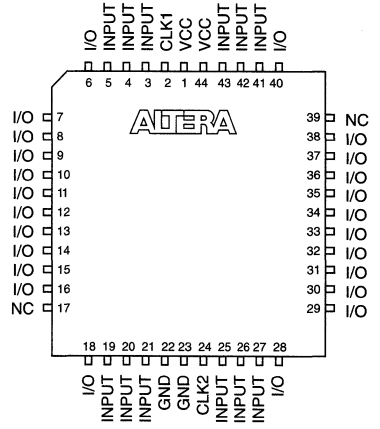
(7) Sample tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.

Features

- High-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 12 ns
  - Counter frequencies of up to 76.9 MHz
  - Pipelined data rates of up to 125 MHz
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- EP910, EP910I, and EP900I devices that are pin-, function, and programming file- compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 11):
  - 44-pin plastic J-lead chip carrier (PLCC)
  - 40-pin ceramic and plastic dual in-line packages (CerDIP and PDIP)

Figure 11. EP910 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



44-Pin PLCC

EP910
EP910I

40-Pin DIP

EP910
EP910I

8 Classic

General Description

The Altera EP910 EPLD can implement up to 900 equivalent gates of small-scale integration (SSI) and medium-scale integration (MSI) logic functions. The EP910 has 24 macrocells, 12 dedicated input pins, 24 I/O pins, and 2 global clock pins (see Figure 12). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. The CLK1 and CLK2 signals are the dedicated clock inputs for the registers in macrocells 13 through 24 and 1 through 12, respectively.

Figure 12. EP910 Block Diagram

Numbers without parentheses are for DIP packages. Numbers in parentheses are for J-lead packages.

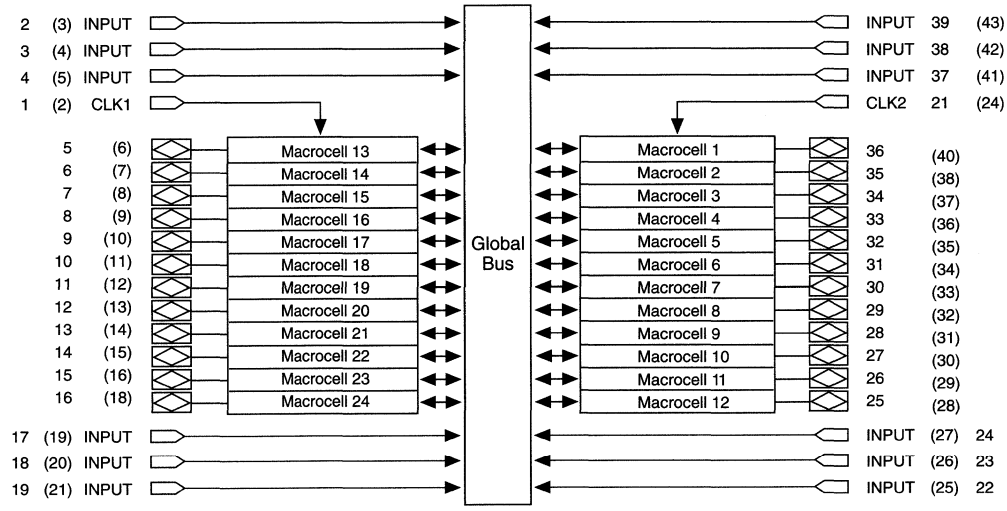


Figure 13 shows typical supply current (I_{CC}) versus frequency for EP910 devices.

Figure 13. I_{CC} vs. Frequency of EP910 Devices

EP910 EPLDs

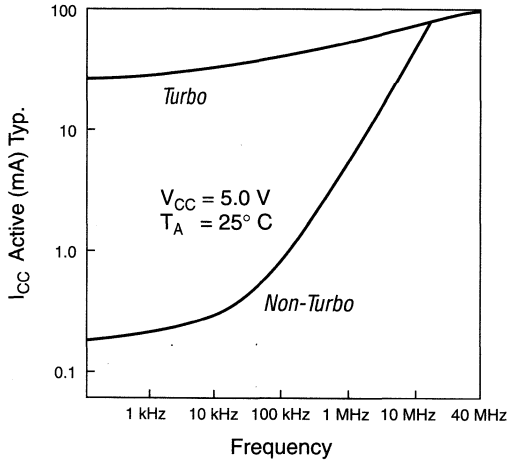
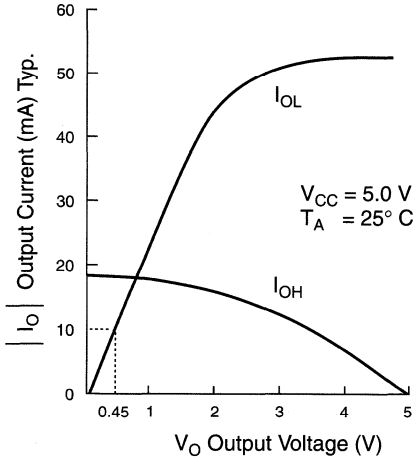


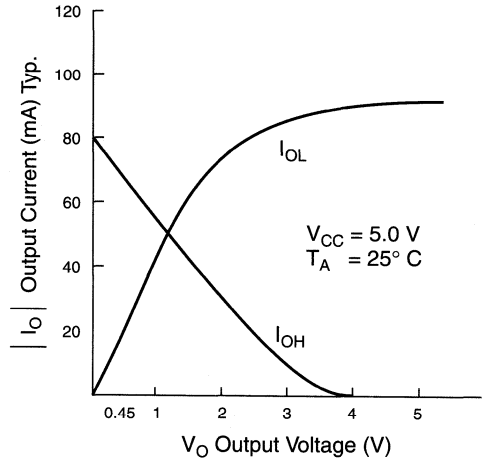
Figure 14 shows the output drive characteristics of EP910 devices.

Figure 14. Output Drive Characteristics of EP910 Devices

EP910 EPLDs



EP910I EPLDs



EP910 & EP910I Device Absolute Maximum Ratings *Note (1)*

			EP910		EP910I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	*Notes (2), (3)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage	*Notes (2), (3)*	–2.0	7.0	–0.5	V_{CC} + 0.5	V
I_{MAX}	DC V_{CC} or GND current		–250	250			mA
I_{OUT}	DC output current, per pin		–25	25			mA
P_D	Power dissipation			1,200			mW
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	*Note (4)*	–65	135	–10	85	° C
T_J	Junction temperature	Ceramic packages, under bias		150		150	° C
		Plastic packages, under bias		135		135	° C

EP910 & EP910I Device Recommended Operating Conditions *Note (5)*

			EP910		EP910I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	*Note (6)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
T_A	Operating temperature	For industrial use	–40	85			° C
t_R	Input rise time	*Note (7)*		100 (50)		500	ns
t_F	Input fall time	*Note (7)*		100 (50)		500	ns

EP910 & EP910I Device DC Operating Conditions *Notes (5), (8), (9)*

Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (10)*	2.4		V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC, *Note (10)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (10)*		0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or GND	–10	10	µA

EP910 & EP910I Device Capacitance *Notes (8), (11)*

			EP910		EP910I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		8	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		12	pF

EP910 & EP910I Device I_{CC} Supply Current *Notes (5), (8), (9)*

			EP910			EP910I			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or GND, no load, *Notes (12), (13)*		20	150		60	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Note (13)*		6	20		4	12	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Note (13)*		45	80 (100)		120	150	mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Voltage with respect to ground.
(3) For EP910 EPLDs, the minimum DC input is –0.3 V; for EP910I EPLDs, the minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(4) Under bias. Extended temperature versions are also available.
(5) Numbers in parentheses are for industrial-temperature-range versions.
(6) Maximum V_{CC} rise time for EP910 devices = 50 ms; for EP910I devices, maximum V_{CC} rise time is unlimited with monotonic rise.
(7) For all clocks: t_R and t_F = 100 ns (50 ns for the industrial-temperature-range version).
(8) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(9) Typical values are T_A = 25° C and V_{CC} = 5 V.
(10) This parameter does not apply to EP910I devices. The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(11) For EP910 devices: capacitance measured at 25° C; sample-tested devices only; clock-pin capacitance for dedicated clock inputs only; pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF. Values for EP910I devices are evaluated during initial characterization and design modifications.
(12) When the Turbo Bit is not set (non-Turbo mode), an EP910 device will enter standby mode if no logic transitions occur for 100 ns after the last transition, and an EP910I device will enter standby mode if no logic transitions occur for 75 ns after the last transition.
(13) Measured with a device programmed as a 24-bit counter.

EP910 Device AC Operating Conditions *Notes (1), (2)*

External Timing Parameters			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		30		35		40	30	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		33		38		43	30	ns
t_{PZX}	Input to output enable	C1 = 35 pF		30		35		40	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (4)*		30		35		40	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		33		38		43	30	ns
f_{MAX}	Maximum frequency	*Note (5)*	41.7		37		32.3		0	MHz
t_{SU}	Global clock input setup time		24		27		31		30	ns
t_{H}	Global clock input hold time		0		0		0		0	ns
t_{CH}	Global clock high time		12		13		15		0	ns
t_{CL}	Global clock low time		12		13		15		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		18		21		24	0	ns
t_{CNT}	Global clock minimum clock period			30		35		40	0	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	33.3		28.6		25		0	MHz
t_{ASU}	Array clock input setup time		10		10		10		30	ns
t_{AH}	Array clock input hold time		15		15		15		0	ns
t_{ACH}	Array clock high time		15		16		17		0	ns
t_{ACL}	Array clock low time		15		16		17		0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (7)*	1		1		1			ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		33		38		43	30	ns
t_{ACNT}	Array clock minimum clock period			30		35		40	0	ns
f_{ACNT}	Max. internal array clock frequency	*Note (6)*	33.3		28.6		25		0	MHz

Internal Timing Parameters			EP910-30		EP910-35		EP910-40		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			9		10		13	ns
t_{IO}	I/O input pad and buffer delay			3		3		3	ns
t_{LAD}	Logic array delay			14		16		17	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		7		9		10	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		7		9		10	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		9		10	ns
t_{SU}	Register setup time		12		13		15		ns
t_{H}	Register hold time		12		12		12		ns
t_{IC}	Array clock delay			17		19		20	ns
t_{ICS}	Global clock delay			2		2		1	ns
t_{FD}	Feedback delay			4		6		8	ns
t_{CLR}	Register clear time			17		19		20	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°C$ to $70°C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°C$ to $85°C$ for industrial use.

(2) See *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* for additional internal timing parameters.

(3) The non-Turbo adder must be added to this parameter when the Turbo Bit is off.

(4) Sample-tested only for an output change of 500 mV.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Measured with a device programmed as a 24-bit counter. I_{CC} is measured at 0°C.

(7) Sample tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.

EP910I Device AC Operating Conditions *Notes (1), (2)*

External Timing Parameters			EP910I-12		EP910I-15		EP910I-25		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output, *Note (4)*			12		15		25	40	ns
t_{PD2}	I/O input to non-registered output			12		15		25	40	ns
t_{PZX}	Input to output enable, *Note (5)*			15		18		28	40	ns
t_{PXZ}	Input to output disable, *Note (5)*			15		18		28	40	ns
t_{CLR}	Asynchronous output clear time			15		18		28	40	ns
f_{MAX}	Global clock maximum frequency		125		100		62.5		0	MHz
t_{SU}	Global clock input setup time		8		11		16		40	ns
t_{H}	Global clock input hold time		0		0		0		0	ns
t_{CH}	Global clock high time		5		6		10		0	ns
t_{CL}	Global clock low time		5		6		10		0	ns
t_{CO1}	Global clock to output delay, *Note (6)*			8		9		14	0	ns
t_{CNT}	Global clock minimum clock period			13		15		25	40	ns
f_{CNT}	Max. internal global clock frequency *Note (6)*		76.9		66.6		40		0	MHz
t_{ASU}	Array clock input setup time		0		2		8		40	ns
t_{AH}	Array clock input hold time		8		9		8			ns
t_{ACH}	Array clock high time		6		7.5		12.5			ns
t_{ACL}	Array clock low time		6		7.5		12.5			ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (7)*	1		1		1			ns
t_{ACO1}	Array clock to output delay, *Note (6)*			16		18		22	40	ns
t_{ACNT}	Array clock minimum clock period			13		15		25	40	ns
f_{ACNT}	Max. internal array clock frequency *Note (6)*		76.9		66.6		40			MHz

Internal Timing Parameters			EP910I-12		EP910I-15		EP910I-25		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2		3		2	ns
t_{IO}	I/O input pad and buffer delay			0		0		0	ns
t_{LAD}	Logic array delay			8		9		17	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		2		3		6	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		6		9	ns
t_{SU}	Register setup time		4		5		5		ns
t_{H}	Register hold time		4		6		11		ns
t_{IC}	Array clock delay			12		12		14	ns
t_{ICS}	Global clock delay			4		3		6	ns
t_{FD}	Feedback delay			1		1		3	ns
t_{CLR}	Register clear time			11		12		20	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°C$ to $70°C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°C$ to $85°C$ for industrial use.

(2) See *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book for additional internal timing parameters.

(3) If the device is inactive for more than 75 ns while operated in non-Turbo mode, the non-Turbo adder must be added to this parameter. See "Turbo Bit" on page 357 of this data sheet.

(4) Measured with eight outputs switching.

(5) The t_{PZX} and t_{PXZ} parameters are measured at ± 0.5 V from steady-state voltage as driven by the specified output load.

(6) Measured with device programmed as a 24-bit counter.

(7) Sample tested only. This parameter is a guideline based on extensize device characterization. This parameter applies for both global and array clocking.

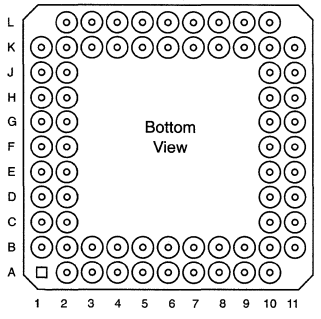
Notes:

Features

- High-performance, 48-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 20 ns
  - Counter frequencies of up to 50 MHz
  - Pipelined data rates of up to 62.5 MHz
- Programmable I/O architecture with up to 64 inputs or 48 outputs
- EP1810 and EP1800I devices that are pin-, function-, and programming file-compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in 68-pin windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 15)
  - Pin-grid array package (ceramic PGA only)
  - Plastic J-lead chip carrier (PLCC)

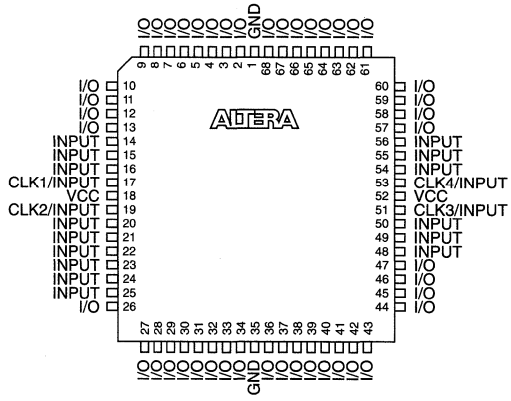
Figure 15. EP1810 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Table 2 on page 389 in this data sheet for PGA package pin-out information. Windows in ceramic packages only.



68-Pin PGA

EP1810



68-Pin PLCC

EP1810

8 Classic

General Description

The Altera EP1810 EPLD offers large-scale integration (LSI) density, TTL-equivalent speed, and low power consumption. The EP1810 has 48 macrocells, 16 dedicated input pins, and 48 I/O pins (see Figure 16). The EP1810 is divided into four quadrants, each containing 12 macrocells. Of the 12 macrocells in each quadrant, 8 have quadrant feedback and are "local" macrocells (see "Feedback Selection" on page 353 of this data sheet for more information). The remaining 4 macrocells in the quadrant are "global" macrocells. Both local and global macrocells can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of the feedbacks from the global macrocells.

The EP1810 also has four dedicated inputs (one in each quadrant) that can be used as quadrant clock inputs. If the dedicated input is used as a clock pin, the input feeds the clock input of all registers in that particular quadrant.

Figure 16. EP1810 Block Diagram

Numbers without parentheses are for J-lead packages. Numbers with parentheses are for PGA packages.

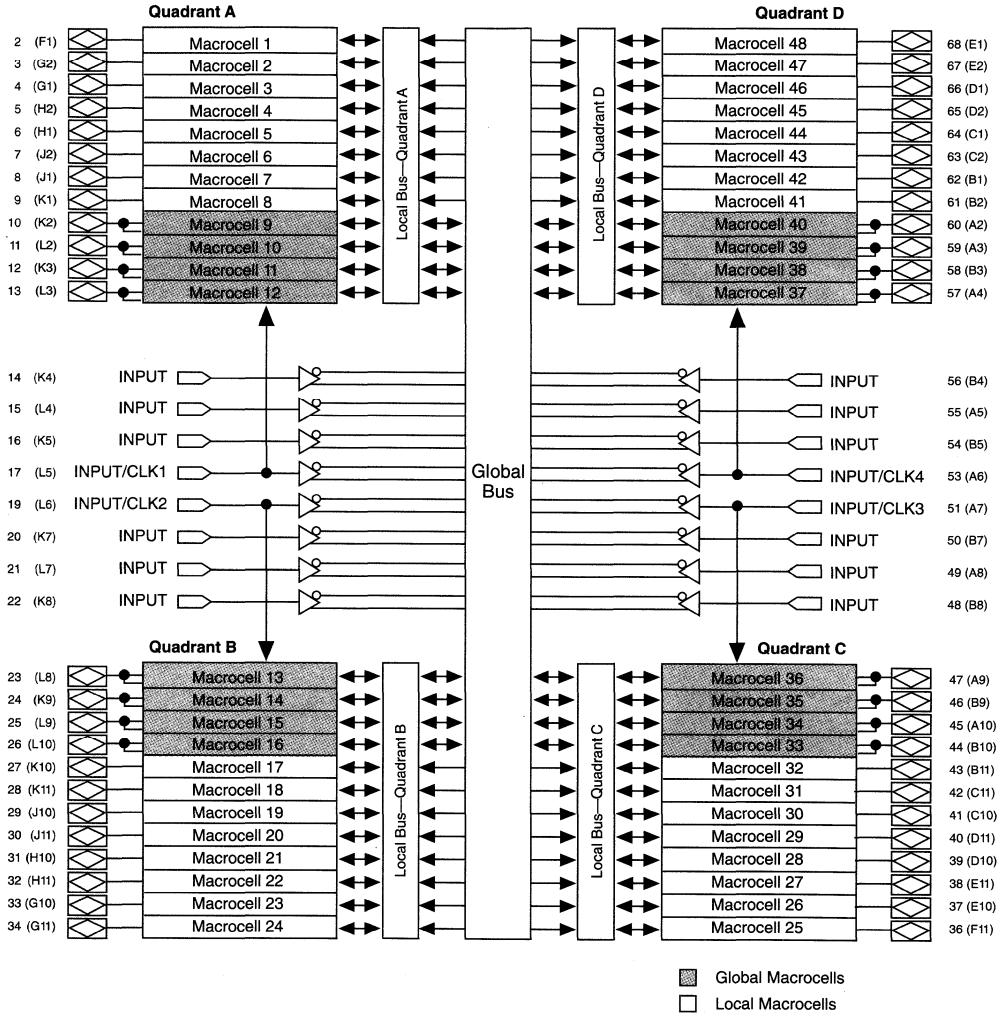


Figure 17 shows the typical supply current (I_{CC}) versus frequency for the EP1810 EPLDs.

Figure 17. I_{CC} vs. Frequency of EP1810 Devices

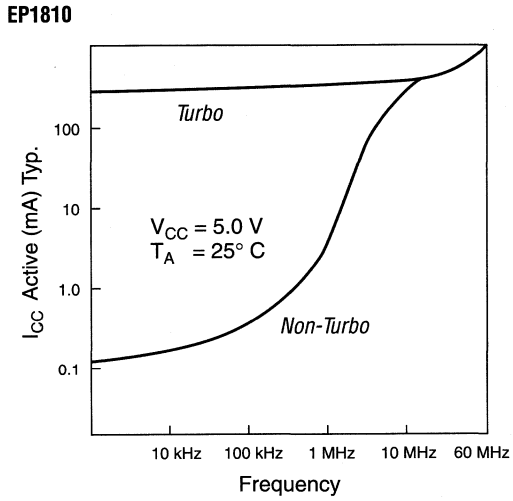
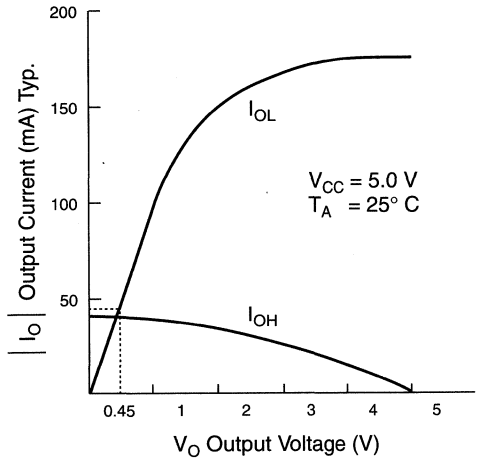


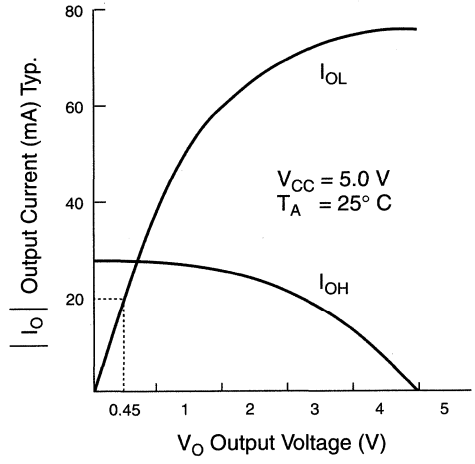
Figure 18 shows the output drive characteristics of EP1810 devices.

Figure 18. Output Drive Characteristics of EP1810 Devices

EP1810-20 & EP1810-25 EPLDs



EP1810-35 & EP1810-45 EPLDs



EP1810 Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Notes (2), (3)*	–2.0 (–0.5)	7.0	V
V_I	DC input voltage	With respect to GND, *Notes (2), (3)*	–2.0 (–0.5)	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300 (–400)	300 (400)	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1,500 (2,000)	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65 (–55)	135 (125)	° C
T_J	Junction temperature	Under bias		(150)	° C

EP1810 Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (2), (4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time	*Note (5)*		50	ns
t_F	Input fall time	*Note (5)*		50	ns

EP1810 Device DC Operating Conditions *Notes (2), (6), (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (8)*	2.4		V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC, *Note (8)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (8)*		0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or GND	–10	10	µA

EP1810 Device Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

EP1810 Device I_{CC} Supply Current *Notes (2), (6), (7)*

				EP1810			
Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or GND, I/O = 0 Notes (10), *(11)*	-20, -25		50	150	µA
			-35, -45		35	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or GND no load, f = 1.0 MHz *Notes (2), (10), (11), (12)*	-20, -25		20	40	mA
			-35, -45		10	30 (40)	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	V_I = V_{CC} or GND, no load f = 1.0 MHz *Notes (2), (10), (12)*	-20, -25		180	225 (250)	mA
			-35, -45		100	180 (240)	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Numbers in parentheses are for industrial-temperature-range versions.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(4) Maximum V_{CC} rise time is 50 ms.
(5) For EP1810 clocks: t_R and t_F = 100 ns (50 ns for industrial-temperature-range versions).
(6) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(7) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(8) Tested at 25° C and 125° C only. The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(9) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. Pin 19 has a maximum capacitance of 160 pF.
(10) Measured with a device programmed as four 12-bit counters. I_{CC} measured at 0° C.
(11) Tested at 25° C only.
(12) Tested with non-output loading using a data pattern specified by Altera. The data path is correlated to four 12-bit counters.

EP1810-20 & EP1810-25AC Device Operating Conditions *Note (1)*

External Timing Parameters			EP1810-20		EP1810-25		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	25	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		22		28	25	ns
t_{SU}	Global clock setup time		13		17		25	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		15		18	0	ns
t_{CH}	Global clock high time		8		10		0	ns
t_{CL}	Global clock low time		8		10		0	ns
t_{ASU}	Array clock setup time		8		10		25	ns
t_{AH}	Array clock hold time		8		10		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	25	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (6)*	1		1		0	ns
t_{CNT}	Minimum global clock period			20		25	0	ns
f_{CNT}	Maximum internal frequency	*Note (3)*	50		40		0	MHz
f_{MAX}	Maximum clock frequency	*Note (4)*	62.5		50		0	MHz

Internal Timing Parameters			EP1810-20		EP1810-25		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{IN}	Input pad and buffer delay			5		7	0	ns
t_{IO}	I/O input pad and buffer delay			2		3	0	ns
t_{LAD}	Logic array delay			9		12	25	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		6	0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		6		6	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (4)*		6		6	0	ns
t_{SU}	Register setup time		8		10		0	ns
t_{H}	Register hold time		5		10		0	ns
t_{IC}	Array clock delay			9		12	25	ns
t_{ICS}	Global clock delay			4		5	0	ns
t_{FD}	Feedback delay			3		3	–25	ns
t_{CLR}	Register clear time			9		12	25	ns

EP1810-35 & EP1810-45 Device AC Operating Conditions *Note (1)*

External Timing Parameters			EP1810-35		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		35		45	30	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		50	30	ns
t_{SU}	Global clock setup time		25		30		30	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		20		25	0	ns
t_{CH}	Global clock high time		12		15		0	ns
t_{CL}	Global clock low time		12		15		0	ns
t_{ASU}	Array clock setup time		10		11		30	ns
t_{AH}	Array clock hold time		15		18		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		35		45	30	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (6)*	1		1			ns
t_{CNT}	Minimum global clock period			35		45	0	ns
f_{CNT}	Maximum internal frequency	*Note (3)*	28.6		22.2		0	MHz
f_{MAX}	Maximum clock frequency	*Note (5)*	40		33.3		0	MHz

Internal Timing Parameters			EP1810-35		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{IN}	Input pad and buffer delay			7		6	0	ns
t_{IO}	I/O input pad and buffer delay			5		5	0	ns
t_{LAD}	Logic array delay			19		28	30	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		9		11	0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		9		11	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (5)*		9		11	0	ns
t_{SU}	Register setup time		10		10		0	ns
t_{H}	Register hold time		15		18		0	ns
t_{IC}	Array clock delay			19		28	30	ns
t_{ICS}	Global clock delay			4		8	0	ns
t_{FD}	Feedback delay			6		7	–30	ns
t_{CLR}	Register clear time			24		32	30	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) The non-Turbo adder must be added to this parameter when the Turbo Bit is off.

(3) Measured with a device programmed as four 12-bit counters. I_{CC} measured at 0° C.

(4) Sample-tested only for an output change of 500 mV.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

(6) Sample tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for boith global and array clocking.

Pin-Out Information

Table 2 provides pin-out information for EP1810 devices in PGA packages.

Table 2. EP1810 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	GND	K4	INPUT
A3	I/O	B10	I/O	F11	I/O	K5	INPUT
A4	I/O	B11	I/O	G1	I/O	K6	VCC
A5	INPUT	C1	I/O	G2	I/O	K7	INPUT
A6	CLK4/INPUT	C2	I/O	G10	I/O	K8	INPUT
A7	CLK3/INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	CLK1/INPUT
B4	INPUT	E2	I/O	J10	I/O	L6	CLK2/INPUT
B5	INPUT	E10	I/O	J11	I/O	L7	INPUT
B6	VCC	E11	I/O	K1	I/O	L8	I/O
B7	INPUT	F1	I/O	K2	I/O	L9	I/O
B8	INPUT	F2	GND	K3	I/O	L10	I/O

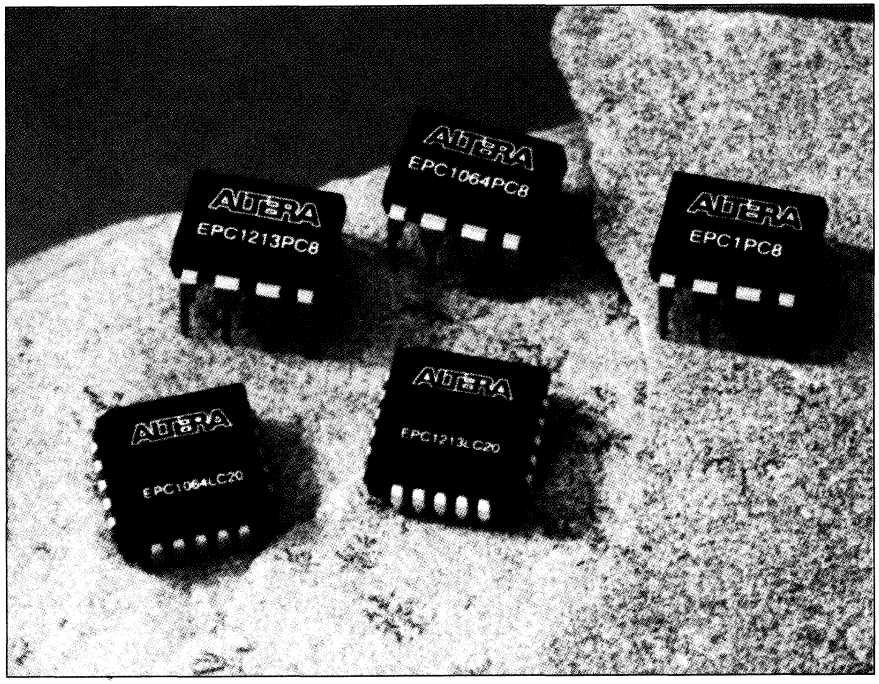
Notes:

Configuration EPROMs

Contents

June 1996

Configuration EPROMs for FLEX Devices Data Sheet


ALTERA
EPC1064PC8
ALTERA
EPC1213PC8
ALTERA
EPC1PC8
ALTERA
EPC1064LC20
ALTERA
EPC1213LC20

Configuration EPROMs
for FLEX Devices

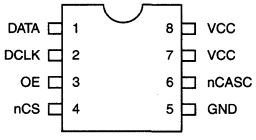
June 1996, ver. 5 — Data Sheet

Features

- Serial EPROM family for configuring FLEX devices
- Simple, easy-to-use 4-pin interface to FLEX devices
- Low current during configuration and near-zero standby current
- 5.0-V and 3.3-V operation
- Software design support with Altera's MAX+PLUS II development system for 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from Data I/O and other manufacturers
- Available in compact, one-time-programmable (OTP) plastic packages (see Figure 1)
  - 8-pin plastic dual in-line package (PDIP)
  - 20-pin plastic J-lead chip carrier package (PLCC)
  - 32-pin plastic thin quad flat pack (TQFP)

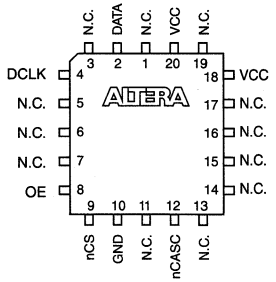
Figure 1. Configuration EPROM Package Pin-Out Diagrams

Package outlines not drawn to scale.



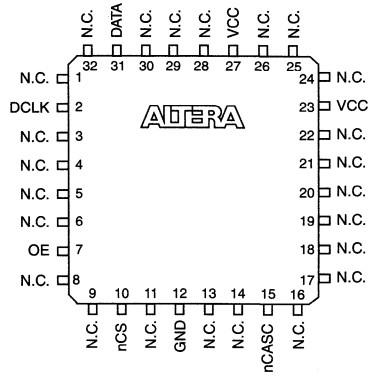
8-Pin PDIP

EPC1
EPC1V
EPC1064
EPC1064V
EPC1213



20-Pin PLCC

EPC1
EPC1V
EPC1064
EPC1064V
EPC1213



32-Pin TQFP

EPC1064
EPC1064V

9 Configuration EPROMs

Functional Description

In SRAM-based devices, configuration data must be reloaded each time the system initializes, or whenever new configuration data is needed. Altera's serial Configuration EPROMs store configuration data for SRAM-based Altera FLEX devices. Table 1 lists the Configuration EPROMs provided by Altera.

Table 1. Configuration EPROMs

Device	Description
EPC1	1,046,496 × 1 bit device with 5.0-V operation
EPC1V	1,046,496 × 1 bit device with 3.3-V operation
EPC1064	65,536 × 1 bit device with 5.0-V operation
EPC1064V	65,536 × 1 bit device with 3.3-V operation
EPC1213	212,942 × 1 bit device with 5.0-V operation

Table 2 shows the appropriate Configuration EPROM for each FLEX device.

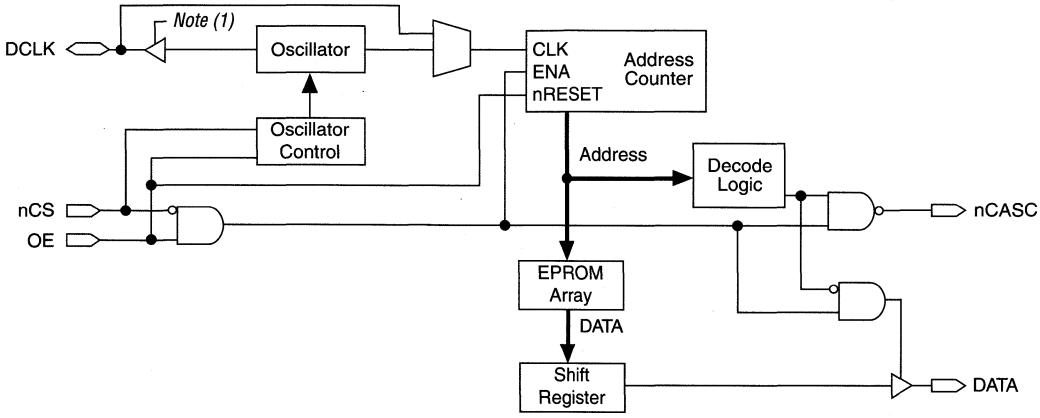
Table 2. Appropriate Configuration EPROM for Each FLEX Device

FLEX Device	Configuration EPROM
EPF10K10	EPC1
EPF10K20	EPC1
EPF10K30	EPC1
EPF10K40	EPC1
EPF10K50	EPC1
EPF10K70	EPC1
EPF10K100	Two EPC1 devices
EPF8282A	EPC1 or EPC1064
EPF8282AV	EPC1V or EPC1064V
EPF8452A	EPC1 or EPC1064
EPF8636A	EPC1 or EPC1213
EPF8820A	EPC1 or EPC1213
EPF81188A	EPC1 or EPC1213
EPF81500A	EPC1 or two EPC1213 devices

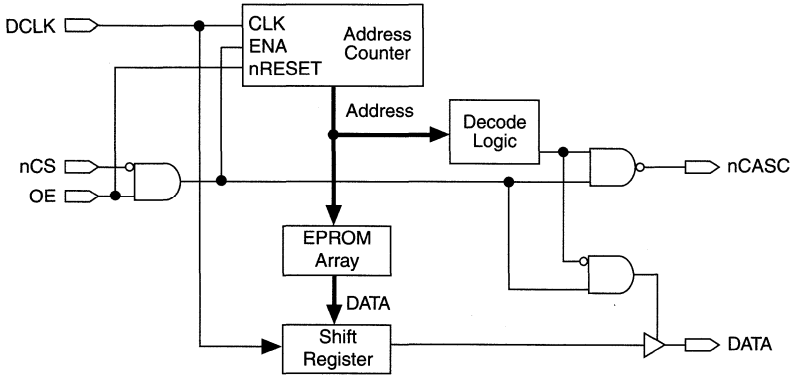
Figure 2 shows block diagrams of the Configuration EPROM devices.

Figure 2. Configuration EPROM Block Diagram

EPC1



EPC1064 & EPC1213



Note:

(1) This output enable controls the operation of the DCLK pin on the EPC1 device. The operation of the DCLK pin is determined by the configuration mode programmed into the EPC1 device.

Device Configuration

The control signals for Configuration EPROMs—nCS, OE, and DCLK—interface directly to the FLEX device control signals. All FLEX devices can control the entire configuration process and retrieve data from the Configuration EPROM without requiring an external intelligent controller.

The configuration EPROM device's OE and nCS pins control the tri-state buffer on the DATA output pin and enable the address counter (and the oscillator in the EPC1 device). When OE is driven low, the Configuration EPROM device resets the address counter and tri-states its DATA pin. For the EPC1, the device determines its operation mode and whether it should use FLEX 10K or FLEX 8000 protocols when OE is driven high again. The nCS pin controls timing. If nCS is held high after the OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is driven low, the counter and the DATA output pin are enabled. When OE is driven low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of nCS.

When the Configuration EPROM has driven out all of its data and nCASC is driven low, the device tri-states the DATA pin to avoid contention with other Configuration EPROMs. Upon power-up, the address counter is automatically reset.

FLEX 10K Device Configuration

FLEX 10K devices can be configured with the EPC1 Configuration EPROM. The EPC1 device stores configuration data in its EPROM array and clocks the data out serially with its internal oscillator. The OE, nCS, and DCLK pins supply the control signals for the address counter and the output tri-state buffer. The EPC1 device sends a serial bitstream of configuration data to its DATA pin, which is routed to the DATA0 input pin on the FLEX 10K device.

When configuration data for a FLEX 10K device exceeds the capacity of a single EPC1 device, multiple EPC1 devices can be linked together serially. When multiple EPC1 devices are required, the nCASC and nCS pins provide handshaking between the EPC1 devices. The position of an EPC1 device in a chain determines its operation. The first EPC1 device in the Configuration EPROM chain is powered up or reset with nCS low and is configured for FLEX 10K protocol. The first EPC1 device supplies all clock pulses to one or more FLEX 10K devices and to any downstream EPC1 devices during configuration. The first EPC1 device also provides the first stream of data to the FLEX 10K devices during multi-device configuration. Once this EPC1 device finishes sending configuration data, it drives its nCASC pin low, which drives the nCS pin of the next EPC1 device in the chain low, activating the next EPC1 device. The first EPC1 device clocks all subsequent EPC1 devices until configuration is complete. Once all configuration data is transferred and nCS is driven high by CONF_DONE on the FLEX 10K device, the first EPC1 device clocks 16 additional cycles to initialize the FLEX 10K device, and then goes into Zero-power (idle) state. If nCS is driven high before all configuration data is transferred, the nSTATUS pin is pulled low, indicating a configuration error.

All downstream EPC1 devices in the Configuration EPROM chain are powered up or reset when nCS goes high and the device is configured for FLEX 10K protocol. Downstream EPC1 devices are clocked by the first EPC1 device. Each downstream EPC1 supplies configuration data after its nCS pin is driven low by the previous EPC1 device's nCASC pin. This EPC1 device then activates the next EPC1 device in the configuration chain. An inactive downstream EPC1 device waits in a zero-power (idle) state.

Table 3 describes EPC1 and EPC1V pin functions during FLEX 10K device configuration.

Table 3. EPC1 & EPC1V Pin Functions during FLEX 10K Device Configuration

Pin Name	Pin Number		Pin Type	Description
	8-Pin PDIP	20-Pin PLCC		
DATA	1	2	Output	Serial data output.
DCLK	2	4	I/O	Clock output or clock input. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the OE input is held high, the nCS input is held low, and all configuration data has not been transferred to the target device (otherwise, in FLEX 10K master mode, the DCLK pin drives low.)
OE	3	8	Input	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count. In FLEX 10K mode, if this pin is low (reset), the internal oscillator becomes inactive and DCLK drives low.
nCS	4	9	Input	Chip select input (active low). A low input allows DCLK to increment the address counter and enables DATA to drive out. If the EPC1 is reset with nCS low, the device initializes as the first device in a daisy-chain. If the EPC1 is reset with nCS high, the device initializes as a subsequent EPC1 device in the chain.
nCASC	6	12	Output	Cascade select output (active low). This output goes low when the address counter has reached its maximum value. In a daisy-chain of EPC1 devices, the nCASC pin of one device is usually connected to the nCS input pin of the next device in the chain, which permits DCLK to clock data from the next EPC1 device in the chain.
GND	5	10	Ground	A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.
VCC	7, 8	18, 20	Power	Power pin.

FLEX 8000 Device Configuration

FLEX 8000 devices have internal oscillators that can provide a DCLK signal to the Configuration EPROM. The Configuration EPROM device sends configuration data out as a serial bitstream on the DATA output pin. This data is routed into the FLEX 8000 device via the DATA0 input pin. The nCASC and nCS pins provide handshaking between multiple Configuration EPROMs, allowing several linked Configuration EPROM devices to serially configure multiple FLEX devices. FLEX 8000 devices can be configured with the EPC1, EPC1064, or EPC1213 Configuration EPROMs.

Configuration with EPC1

The EPC1 can replace the EPC1064 and EPC1213 Configuration EPROMs, which are also used to configure FLEX 8000 devices. EPC1 devices automatically emulate the EPC1064 or EPC1213 when it is programmed with the appropriate Programmer Object File (**.pof**). When the EPC1 device is programmed with a POF, the FLEX 8000 device drives the EPC1 device's OE pin high and clocks the EPC1 device. One EPC1 device can store more configuration data than either the EPC1064 or EPC1213 device. Therefore designers can use one type of Configuration EPROM, the EPC1, for all FLEX devices.

Configuration with EPC1064 & EPC1213

FLEX 8000 device configuration with EPC1064 and EPC1213 Configuration EPROMs is described under "Device Configuration" on page 395. Table 4 describes the pin functions of the EPC1, EPC1213, and EPC1064 during FLEX 8000 device configuration.

Table 4. Configuration EPROM Pin Functions during FLEX 8000 Device Configuration

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP	20-Pin PLCC	32-Pin TQFP *Note (1)*		
DATA	1	2	31	Output	Serial data output.
DCLK	2	4	2	Input	Clock input. Rising edges on DCLK increment the internal address counter and cause the next bit of data to be presented on DATA. The counter is incremented only if the OE input is held high and the nCS input is held low.
OE	3	8	7	Input	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count.
nCS	4	9	10	Input	Chip-select input (active low). A low input allows DCLK to increment the address counter and enables DATA.
nCASC	6	12	15	Output	Cascade-select output (active low). This output goes low when the address counter has reached its maximum value. The nCASC output is usually connected to the nCS input of the next Configuration EPROM in a daisy-chain, so the next DCLK clocks data out of the next Configuration EPROM.
GND	5	10	12	Ground	A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.
VCC	7, 8	18, 20	23, 27	Power	Power pin.

Note:
(1) EPC1064 and EPC1064V devices only.

Active serial (AS) and multi-device sequential active serial (MD-SAS) configuration schemes use an EPC1 Configuration EPROM as a data source for FLEX 8000 devices.

For information on FLEX 10K and FLEX 8000 devices and how to configure them, see the following documents:

- *FLEX 10K Embedded Programmable Logic Family Data Sheet*
- *FLEX 8000 Programmable Logic Device Family Data Sheet*
- *Application Note 59 (Configuring FLEX 10K Devices)*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

MAX+PLUS II Support

The MAX+PLUS II development system provides programming support for Altera Configuration EPROMs. The MAX+PLUS II software automatically generates a Programmer Object File (**.pof**) for every Configuration EPROM in a project. In a multi-device project, MAX+PLUS II can combine the programming files for multiple FLEX devices into one or more Configuration EPROMs. MAX+PLUS II allows you to select the appropriate Configuration EPROM to most efficiently store the data for each FLEX device.

The POF includes a preamble, cyclic redundancy code (CRC), and synchronization data that allow it to be used in a serial bitstream. The POF is programmed into the Configuration EPROM with MAX+PLUS II and a Configuration EPROM programming adapter. Many programming hardware manufacturers, including Data I/O, support programming of Configuration EPROMs.

For more information on programming hardware, see the *Altera Programming Hardware Data Sheet* and *Programming Hardware Manufacturers* in this data book.

Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND *Note (2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			20	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			100	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage for 5.0-V device		4.75	5.25	V
	Supply voltage for 3.3-V device		3.0	3.6	V
V_I	Input voltage	With respect to GND, *Note (2)*	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V device high-level TTL output voltage	I_{OH} = –4 mA DC, *Note (5)*	2.4		V
	3.3-V device high-level TTL output voltage	I_{OH} = –0.1 mA DC, *Note (5)*	V_{CC} – 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (5)*		0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10	10	µA

EPC1064, EPC1064V & EPC1213 Device I_{CC} Supply Current Values *Note (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			100		µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 6 MHz		10		mA

EPC1 & EPC1V Device I_{CC} Supply Current Values *Note (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			50	100	µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 10 MHz		10	50	mA

Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

FLEX 10K Device Configuration Timing Parameters Using EPC1 *Note (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CE}	OE high to first clock delay				200	ns
t_{OEZX}	OE high to data output enabled				160	ns
t_{CO}	DCLK to data out delay				30	ns
t_{MCH}	DCLK high time in master mode		30	50		ns
t_{MCL}	DCLK low time in master mode		30	50		ns
t_{SCH}	DCLK high time in slave mode		30			ns
t_{SCL}	DCLK low time in slave mode		30			ns
t_{CASC}	CLK rising edge to nCASC				20	ns
t_{CCA}	nCS to nCASC cascade delay				10	ns
f_{CDOE}	CLK to data enable/disable				30	ns
t_{OEC}	OE low to CLK disable delay				45	ns
t_{OH}	DATA hold from CLK rising edge		0		10	ns
t_{NRCAS}	OE low (reset) to nCASC delay				25	ns
t_{NRR}	OE low time (reset) minimum		100			ns

FLEX 8000 Device Configuration Timing Parameters Using EPC1, EPC1V, EPC1064, EPC1064V & EPC1213

			EPC1064V		EPC1064 EPC1213		EPC1 *Note (6)*		EPC1V *Note (6)*		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{OEZX}	OE high to DATA output enabled			75		50		50			ns
t_{CSZX}	nCS low to DATA output enabled			75		50		50			ns
t_{CSXZ}	nCS high to DATA output disabled			75		50		50			ns
t_{CSS}	nCS low setup time to first DCLK rising edge		150		100		50				ns
t_{CSH}	nCS low hold time after DCLK rising edge		0		0		0				ns
t_{DSU}	Data setup time before rising edge on DCLK, *Note (8)*		75		50		50				ns
t_{DH}	Data hold time after rising edge on DCLK, *Note (8)*		0		0		0				ns
t_{CO}	DCLK to DATA out delay, *Note (6)*			100		75		75			ns
t_{CK}	Clock period		240		160		100				ns
f_{CK}	Clock frequency			4		6		10			MHz
t_{CL}	DCLK low time		120		80		50				ns
t_{CH}	DCLK high time		120		80		50				ns
t_{XZ}	OE low or nCS high to DATA output disabled			75		50		50			ns
t_{OEW}	OE pulse width to guarantee counter reset		150		100		100				ns
t_{CASC}	Last DCLK + 1 to nCASC low delay			90		60		50			ns
t_{CKXZ}	Last DCLK + 1 to DATA tri-state delay			75		50		50			ns
t_{CEOUT}	nCS high to nCASC high delay			150		100		100			ns

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Typical values are for $T_A = 25°$ C and $V_{CC} = 5.0$ V.
(4) Operating conditions: $V_{CC} = 5.0$ V ± 5%, $T_A = 0°$ C to 70° C for commercial use.
$V_{CC} = 5.0$ V ± 10%, $T_A = -40°$ C to 85° C for industrial use.
(5) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.
(6) Parameters for EPC1 devices are preliminary. Contact Altera Applications for information on EPC1V devices.
(7) Capacitance is sample-tested only.
(8) This parameter applies to FLEX 8000 devices.

Notes:

June 1996

MPLDs: Mask-Programmed Logic Devices Data Sheet


ALTERA
MPF81500AQC240
ALTERA
MPM9560QC240
ALTERA
MPM7256EQC208

MPLDs

Mask-Programmed Logic Devices

June 1996, ver. 4 — Data Sheet

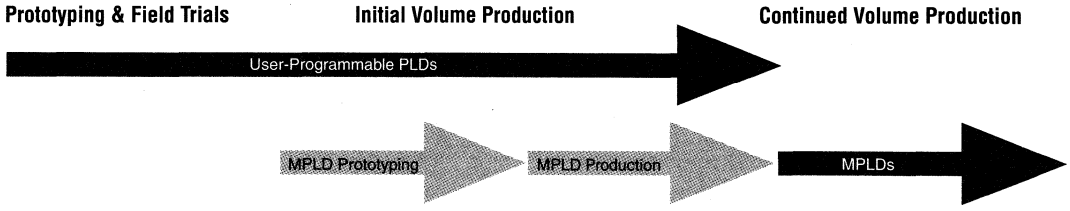
Features

- Masked versions of Altera programmable logic devices (PLDs)
- Reduced cost for high-volume production
- Available for all Altera devices
- Pin-, function-, and timing-compatible with original device
- Conversion process performed by Altera
- Fast turn-around to shorten time-to-market
- Low power consumption

General Description

Altera Mask-Programmed Logic Devices (MPLDs) provide a masked alternative to PLDs. By using a generic CMOS process and removing all programmable cells, Altera passes considerable savings on to customers who anticipate high-volume production. In addition, Altera performs the PLD-to-MPLD conversion so that customer redesign effort is not required. The combination of Altera PLDs and MPLDs provides the best of both worlds: the fast time-to-market of PLDs, and the low cost of MPLDs. See Figure 1.

Figure 1. High-Volume Production Flow with Altera PLDs & MPLDs



MPLD Compatibility

Each Altera MPLD is pin-, function-, and timing-compatible with the original PLD. This compatibility ensures that the MPLD can replace the original Altera device, while providing lower cost and maintaining the production flow. In addition, the MPLD typically consumes less power than the equivalent PLD, depending on the design and operating conditions.

The pin-out and DC specifications of the MPLD will match those of the original device. Altera ensures functional compatibility by mapping the logic within the PLD (for example, product terms, programmable flipflops, etc.) directly to specially designed elements within the MPLD. Altera's proprietary logic synthesis program uses netlist files generated by the MAX+PLUS II software to describe the final synthesis, placement, and routing of the original design. The conversion process accounts for all architecture-specific features—such as wide fan-in product terms, carry chains, and cascade chains—commonly found in programmable logic applications.

Quick, Seamless Conversion

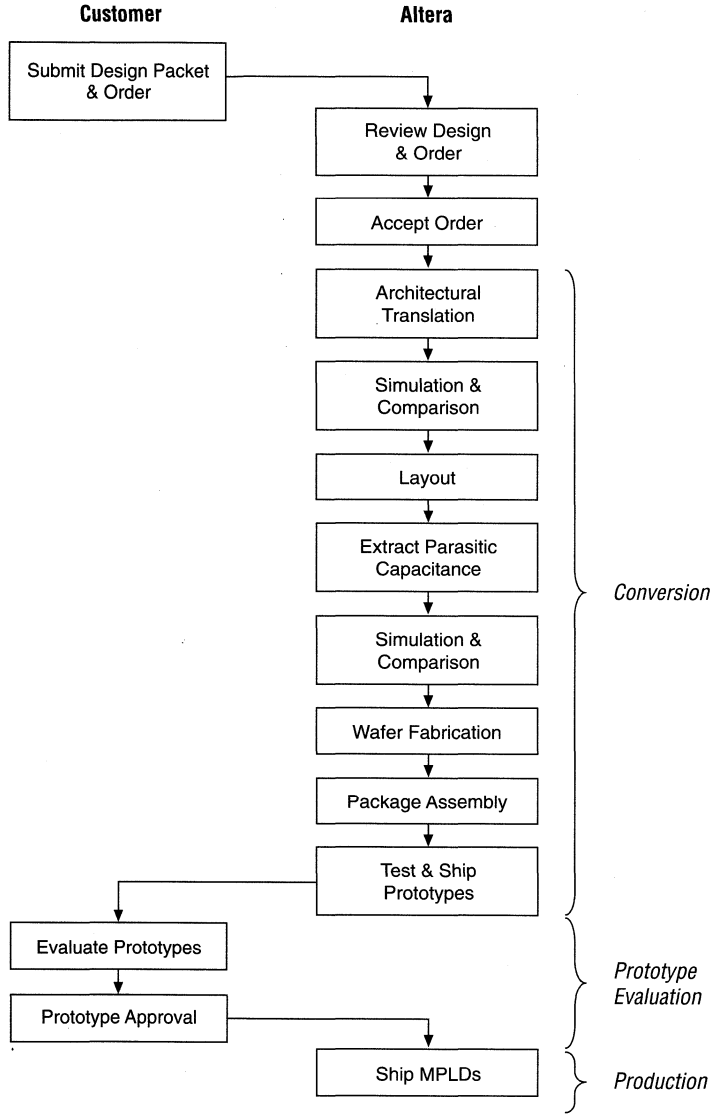
One of the principal objectives of Altera's MPLD conversion program is to minimize the engineering time and resources required for the conversion. The engineer simply submits design files created with the MAX+PLUS II software and Altera delivers MPLDs within weeks of the design sign-off.

The design conversion includes architectural translation, simulation and comparison, layout, extraction of parasitic capacitance, additional simulation and comparison, wafer fabrication, and package assembly.

Go to the ***MPLD Conversion Information & Order Forms*** workbook, available from an Altera sales representative, for the instructions and forms necessary to initiate the PLD-to-MPLD conversion.

The MPLD conversion flow chart shows how easily a programmable Altera device can be converted into an MPLD. See Figure 2.

Figure 2. MPLD Conversion Flow



Conclusion

The two most important design goals for engineers today are reducing time-to-market and minimizing system cost. Together, Altera PLDs and MPLDs provide a solution that addresses these concerns, allowing companies to take products to market quickly, lower the end-product cost, and eliminate the risks associated with ASIC design conversions.

Notes:

Device Operation

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Operating Requirements for Altera Devices Data Sheet

Application Note 74: Evaluating Power for Altera Devices

Application Note 42: Metastability in Altera Devices

Application Note 75: High-Speed Board Designs

Application Note 76: Understanding FLEX 8000 Timing

Application Note 77: Understanding MAX 9000 Timing

Application Note 78: Understanding MAX 7000, MAX 5000 & Classic Timing

Application Note 79: Understanding FLASHlogic Timing

Operating Requirements for Altera Devices

June 1996, ver. 7 Data Sheet

Introduction

Altera devices combine unique programmable logic architectures with advanced CMOS processes to provide exceptional performance and reliability. To maintain the highest possible performance and reliability of Altera devices, system designers must consider the following operating requirements:

- Operating conditions
- Pin voltage levels
- Output loading
- Power-supply management
- Device programming/erasure

Operating Conditions

When Altera devices are implemented in a system, they are rated according to a set of defined parameters. These parameters are provided in each device family data sheet and include absolute maximum ratings, recommended operating conditions, and DC and AC operating conditions.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for a particular Altera device. These values are based on experiments conducted with Altera devices, and on theoretical modeling of breakdown and damage mechanisms. These ratings are stress ratings only. The functional operation of Altera devices is not implied at these conditions or at conditions beyond those indicated in the "Recommended Operating Conditions" tables in device family data sheets. For example, I_{OUT} is the absolute current capacity, not the drive capability of an output pin. The output drive characteristics are given as I_{OH} and I_{OL} in the "DC Operating Conditions" table of each device family data sheet.

Device reliability can be impaired if an Altera device operates for extended periods of time at conditions listed in the "Absolute Maximum Ratings" table of each device family data sheet. Operating the device at conditions that exceed these ratings can permanently damage the device.

Recommended Operating Conditions

The functional operation limits for an Altera device, listed in the "Recommended Operating Conditions" table of each device family data sheet, specify limits for all DC and AC parameters. These parameters are expressed differently in other rating sections. For example, the V_{CC} range specified in the "Recommended Operating Conditions" table is the voltage range for safe device operation, while the V_{CC} range specified in the "Absolute Maximum Ratings" table is the power-supply level beyond which the device can be permanently damaged.

DC Operating Conditions

The steady-state voltage and current values expected from Altera devices are provided in the "DC Operating Conditions" table of each device family data sheet. This information includes input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), current drive characteristics (I_{OH} and I_{OL}), and input and output leakage currents (I_I and I_{OZ}).

AC Operating Conditions

The internal and external timing parameters for an Altera device are listed in the "AC Operating Conditions" table in each device family data sheet. These parameters are determined under the conditions specified in the "Recommended Operating Conditions" table. The internal timing parameters are the delays associated with specific architectural features. Device performance can be estimated by following the signal path from a source to the destination and adding the appropriate internal timing parameters. The external timing parameters are specified as pin-to-pin delays when the device is operating under these conditions.

Timing parameters are specified as maximum, minimum, or typical values. A maximum value indicates that the delay will not exceed the specified time. Setup, hold, and pulse width times are expressed as minimum values that the system must provide to ensure reliable device operation. Expected values based on device characteristics are expressed as typical values; actual values can vary.

Pin Voltage Levels

Device pins can be exposed to dangerous voltages during handling or device operation. During handling, pins can be exposed to high-voltage static discharges that cause electrostatic discharge (ESD) damage. During operation, power-supply spikes on the VCC and GND pins or errant logic levels elsewhere in the system can produce logic-level stress with voltages similar to V_{CC} (0 V to 15 V). To minimize these hazards, the user must observe the precautions specified for the following conditions:

- Pin connections
- Latch-up
- Hot-socketing
- ESD

Pin Connections

During project compilation, the MAX+PLUS II Compiler generates a device utilization report, called a Report File (**.rpt**). The Report File provides information on the pin-outs and connectivity of the device(s) used in the project. The Report File includes a pin-out diagram that shows the user VCC, GND, signal, dedicated function, and unused pins.

The VCC and GND pins should be tied to the V_{CC} or GND planes, respectively, on the printed circuit board (PCB). Dedicated input pins used in a design and I/O pins configured as inputs should always be driven by an active source. I/O pins configured as bidirectional pins should always be driven whenever the I/O pin is used as an input. Unused dedicated input and I/O pins are marked in the Report File as GND and RESERVED, respectively. Unused dedicated inputs should be tied to the GND plane. Otherwise, these pins may "float" in an indeterminate state, possibly increasing DC current in the device and introducing noise into the system. To prevent unused I/O pins from floating, they are driven by an internal signal and are reported as RESERVED. All RESERVED I/O pins should remain unconnected. Tying a RESERVED I/O pin to V_{CC}, GND, or another signal source creates contention that can damage the output driver on the device.

For proper operation, signals on the input and output pins must be in the following range:

$GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$

Latch-Up

Parasitic bipolar transistors, which are present in the fundamental structure of CMOS devices, can create paths in the device for destructive currents. Typically, the base-emitter and base-collector junctions of these parasitic transistors are not forward-biased, so they are not turned on. Figure 1 shows a cross-section of a CMOS wafer and primary parasitic transistors (labeled Q1 and Q2). To ensure that all junctions remain reverse-biased, the P-type substrate is connected to the most negative voltage available on the device (GND), and the N-type well structure is connected to the most positive voltage on the device (V_{CC}).

Figure 1. Parasitic Bipolar Transistors in CMOS Devices

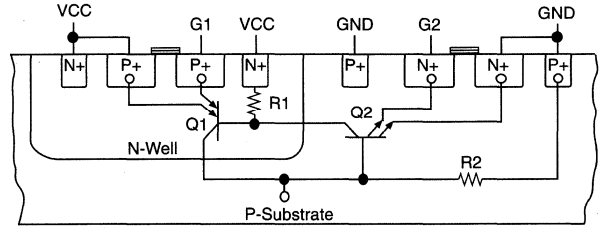


Figure 1 also shows the parasitic resistors (labeled R1 and R2) that occur in the CMOS structure. Generally, these resistors are of no concern as long as currents do not flow through the structure laterally. However, voltage drops across parasitic resistors can occur in the structure if any of the associated diodes are turned on. The diodes can be turned on initially by power-supply or I/O pin transients that exceed the limits of GND and V_{CC}. These I/O pin transients can be induced by signal ringing and other inductive effects in the system.

Catastrophic failure can occur if these parasitic structures begin to conduct, because the effect is regenerative and reinforces itself until potentially destructive currents are produced. This silicon-controlled rectifier (SCR) effect is called the "latch-up " effect. As the current flows through the parasitic transistor, the voltage drop through the resistor increases, further forward-biasing the base-emitter junction. The cycle continues until the current is limited by drops in the primary current path. At this point, the current may have reached a level that permanently damages internal circuitry.

Altera devices have been designed to minimize the effects of latch-up that is caused by power-supply and I/O pin transients. Under recommended operating conditions, all devices can withstand input voltage extremes between GND – 1 V and V_{CC} + 1 V, as well as input currents of 100 mA or less that are forced through the device pins.

To minimize the chances of inducing latch-up during power-up, GND should be applied to the device first, then V_{CC}, and finally the inputs. The power should be removed from the device in the reverse order: the inputs are removed first, then V_{CC}, and finally GND.

Simultaneous application of inputs and V_{CC} to the device, which can occur as a power supply rises during power-up, should be safe as long as V_{CC} meets the maximum rise time. The designer should ensure that the inputs cannot rise faster than the supply at the VCC pin(s).

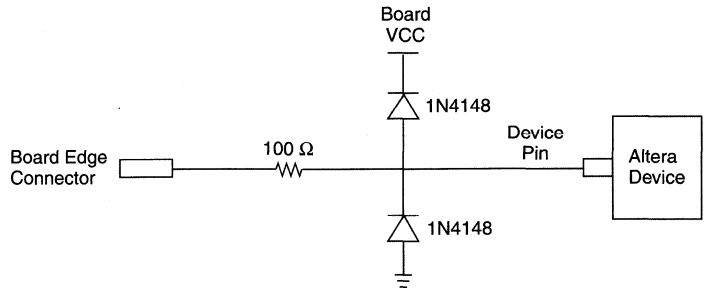
Hot-Socketing

Latch-up frequently occurs when electrical subsystems are "hot-socketed" or plugged into active hardware. When a subsystem is hot-socketed, the logic levels often appear at the subsystem's logic devices before the power supply can provide current to the V_{CC} and GND grid of the subsystem board. This condition can lead to latch-up.

Increasing the length of the V_{CC} and GND connections can reduce the chances of latch-up during hot-socketing. If metal "fingers" are used for the board connection, the V_{CC} and GND fingers at the card edge should be longer than the logic connections. The difference in length would cause the power supply to appear at the device before the logic levels, which is usually sufficient to prevent latch-up. Off-the-shelf connectors with longer V_{CC} and GND connections can provide similar results.

Implementing the circuitry shown in Figure 2 also provides protection against latch-up during hot-socketing. The diode structure provides a "clamp" level on the input voltage, preventing it from swinging more than one diode-drop away from a power rail (–0.6 V to V_{CC} + 0.6 V). The series resistor also reduces the possibility of latch-up by restricting the current to the device input and clamp diodes. This circuitry provides the maximum protection against latch-up, but is usually required only if the input on the device is tied directly to the edge connector. Device inputs that are driven by other circuit elements in the subsystem are generally safe from latch-up, because these elements provide a natural delay before the logic levels are established.

Figure 2. Hot-Socket Protection



Electrostatic Discharge

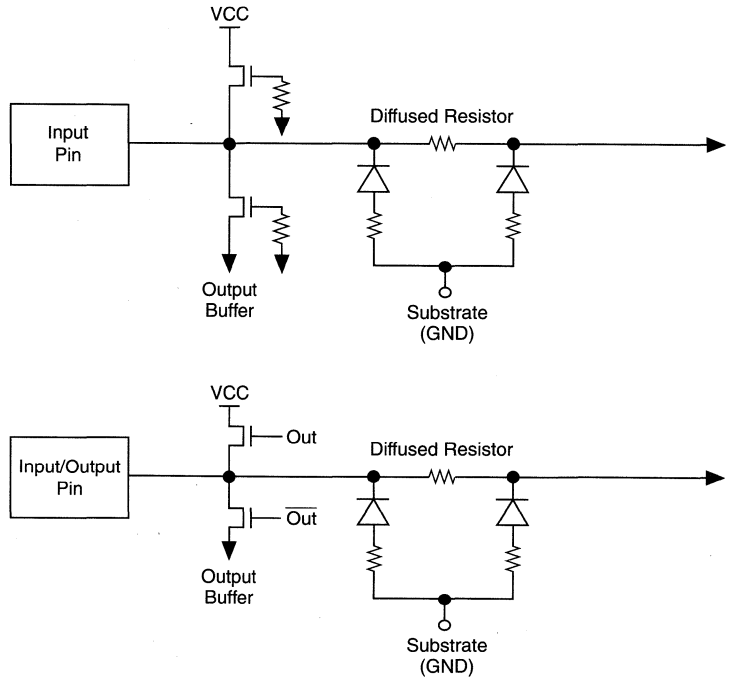
Electrostatic discharge (ESD) resulting from improper device handling can cause device failure that may manifest itself in the following ways:

- Immediate functional failure
- Degraded I/O performance
- Decreased long-term reliability

Handling devices during the programming cycle increases exposure to potential static-induced failure. Synthetic materials used in clothing can store large amounts of static electricity, which can cause ESD. During normal activity, the human body can generate voltages of up to tens of kilovolts (kV). Therefore, to reduce the likelihood of ESD damage, users should wear ground straps when handling devices and ground all surfaces that contact devices.

Altera devices include special structures that reduce the effects of ESD on the pins. Figure 3 shows a typical input structure for an Altera device. Diode structures and an output buffer shunt harmful voltages to ground before the circuitry could be damaged. Most Altera devices can withstand ESD voltages greater than 2 kV, but all devices can withstand ESD voltages up to 1 kV. ESD performance data is reported in Altera's reliability reports.

Figure 3. Altera Device Input Protection Structures



Output Loading

Output loading is typically resistive and/or capacitive. During development, the designer should ensure that the target device can supply both the current and speed necessary for the loads.

Resistive Loading

Resistive loading exists whenever a device output sinks or sources a current in a steady state (e.g., devices with TTL inputs, terminated buses, and discrete bipolar transistors).

Output drive characteristics (I_{OH} and I_{OL}), which are functions of output voltages (V_{OH} and V_{OL}), are listed in each device family data sheet. In DC condition, the output current capabilities determine the maximum resistivity of a load while still maintaining the necessary output voltage. If the system requires higher currents, such as those necessary to drive an LED or a relay, a high-current buffer or a discrete current switch must be used.

Short-circuit conditions—where I_{OH} and I_{OL} exceed the absolute maximum rating (I_{OUT})—can permanently damage the device.

Capacitive Loading

The "AC Operating Conditions" table in each device family data sheet specifies an output capacitance condition (C1) for parameters relating to external performance. For most Altera devices, C1 is 35 pF for active signals and 5 pF for disabling output buffers.

Device packages and board-level trace capacitance contribute the majority of loading capacitance. The specified 35-pF load condition is a representative value for most CMOS circuits. For applications in which a device drives a higher capacitance, performance decreases as the capacitive load increases.

Device sockets are a source of both capacitive and inductive loading. Once a system is finalized for production, sockets should be removed if possible, and the devices should be mounted directly onto the PCB. Direct board mounting reduces both the capacitive load and noise from socket contacts.

To ensure the highest circuit performance, the capacitance on device outputs should be minimized. Because wiring traces on the PCB, device input pins, and device packaging all contribute to the total capacitance, the following guidelines should be observed:

- Board layout should ensure that signals run perpendicular to each other to provide a minimum capacitive coupling effect. Also, signal traces should be kept as short as possible.
- A high-current buffer should be used to speed the signal to all destinations for networks in which a single source drives many loads.

The lack of V_{CC} and GND planes or excessive trace lengths can cause problems with radiated coupling of noise into logic signals and transmission-line effects on signal quality. These ringing and noise elements on logic levels can lead to circuit reliability problems. When recommended layout practices cannot be implemented to prevent transmission-line problems, a small series resistance (10 Ω to 30 Ω) can be used to reduce the undershoot or overshoot magnitude on signal edges. This resistance dampens the ringing that can occur on long board traces and prevents false triggering.

Power-Supply Management

Although Altera devices are designed to minimize noise generation and susceptibility, they can be sensitive to fluctuations in power supply and input lines, like all CMOS devices.

To minimize the effect of these fluctuations, the system designer must pay special attention to:

- V_{CC} and GND planes
- Decoupling capacitors
- V_{CC} rise time
- Current dissipation

V_{CC} & GND Planes

The system designer can minimize power-supply noise or "ground bounce" by providing separate V_{CC} and GND planes for every PCB, thus ensuring a large current-sink capability, noise protection, and shielding for logic signals on the board. If an entire plane cannot be provided, the widest possible GND and V_{CC} traces should be created throughout the entire board. Logic-width traces should not be used to carry the power supply. Although V_{CC} and GND planes tend to increase the capacitive load of the traces, they significantly reduce system noise and dramatically increase system reliability.

Decoupling Capacitors

Each VCC and GND pin should be connected directly to the V_{CC} and GND planes in the PCB. Each pair of VCC and GND pins should be decoupled with a 0.2-µF power-supply decoupling capacitor, located as close as possible to the Altera device. For devices with a very large number of VCC and GND pins—i.e., more than 8 pairs of each—it is not necessary to provide a decoupling capacitor for every pair. In general, 8 decoupling capacitors are sufficient for most designs.

Decoupling requirements are based on the amount of logic used in the device, the frequency of operation, and the output switching requirements. As the number of I/O pins and the switching frequency increase, more decoupling capacitance is required. The ideal solution is to provide a capacitor for every VCC/GND pair, which will decouple the device for any logic utilization or operating frequency. For less dense or slower designs, a reduction in the number of capacitors may be acceptable. For example, the EPM7192E has 14 VCC/GND pairs. Decoupling capacitors should have a good frequency response, like that of monolithic-ceramic capacitors. Table 1 summarizes the recommended number of decoupling capacitors.

Table 1. Recommended Number of Decoupling Capacitors

Number of Ground Pins	Number of Decoupling Capacitors
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8 or more	8

Each PCB should also have a large-capacity, general-purpose, electrolytic capacitor network to stabilize the power supply. A 100-µF capacitor should be placed immediately adjacent to the location where the power-supply lines come into the PCB. If a transformer or regulator is used to change the voltage level, the capacitor should be placed immediately after the final stage that develops the device's V_{CC} supply. This capacitor provides a beneficial leveling effect that supplies extra current when a large number of nodes switch simultaneously in a circuit. However, the larger the power supply capacitor, the longer the time required to bring the maximum V_{CC} to the operating level. The size of the capacitor must not force the V_{CC} rise time to violate the maximum rise time.

V_{CC} Rise Time

When power is applied to an Altera device, the device initiates a Power-On Reset (POR) event, typically as V_{CC} approaches 1.5 V to 2.0 V. The POR event occurs only if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). Slower rise times can cause incorrect device initialization and functional failure. The maximum V_{CC} rise times for Altera devices are provided in the "Recommended Operating Conditions" section of each device family data sheet.

The POR time is the time required after V_{CC} reaches the recommended operating range to clear device registers, configure I/O pins, and release tri-states. Once this initialization is complete, the device is ready to begin logic operation. The POR time does not exceed 50 ms.

Current Dissipation

Each Altera device is designed to consume a minimal amount of power while providing high performance. Since these two design goals can conflict with each other, Altera devices and software tools allow designers to monitor and control the current with built-in device features.

Each MAX 9000 and MAX 7000 macrocell can be configured for either high performance or low power consumption during design entry. Turning on the macrocell's Turbo Bit allows the macrocell to function in a high-performance mode at the specified device ratings. If the Turbo Bit is turned off, the macrocell's built-in power-saving mode trades higher performance for lower current consumption.

MAX 9000 and MAX 7000 devices operating in low-power mode consume less current. The supply current (I_{CC}) can be reduced by approximately 50%, depending on the design and operating frequency. I_{CC} vs. frequency graphs are provided in the *MAX 9000 Programmable Logic Device Family* and the *MAX 7000 Programmable Logic Device Family* data sheets. For a device with the Turbo Bit option, the graph provides two curves: one showing I_{CC} versus frequency when all macrocells have their Turbo Bits turned on and the other with all Turbo Bits off. Because most designs use a combination of turbo and non-turbo macrocells, a formula that accounts for this ratio and the frequency of operation is also provided with the graph. The values shown in the graph and formula are measured with no output loads and represent only the current consumed by device operation.

Many Classic devices also have a Turbo Bit option. A Classic device operating in low-power mode enters a standby mode after 100 ns of inactivity (i.e., when no inputs or outputs have changed). An input signal transition "wakes" the device, which then performs normally until the next standby mode period. However, the input signal incurs an additional delay—specified as the non-turbo delay adder in device family data sheets—as it wakes and propagates through the device.

Device Programming/ Erasure

MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices use non-volatile, reprogrammable EPROM, EEPROM, or FLASH memory elements to retain configuration data. Therefore, configuration data does not need to be reloaded when the system powers up. EPROM, EEPROM, and FLASH memory elements share similar programming characteristics, but different erasure mechanisms.

Altera's EPROM-based devices are available in both plastic and ceramic packages. EPROM devices in plastic packages are one-time-programmable (OTP) devices; windowed ceramic packages allow erasure by exposure to UV light. Altera EPROM-based devices begin to erase when exposed to lights with wavelengths shorter than 4,000 Å. Because fluorescent lighting and sunlight fall into this range, an opaque label must be placed over the device window to ensure long-term reliability. To completely erase a device, it must be exposed to UV light with a wavelength of 2,540 Å. Devices should be erased for one hour by an eraser system with a power rating of 12,000 $\mu W/cm^2$. Altera devices can be damaged by long-term exposure to high-intensity UV light.

Altera EPROM-based devices can be programmed and erased at least 25 times, provided that the recommended erasure exposure levels are followed. However, most devices can be reliably erased and reprogrammed many more times beyond this specified minimum.

All Altera EEPROM- and FLASH-based devices are reprogrammable. EEPROM and FLASH memory elements are electrically erasable and therefore do not have an erasure window. EEPROM- and FLASH-based devices are automatically erased immediately before being programmed, and can be erased and reprogrammed at least 100 times. Most devices can be reliably erased and reprogrammed many more times beyond this specified minimum.

Evaluating Power for Altera Devices

June 1996, ver. 1 Application Note 74

Introduction

A critical element of system reliability is the capacity of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature. This application note discusses how to evaluate and manage power, and provides sample worksheets for performing a power evaluation.

Power Evaluation

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Consumption

Use the following formula to estimate the power consumption (P_{EST}) of the application:

$$P_{EST} = P_{INT} + P_{IO}$$

where $P_{INT} = I_{CCINT} \times V_{CC}$

$P_{IO} = P_{ACOUT} + P_{DCOUT}$

The no-load power (P_{INT}) value can be obtained from the "Power Consumption" section in each device family data sheet. Because this value is "unloaded," it is necessary to add the power dissipated by the I/O buffers—P_{DCOUT} from steady-state outputs and the P_{ACOUT} current from frequently switching outputs. P_{DCOUT} depends on the number of steady-state outputs, the logic levels they drive, and the resistive load on each output, as shown in the following formula:

$$P_{DC_{OUT}} = \sum_{n=1}^{d} P_{DCn}$$

In this formula, d is the number of DC outputs and P_{DCn} is the DC output power of output n.

Table 1 shows the DC power dissipated by the output drivers of the device for typical types of loads. Note that the DC power dissipated by the output driver does not equal the $V_{CC} \times I_{CCIO}$ value because most of the DC power is consumed by the load.

Table 1. DC Power Dissipated

Description	P_{DCn}
1K pull-up resistor for low outputs	0.49 mW
1K pull-down resistor for high outputs	5.04 mW
Bipolar for low outputs	0.16 mW
Bipolar for high outputs	0.0576 mW
CMOS	Negligible

P_{ACOUT} depends on the capacitive load on each output and the frequency at which each output switches, as shown in the following formula:

$$P_{AC_{OUT}} = \sum_{n=1}^{a} C_n V_n f_n \times V_{CC}$$

In this formula, a is the number of AC outputs, C_n is the capacitive load on output n, V_n is the voltage swing of output n, and f_n is the switching frequency of output n.

The following equation shows the frequency of each output (f_n), in terms of the maximum clock frequency ($\mathbf{f_{MAX}}$), the design, and the percentage of outputs toggling ($\mathbf{tog_{IO}}$) at each clock.

$$f_n = (0.5) \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}}$$

Inserting this into the equation and resolving the summation in terms of an average capacitive load yields:

$$P_{ACOUT} = (0.5) \times OUT \times C_{AVE} \times V_O \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times V_{CC}$$

For applications with $V_{CCIO} = 5$ V, $V_O = 3.8$ V.

This gives the following equation for capacitive load:

$$P_{ACOUT} = (0.5) \times OUT \times C_{AVE} \times 3.8\ V \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times 5.0\ V$$

Calculating Maximum Power for the Device & Package

The following formulas are used to calculate the maximum allowed power (P_{MAX}) for a device:

$$P_{MAX} = \frac{T_J - T_A}{\theta_{JA}} \quad \text{or} \quad P_{MAX} = \frac{T_J - T_C}{\theta_{JC}}$$

The maximum allowed power is dependent on the maximum allowed junction temperature of the silicon, the ambient temperature of operation (T_A), and the package's thermal resistance (θ) when configured in the system. The maximum junction temperature is specified in Altera device family data sheets. The ambient temperature depends on the application. The worst-case P_{MAX} value is estimated using the formula with θ_{JA}, the junction-to-ambient thermal resistance. The θ_{JA} value for Altera devices is provided for still air (with convection cooling only), and forced-air flow or 100 feet/second, 200 feet/second, and 400 feet/second. If heat-sinking is used to dissipate heat, the designer should use the case temperature (T_C) and the junction-to-case thermal resistance (θ_{JC}) to calculate P_{MAX} for a device. θ_{JC} is a measure of the lowest possible thermal resistance.

For thermal resistance values (θ_{JC} and θ_{JA}) for Altera devices, refer to the *Altera Device Packaging Information Data Sheet* in this data book.

Comparing Maximum Allowed Power & Estimated Power

To avoid reliability problems, the system designer should compare the values calculated for the maximum allowed power and estimated power. The estimated power should be the smaller of the two values. If the estimated power exceeds the maximum allowed power, refer to "Thermal Management" on page 433 for suggestions on how to reduce power requirements for a design.

Figure 1 shows a sample worksheet for evaluating power.

Figure 1. Power Evaluation Worksheet (Part 1 of 2)

Design:_____ Device:_____

Estimating the Power Consumption of the Application

Internal Power Calculation

FLEX 10K & FLEX 8000 Devices

Standby current ($I_{CCSTANDBY}$) $I_{CCSTANDBY}$ = _____mA

Coefficient for I_{CC} calculation. See the appropriate device family data sheet for this value. K = _____uA/MHz × LE

Highest clock frequency of the device ($\mathbf{f_{MAX}}$) $\mathbf{f_{MAX}}$ = _____MHz

Logic elements used (N) N = _____

Average ratio of logic cells toggling ($\mathbf{tog_{LC}}$) at each clock (typically 0.125) $\mathbf{tog_{LC}}$ = _____

Total internal current (I_{CCINT}) I_{CCINT} = _____mA

$I_{CCINT} = I_{CCSTANDBY} + K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}}$

Total internal power (P_{INT}) P_{INT} = _____ mW

$P_{INT} = V_{CC} \times I_{CCINT}$

MAX 9000 & MAX 7000 Devices

Coefficients for I_{CC} calculation. See the appropriate device family data sheet for these values. A = _____

B = _____

C = _____

Macrocells with turbo bit on (MC_{TON}) MC_{TON} = _____

Number of macrocells in the device (MC_{DEV}) MC_{DEV} = _____

Number of macrocells in the design (MC_{USED}) MC_{USED} = _____

Highest clock frequency of the device ($\mathbf{f_{MAX}}$) $\mathbf{f_{MAX}}$ = _____MHz

Average ratio of logic cells toggling ($\mathbf{tog_{LC}}$) at each clock (typically 0.125) $\mathbf{tog_{LC}}$ = _____

Total internal current (I_{CCINT}) I_{CCINT} = _____mA

$I_{CCINT} = (A \times MC_{TON}) + (B \times MC_{TOFF}) + (C \times MC \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$

Total internal power (P_{INT}) P_{INT} = _____mW

$P_{INT} = V_{CC} \times I_{CCINT}$

Figure 1: Power Evaluation Worksheet (Part 2 of 2)

External Power Calculation

Power consumed by the DC output load (P_{DCOUT}) — P_{DCOUT} = _____ mW

$$P_{DCOUT} = \sum_{n=1}^{OUT} P_{DC_n}$$

Average capacitive load (C_{AVE}) at output pins — C_{AVE} = _____ mW

Number of output/bidirectional pins in design (OUT) — OUT = _____

Average ratio of I/O pins toggling ($\mathbf{tog_{IO}}$) at each clock (typically 0.125) — $\mathbf{tog_{IO}}$ = _____

Power consumed by AC output load (P_{ACOUT}) — P_{ACOUT} = _____ mA

$$P_{ACOUT} = 1/2 \times OUT \times C_{AVE} \times 3.8V \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times 5V$$

Total external power (P_{IO}) — P_{IO} = _____ mW

$$P_{IO} = P_{DCOUT} + P_{ACOUT}$$

Total Power Calculation

Estimated total power (P_{EST}) — P_{EST} = _____ mW

$$P_{EST} = P_{INT} + P_{IO}$$

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device — θ_{JA} = _____ C/W

Maximum junction temperature (T_J) as specified in the appropriate device family data sheet — T_J = _____ ° C

Ambient temperature (T_A) of the design — T_A = _____ ° C

Maximum power (P_{MAX}) allowed for the device — P_{MAX} = _____ W

$$P_{MAX} = \frac{T_J - T_A}{\theta_{JA}}$$

Comparing Maximum Power Allowed & Estimated Power

Is $P_{EST} < P_{MAX}$? — Yes or No

Sample power evaluations for FLEX 10K and MAX 9000 devices are provided in Figures 2 and 3, respectively.

Figure 2. Sample Power Evaluation for a FLEX 10K Device (Part 1 of 2)

Design: atm_pkt.tdf Device: EPF10K50GC403-4

Estimating the Power Consumption of the Application

Internal Power Calculation

FLEX 10K & FLEX 8000 Devices

Standby current ($I_{CCSTANDBY}$) — $I_{CCSTANDBY}$ = 0.500 mA

Coefficient for I_{CC} calculation. See the appropriate device family data sheet for this value. — K = 90 uA/MHz × LE

Highest clock frequency of the device (f_{MAX}) — f_{MAX} = 20 MHz

Logic elements used (N) — N = 2747

Average ratio of logic cells toggling (tog_{LC}) at each clock (typically 0.125) — tog_{LC} = 0.125

Total internal current (I_{CCINT}) — I_{CCINT} = 557 mA

$I_{CCINT} = I_{CCSTANDBY} + K \times f_{MAX} \times N \times tog_{LC}$

Total internal power (P_{INT}) — P_{INT} = _____ mW

$P_{INT} = V_{CC} \times I_{CCINT}$

MAX 9000 & MAX 7000 Devices

Coefficients for I_{CC} calculation. See the appropriate device family data sheet for these values. — A = _____ B = _____ C = _____

Macrocells with turbo bit on (MC_{TON}) — MC_{TON} = _____

Number of macrocells in the device (MC_{DEV}) — MC_{DEV} = _____

Number of macrocells in the design (MC_{USED}) — MC_{USED} = _____

Highest clock frequency of the device (f_{MAX}) — f_{MAX} = _____ MHz

Average ratio of logic cells toggling (tog_{LC}) at each clock (typically 0.125) — tog_{LC} = _____

Total internal current (I_{CCINT}) — I_{CCINT} = _____ mA

$I_{CCINT} = (A \times MC_{TON}) + (B \times MC_{TOFF}) + (C \times MC \times f_{MAX} \times tog_{LC})$

Total internal power (P_{INT}) — P_{INT} = _____ mW

$P_{INT} = V_{CC} \times I_{CCINT}$

Figure 2: Sample Power Evaluation for a FLEX 10K Device (Part 2 of 2)

External Power Calculation

Power consumed by the DC output load ($P_{DC_{OUT}}$) — $P_{DC_{OUT}}$ = 35 mW

$$P_{DC_{OUT}} = \sum_{n=1}^{OUT} P_{DC_n}$$

Average capacitive load (C_{AVE}) at output pins — C_{AVE} = 0 mW

Number of output/bidirectional pins in design (OUT) — OUT = 302

Average ratio of I/O pins toggling ($\mathbf{tog_{IO}}$) at each clock (typically 0.125) — $\mathbf{tog_{IO}}$ = 0.125

Power consumed by AC output load ($P_{AC_{OUT}}$) — $P_{AC_{OUT}}$ = _____ mA

$$P_{AC_{OUT}} = 1/2 \times OUT \times C_{AVE} \times 3.8V \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times 5V$$

Total external power (P_{IO}) — P_{IO} = 66 mW

$$P_{IO} = P_{DC_{OUT}} + P_{AC_{OUT}}$$

Total Power Calculation

Estimated total power (P_{EST}) — P_{EST} = 3115 mW

$$P_{EST} = P_{INT} + P_{IO}$$

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device — θ_{JA} = 11.6 C/W

Maximum junction temperature (T_J) as specified in the appropriate device family data sheet — T_J = 80 ° C

Ambient temperature (T_A) of the design — T_A = 40 ° C

Maximum power (P_{MAX}) allowed for the device — P_{MAX} = 3.448 W

$$P_{MAX} = \frac{T_J - T_A}{\theta_{JA}}$$

Comparing Maximum Power Allowed & Estimated Power

Is $P_{EST} < P_{MAX}$? — (Yes) or No

Figure 3. Sample Power Evaluation for a MAX 9000 Device (Part 1 of 2)

Design:_____ Device: EPM9560RC304-15

Estimating the Power Consumption of the Application

Internal Power Calculation

FLEX 10K & FLEX 8000 Devices

Standby current ($I_{CCSTANDBY}$) $I_{CCSTANDBY}$ = _____ mA

Coefficient for I_{CC} calculation. See the appropriate device family data sheet for this value. K = _____ uA/MHz × LE

Highest clock frequency of the device ($\mathbf{f_{MAX}}$) $\mathbf{f_{MAX}}$ = _____ MHz

Logic elements used (N) N = _____

Average ratio of logic cells toggling ($\mathbf{tog_{LC}}$) at each clock (typically 0.125) $\mathbf{tog_{LC}}$ = _____

Total internal current (I_{CCINT}) I_{CCINT} = _____ mA

$I_{CCINT} = I_{CCSTANDBY} + K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}}$

Total internal power (P_{INT}) P_{INT} = _____ mW

$P_{INT} = V_{CC} \times I_{CCINT}$

MAX 9000 & MAX 7000 Devices

Coefficients for I_{CC} calculation. See the appropriate device family data sheet for these values. A = 0.80

B = 0.27

C = 0.052

Macrocells with turbo bit on (MC_{TON}) MC_{TON} = 421

Number of macrocells in the device (MC_{DEV}) MC_{DEV} = 139

Number of macrocells in the design (MC_{USED}) MC_{USED} = 560

Highest clock frequency of the device ($\mathbf{f_{MAX}}$) $\mathbf{f_{MAX}}$ = 40 MHz

Average ratio of logic cells toggling ($\mathbf{tog_{LC}}$) at each clock (typically 0.125) $\mathbf{tog_{LC}}$ = 0.125

Total internal current (I_{CCINT}) I_{CCINT} = 520 mA

$I_{CCINT} = (A \times MC_{TON}) + (B \times MC_{TOFF}) + (C \times MC \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$

Total internal power (P_{INT}) P_{INT} = _____ mW

$P_{INT} = V_{CC} \times I_{CCINT}$

Figure 3: Sample Power Evaluation for a MAX 9000 Device (Part 2 of 2)

External Power Calculation

Power consumed by the DC output load ($P_{DC_{OUT}}$) — $P_{DC_{OUT}}$ = 50 mW

$$P_{DC_{OUT}} = \sum_{n=1}^{OUT} P_{DC_n}$$

Average capacitive load (C_{AVE}) at output pins — C_{AVE} = 0 mW

Number of output/bidirectional pins in design (OUT) — OUT = 211

Average ratio of I/O pins toggling ($\mathbf{tog_{IO}}$) at each clock (typically 0.125) — $\mathbf{tog_{IO}}$ = 0.125

Power consumed by AC output load ($P_{AC_{OUT}}$) — $P_{AC_{OUT}}$ = ____ mA

$$P_{AC_{OUT}} = 1/2 \times OUT \times C_{AVE} \times 3.8V \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times 5V$$

Total external power (P_{IO}) — P_{IO} = 66 mW

$$P_{IO} = P_{DC_{OUT}} + P_{AC_{OUT}}$$

Total Power Calculation

Estimated total power (P_{EST}) — P_{EST} = 3260 mW

$$P_{EST} = P_{INT} + P_{IO}$$

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device — θ_{JA} = 20 C/W

Maximum junction temperature (T_J) as specified in the appropriate device family data sheet — T_J = 11 ° C

Ambient temperature (T_A) of the design — T_A = 40 ° C

Maximum power (P_{MAX}) allowed for the device — P_{MAX} = 3.500 W

$$P_{MAX} = \frac{T_J - T_A}{\theta_{JA}}$$

Comparing Maximum Power Allowed & Estimated Power

Is $P_{EST} < P_{MAX}$? — (Yes) or No

Thermal Management

The following guidelines reduce power dissipation and heat build-up for an application:

- *Use available low-power features of the device.* By turning the Turbo Bit off, Classic devices and individual macrocells in MAX 9000 and MAX 7000 devices can be configured for low-power operation, with only a nominal increase in propagation delay. All macrocells in the

MAX 9000 or MAX 7000 device that do not need to run in high-performance mode should be set to low-power mode.

- *Choose a different device package.* A ceramic or higher-pin-count package can be used. Ceramic packages dissipate more heat than plastic packages. Also, packages with higher pin counts can dissipate more heat through the connection to the PCB.

- *Use forced-air cooling and/or heat-sinking.* Forced-air cooling improves the efficiency of convection cooling, which reduces the surface temperature of the device. A heat sink connected to a device significantly increases heat dissipation by radiating heat via the metal mass.

- *Slow the operation in portions of the circuit.* I_{CC} is proportional to the frequency of operation. Slowing parts of a circuit lowers the I_{CC} and hence reduces the power. Altera devices provide global or array clock sources for all registers. Signals that do not require high-speed operation can use a slower array clock that significantly reduces the system power consumption.

- *Reduce the number of outputs.* DC and AC current is required to support all I/O pins on the device. Reducing the number of I/O pins may reduce the current necessary for the device, and thereby reduce the power.

- *Reduce the amount of circuitry in the device.* Power depends on the amount of internal logic that switches at any given time. Reducing the amount of logic in a device reduces the current in the device. The same effect may be achieved by using a larger device, which also provides increased heat dissipation and maintains a single-device solution.

- *Choose a different device family.* The MAX 7000 family provides more power-saving features than the MAX 5000 family. The Classic family provides power-saving features for low-density designs.

- *Modify the design to reduce power.* Identify areas in the design that can be revised to reduce the power requirements. Common solutions include reducing the number of switching nodes and/or required logic, and removing redundant or unnecessary signals. For assistance in locating less obvious changes, contact Altera Applications at (800) 800-EPLD.

Metastability
in Altera Devices

June 1996, ver. 2 Application Note 42

Introduction

The output of an edge-triggered flipflop has two valid states: high and low. To ensure reliable operation, designs must meet the flipflop's timing requirements. The input to the flipflop must be stable for a minimum time before the clock edge (register setup time, or t_{SU}) and a minimum time after the clock edge (register hold time, or t_H). Specific values for t_{SU} and t_H are provided in each device family data sheets in this data book, or they can be determined using the MAX+PLUS II Timing Analyzer.

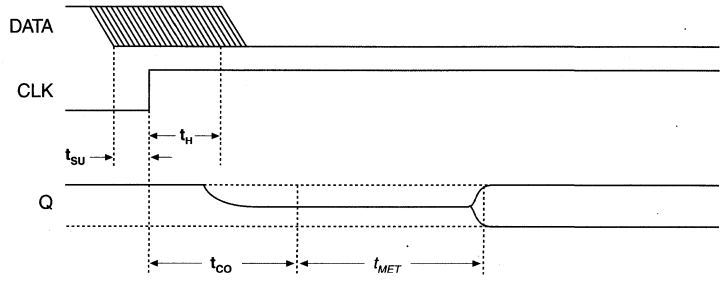
In non-synchronous systems, if the asynchronous input signals violate a flipflop's timing requirements, the output of the flipflop can become metastable. Metastable outputs oscillate or hover between high and low states for a brief period of time, which can cause system failure. Therefore, you must analyze the metastability characteristics of a device to determine the reliability of a non-synchronous design. In synchronous systems, the input signals always meet the flipflop's timing requirements, so metastability does not occur.

This application note describes metastability, how it is quantified, and how to minimize its effect. It also includes metastability data for Altera's FLEX 10K, FLEX 8000A, MAX 9000, and MAX 7000 devices that can be used to estimate a system's mean time between failures (MTBF) when using an Altera device to synchronize asynchronous data.

Metastability

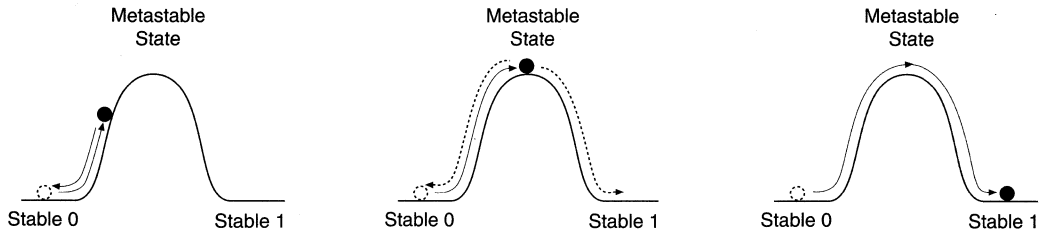
Violating a flipflop's setup or hold times can cause its output to become metastable. When a flipflop is in a metastable ("in between") state, the output hovers at a voltage level between high and low, causing the output transition to be delayed beyond the specified clock-to-output delay (t_{CO}). The additional time beyond t_{CO} that a metastable output takes to resolve to a stable state is called the settling time (t_{MET}). Not every transition that violates the setup or hold times will result in a metastable output. The likelihood that a flipflop will enter a metastable state and the time required to return to a stable state varies depending on the process technology used to manufacture the device and on the ambient conditions. Generally, flipflops quickly return to a stable state. See Figure 1.

Figure 1. Metastability Timing Parameters



The operation of a register is analogous to a ball rolling over a frictionless hill, as shown in Figure 2. Each side of the hill represents a stable (i.e., high or low) state, and the top of the hill represents the metastable state. When the data input of a flipflop complies with minimum setup (t_{SU}) and hold (t_H) times, the output passes from one stable state to another (i.e., from high to low or low to high) without an additional delay. Analogously, the ball will get over the hill within a specified time if given enough of a push.

Figure 2. Effects of Violating t_{SU} & t_H Requirements



Output glitches.

Output temporarily remains at a metastable state and may return to either stable state.

Output passes through a metastable state and incurs an additional delay.

However, when the data input of a flipflop violates the setup or hold times, the flipflop is marginally triggered, and the output may not immediately resolve to either of the two stable states within the specified time. This marginal triggering can cause the output to glitch, to remain temporarily at a metastable state between the high and low logic levels, or to take longer to return to a stable state, any of which increase the delay from the clock transition to a stable output.

Metastability does not necessarily cause unpredictable system performance. If the wait time is sufficient to allow the flipflop to settle to a stable state, then metastability will not affect the system; the output of the flipflop can temporarily have an undefined value, provided that it returns to a known value before the signal is evaluated. Therefore, allowing an additional time (t_{MET}) for the signal to settle to a known state will prevent the propagation of an undefined value to the rest of the system.

Analyzing Metastability

The MTBF value quantitatively shows how metastability affects your design. The MTBF provides an estimate of the mean time between the probable occurrence of two successive metastable events. The MTBF of a synchronizing flipflop can be estimated with the following formula:

$$MTBF = \left[f_{CLOCK} \times f_{DATA} \times C_1 \times e^{(-C_2 \times t_{MET})} \right]^{-1}$$

The t_{MET} parameter is the additional time allowed by the system for the flipflop to settle to a stable state. The constants C_1 and C_2 vary according to the process technology used to manufacture the device. Therefore, different devices manufactured with the same process have similar values for C_1 and C_2.

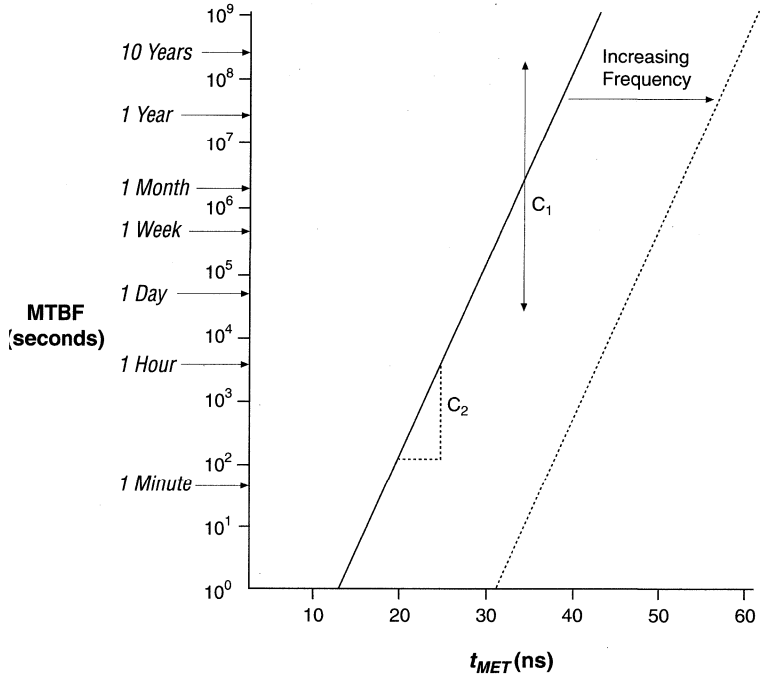
The constants C_1 and C_2 are determined by plotting the natural log of MTBF vs. t_{MET} and performing a linear regression analysis on the data. The slope and the y-intercept of the resulting line determine the values of C_1 and C_2. The formulae for the constants C_1 and C_2 are as follows:

$$C_2 = \frac{\Delta \ln(MTBF)}{\Delta t_{MET}}$$

$$C_1 = \frac{e^{(-C_2 \times t_{MET})}}{MTBF \times f_{CLOCK} \times f_{DATA}}$$

Figure 3 shows the relationship between the MTBF and t_{MET} and shows how changing C_1, C_2, and the system frequency affects this relationship.

Figure 3. MTBF vs. t_{MET}



The constant C_1 scales the MTBF equation linearly, shifting the entire curve up or down. Therefore, the larger the value of C_1, the higher the MTBF. The constant C_2 affects the slope of the MTBF vs. t_{MET} curve; therefore, C_2 determines how quickly the flipflop settles to a stable state. For higher C_2 values, the settling time is lower. Increasing the operating frequency shifts the entire curve to the right, lowering the MTBF value.

Once the values for C_1 and C_2 are determined for a particular device, you can use the MTBF equation shown on page 437 to calculate the MTBF of a system with a given settling time (t_{MET}). The t_{MET} delay is the additional time required for the flipflop to resolve to a legal state. Thus, it is the difference between the minimum system clock period and the actual clock period. You can also use the metastability equation to determine the t_{MET} delay required for a given MTBF value, as shown below:

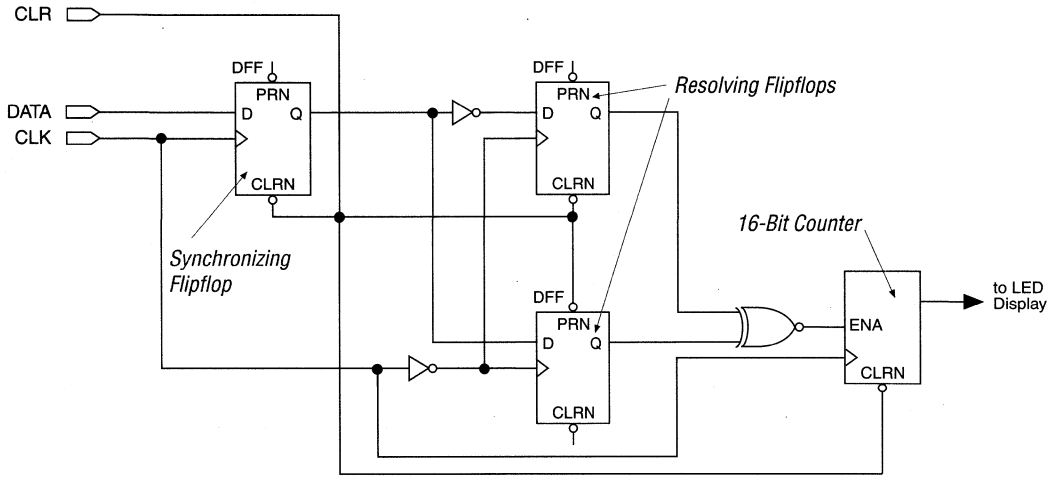
$$t_{MET} = \frac{\ln(\text{MTBF} \times f_{CLOCK} \times f_{DATA} \times C_1)}{C_2}$$

Test Circuitry

Figure 4 shows the test circuit used to determine the metastability characteristics of Altera devices. In this figure, one flipflop has asynchronous clock and data inputs. The logic that generates the metastable event and the logic that detects it are both located in the device under test (DUT). The output of the synchronizing flipflop is fed directly to one of the resolving flipflops and through an inverter to the other resolving flipflop. The outputs of the resolving flipflops feed an XNOR gate that is at a high logic level when the values of the outputs (the signal and its complement) are the same. If the resolving flipflops detect that the signal and its complement have the same logical value, a metastable event has occurred and the counter is incremented.

Figure 4. Metastability Test Circuit

All logic is part of the device under test (DUT).



Because the resolving flipflops are clocked by the falling edge of the clock, the required settling time can be controlled by changing the clock high time (Δt). The settling time t_{MET} can be determined with the equation below. The $\mathbf{t_{ACNT}}$ delay is the minimum clock period, which is equal to the minimum delay from the clock edge to the output of the synchronizing flipflop, plus the delay from the output of the synchronizing flipflop to the input of the resolving flipflops, plus the setup time of the resolving flipflop. The t_{MET} parameter is the minimum time allowed under normal operation of the circuit.

$$t_{MET} = \Delta t - \mathbf{t_{ACNT}}$$

Metastability Characteristics of Altera Devices

Figure 5 shows the metastability characteristics of FLEX 10K, FLEX 8000A, MAX 9000, and MAX 7000 devices. For all devices, f_{DATA} is 1 MHz and f_{CLOCK} is 10 MHz.

Figure 5. Metastability Characteristics of Altera Devices

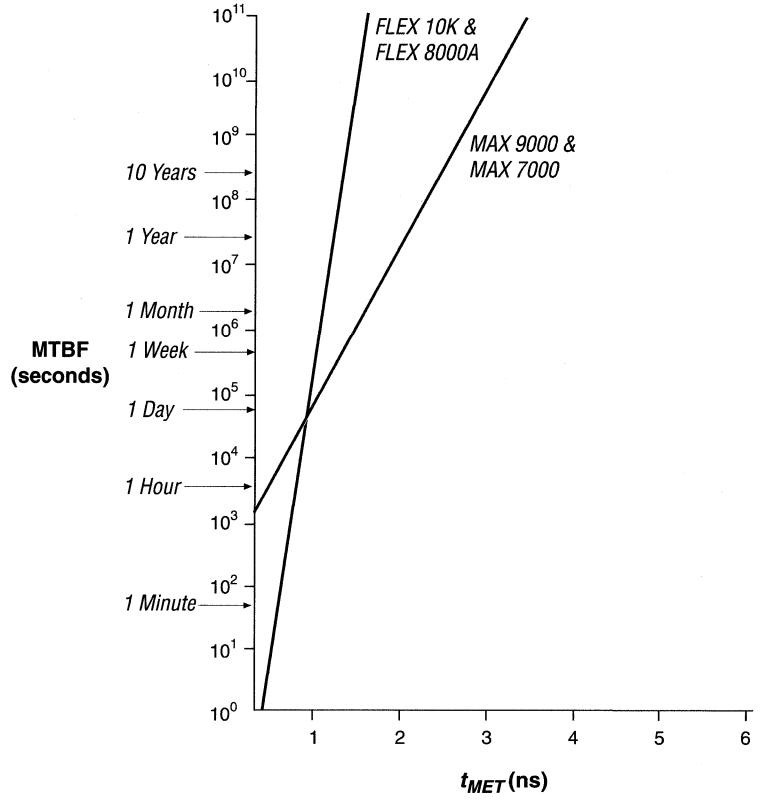


Table 1 summarizes the values of C_1 and C_2 for Altera's FLEX 10K, FLEX 8000A, MAX 9000, and MAX 7000 devices.

Table 1. Metastability Equation Constants Note (1)		
Device	**C_1**	**C_2**
FLEX 10K	1.01×10^{-13}	1.268×10^{10}
FLEX 8000A	1.01×10^{-13}	1.268×10^{10}
MAX 9000	2.98×10^{-17}	5.023×10^{9}
MAX 7000	2.98×10^{-17}	5.023×10^{9}

Note:
(1) Information for FLEX 10K and MAX 9000 devices is preliminary.

Applying the Metastability Equation

You can use the C_1 and C_2 values listed in Table 1 to calculate the MTBF for a specific settling time, or you can calculate the minimum settling time for a specific MTBF. For example, the equation below calculates the t_{MET} needed to ensure a MTBF of 1 year (approximately 3×10^7 seconds) for an EPF8452A with a data frequency of 2 MHz and a clock frequency of 10 MHz.

$$t_{MET} = \frac{\ln(3 \times 10^7) + \ln[(10 \times 10^6)(2 \times 10^6)(1.01 \times 10^{-13})]}{1.268 \times 10^{10}} = 1.41\text{ns}$$

When calculating the delay for the output of the flipflop to the remaining logic for a MTBF of one year, 1.41 ns should be added to the clock-to-output delay (t_{CO}) of the flipflop.

Due to the logarithmic relationship between the MTBF and t_{MET}, small changes in t_{MET} dramatically affect the MTBF. If the MTBF required is increased from one year to 10 years in the example shown above, the t_{MET} delay increases to only 1.59 ns.

Figures 6 and 7 show the t_{MET} delay required for FLEX 10K, FLEX 8000A, MAX 9000, and MAX 7000 devices when f_{DATA} is one half of f_{CLOCK}. Because the MTBF is inversely proportional to the value ($f_{CLOCK} \times f_{DATA}$), these figures can be used to find the MTBF for many designs. Metastability is probabilistic, and MTBF values are mean values calculated for a limited sample of devices and should only be used to estimate t_{MET} delays.

Figure 6. FLEX 10K & FLEX 8000A MTBF Values

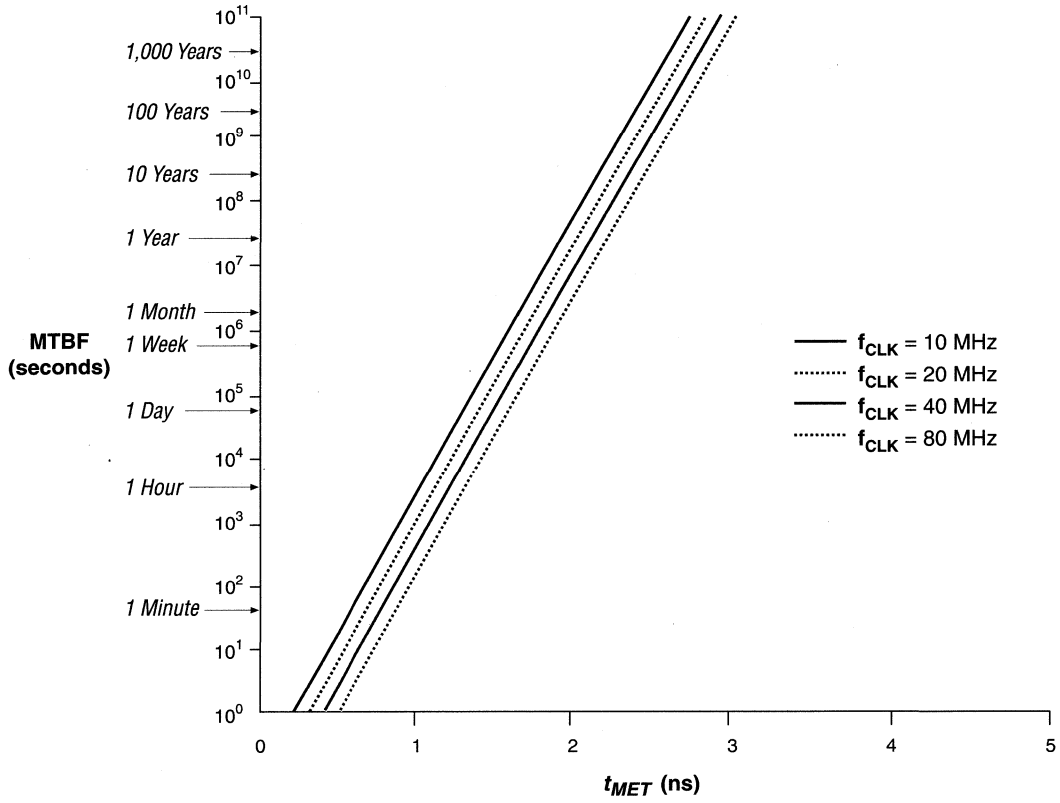
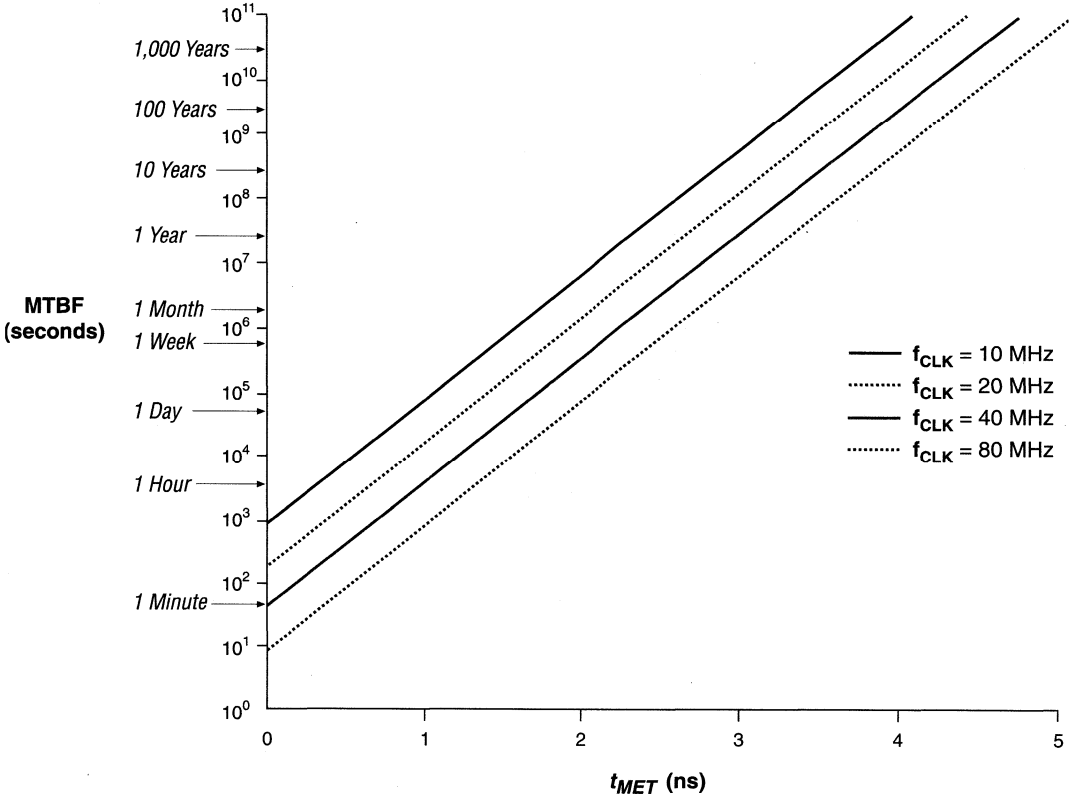


Figure 7. MAX 9000 & MAX 7000 (Including MAX 7000S & MAX 7000E) MTBF Values



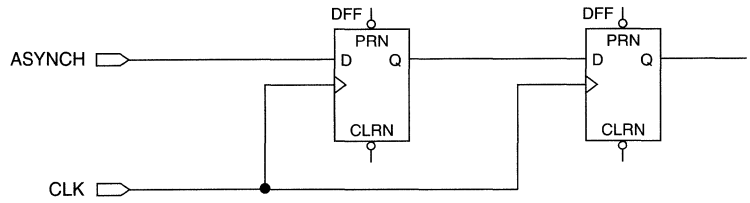
Avoiding Metastability

Several techniques can be used to reduce metastability in a system. If an asynchronous signal is fed to several flipflops, the probability that a metastable event will occur greatly increases because there are more flipflops that could become metastable. In this case, you can avoid metastability by using the output of the synchronizing flipflop throughout the system rather than the asynchronous signal.

You can also avoid the negative effects of metastability by adding the t_{MET} calculated for a specific MTBF to the worst-case timing delay calculations, giving the output of the synchronizing flipflops time to settle. Faster devices provide faster $\mathbf{t_{CO}}$ and $\mathbf{t_{SU}}$ times, which provide additional time for the t_{MET} delay without sacrificing overall system speed.

The most common method of reducing the effects of metastability is to use a multiple-stage synchronizer in which two or more flipflops are cascaded to form a synchronization circuit. See Figure 8. If the synchronizing flipflop produces a metastable output, then the metastable signal may resolve before it is clocked by the second flipflop. This method does not guarantee that the second flipflop will not clock an undefined value, but it dramatically increases the probability that the data will go to a valid state before it reaches the rest of the circuit.

Figure 8. Multiple-Stage Synchronizer



Conclusion

Metastability is a phenomenon only affecting flipflops that are used to synchronize data from asynchronous systems. The metastability characteristics for a particular device depend on the process technology used to manufacture the device and on ambient conditions. Altera devices have very good metastability characteristics; you only need to add a small t_{MET} delay to the $\mathbf{t_{CO}}$ delay to achieve a high MTBF value.

High-Speed Board Designs

June 1996, ver. 1 Application Note 75

Introduction

To create a successful high-speed printed circuit board (PCB), you must integrate the device(s), PCB(s), and other elements into a coherent design. Most Altera devices have user-controllable slew rates, some of which can be as high as 1 to 3 ns. This would contribute to noise generation, signal reflection, cross-talk, and ground bounce. Therefore, your design must:

- Filter and evenly distribute power to all devices to reduce noise
- Terminate signal and transmission lines to diminish signal reflection
- Minimize cross-talk between parallel traces
- Reduce the effects of ground bounce

Power Filtering & Distribution

You can dramatically reduce system noise by providing clean, evenly distributed power supply as close as possible to V_{CC} to all boards and devices.

Filtering Noise

To diminish the low-frequency (< 1 kHz) noise caused by the power supply, you must filter the noise on the power lines at the point where the power connects to the PCB, and where it connects to each device. Altera recommends placing a 100-µF electrolytic capacitor immediately adjacent to the location where the power supply lines enter the PCB. If you use a voltage regulator, place the capacitor immediately after the final stage that provides the V_{CC} signal to the device(s). Capacitors not only filter low-frequency noise from the power supply, but also supply extra current when many outputs switch simultaneously in a circuit.

The components on the PCB add high-frequency noise to the power plane. To filter high-frequency noise at the device, Altera recommends placing 0.02-µF and 0.2-µF decoupling capacitors as close as possible to each V_{CC} and GND pair.

See the *Operating Requirements for Altera Devices Data Sheet* in this data book for more information on bypass capacitors.

Distributing Power

Power distribution also has an impact on system noise. Power can be distributed throughout the PCB with either a power bus network or power planes.

A power bus network consists of two or more wide, metal traces that carry the V_{CC} and GND to the devices. Usually used on two-layer PCBs, power buses provide an inexpensive method of supplying power. The trace widths, which should be as wide as possible, are limited by the density of the PCB. Power buses have significant DC resistance; the last component on the bus may receive V_{CC} power that is degraded by as much as 0.5 V. Consequently, Altera recommends using power buses only for applications that do not require an equal distribution of V_{CC}.

As an alternative, Altera recommends using power planes to distribute power. Power planes are used on multi-layer PCBs and consist of two or more metal layers that carry V_{CC} and GND to the devices. Because the power plane covers the full area of the PCB, its DC resistance is very low. The power plane maintains V_{CC} and distributes it equally to all devices, while also providing near-infinite current-sink capability, noise protection, and shielding for the logic signals on the PCB.

Signal & Transmission Line Termination

Having established the PCB power network, you must consider the layout of the devices and traces. Fast edge rates contribute to noise, cross-talk, and ground bounce to varying degrees, depending on the PCB construction material.

Each PCB substrate has a different relative dielectric constant (E_r) that measures the effect of an insulator on the capacitance of a conductor pair compared to the capacitance of the conductor pair in a vacuum. The type of substrate used determines the length at which the signal traces must be handled as transmission lines. Table 1 lists E_r values for various dielectric materials.

Table 1. Relative Dielectric Constants

Material	E_r
Air	1.0
PTFE/glass	2.2
Rogers RO 2800	2.9
CE/goreply	3.0
BT/goreply	3.3
CE/glass	3.7
Silicon dioxide	3.9
BT/glass	4.0
Polymide/glass	4.1
FR-4/glass	4.1
Glass cloth	6.0
Alumina	9.0

The following equation shows how the relative dielectric constant (E_r) of the material determines the velocity (V_P) at which signals may flow. The constant (C) equals 3×10^8 m/s or 30 cm/ns:

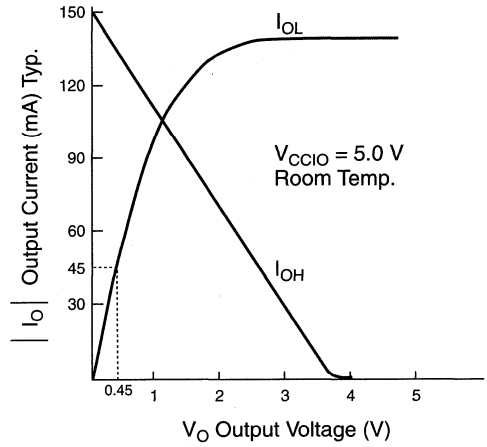
$$V_P = \frac{C}{\sqrt{E_r}}$$

The signal trace must be treated as a transmission line when the two-way propagation delay (PD) of the line exceeds the signal edge rate (t_R). The propagation delay for MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices is the input-to-output delay (t_{PD}). The propagation delay for FLEX 10K and FLEX 8000 devices is either the transfer rate from I/O pin to I/O pin via row, logic element (LE), and column or the transfer rate from I/O pin to I/O pin via row, LE, and row. See the following equation:

$$t_R < 2 \times PD$$

An Altera device's signal edge rate at the rising edge is a function of the capacitance that is driven by the device. You can estimate this signal edge rate if you know the device's capacitive load. Altera device family data sheets include output drive characteristics graphs that show the voltage/current relationship of the output drives. You can derive an equation for signal edge rate at the rising edge as a function of capacitance using these output drive characteristics graphs. Figure 1 shows the output drive characteristics for the MAX 7000 device family.

Figure 1. Output Drive Characteristics of MAX 7000 Devices



The relationship between high-level output current (I_{OH}) and output voltage (V_O) is roughly linear until the voltage approaches 4 V. The equation for the linear approximation is as follows:

$$I_{OH} = 0.15 - \frac{0.15}{3.8} \times V_O = 0.15 - 0.0395 \times V_O$$

Solving the charging capacitor equation for time (t) yields the following equations:

$$\frac{\partial V}{\partial t} = \frac{I_{OH}}{C} \qquad \partial t = \frac{C}{I_{OH}}(\partial V)$$

Substituting the equation above for I_{OH} yields the following equation:

$$\partial t = \frac{C}{0.15 - 0.0395V}(\partial V)$$

Integrating and solving the integral from 0 V to 2.4 V yields the following signal edge rate (t_R) equation for the rising edge:

$$t_R = C\frac{-1}{0.0395} \times \ln(0.15 - 0.0395\ V)\Big|_0^{2.4} = 25.3 \times C$$

You can choose different bounds for the integral if you need to drive a device with an input high voltage (V_{IH}) greater than 2.4 V. For instance, if your Altera device is driving a CMOS input, V_{IH} will increase to 3.84 V, so you can integrate from 0 V to 3.84 V instead of from 0 V to 2.4 V.

To calculate output delay time, you must first determine the rise time of the specified load. At the 35-pF load, the rise time is as follows:

$$t_R = (25.3)(35 \times 10^{-12})\text{sec} = 0.9 \text{ ns}$$

The propagation delay (PD) is the length (l) of the line divided by the velocity (V_P):

$$PD = \frac{l}{V_P}$$

By solving for length (l) using the equation below, you can calculate the length at which the line must be treated as a transmission line:

$$l > \frac{t_R \times k}{2\sqrt{E_r}}$$

As shown in Table 1 on page 447, a PCB with glass cloth substrate has an E_r of 6. Table 2 lists the maximum line lengths for FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, and MAX 5000 devices using a glass cloth substrate under a 35-pF load.

Table 2. Maximum Line Lengths for Glass Cloth Substrate

Device Family	t_R (ns)	l (cm)	l (inches)
FLEX 10K	1.02	6.25	2.46
FLEX 8000	1.1	6.73	2.65
MAX 9000	0.88	5.42	2.14
MAX 7000	0.9	5.51	2.17
MAX 5000	2.7	16.52	6.50

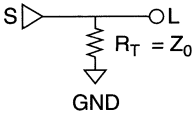
Mismatched impedances cause signals to reflect back and forth, and up and down the line, which in turn causes ringing at the load. To eliminate reflections, the impedance of the source (Z_S) must equal the impedance of the trace (Z_0) and the load (Z_L).

The load impedance is typically much higher than the line impedance, which is higher than the source impedance. On an unmatched transmission line, a signal reflects 100% at the load and approximately 80% at the source, bouncing back and forth until it dies out. To reduce signal reflection, you can match the impedance either at the load (Z_L) or at the source (Z_S) to the line impedance (Z_0). You can match the impedance by adding an impedance in parallel with the load to reduce its input impedance.

Termination Schemes

Parallel termination diminishes the first reflection by matching the load impedance to the line impedance. The following are four parallel termination circuits. Altera recommends using either the Thevenin or resistor and capacitor (series-RC) scheme. For the matching to be effective, you must terminate each load, because any impedance mismatch will result in a signal reflection.

Simple Parallel Termination



In a simple parallel termination scheme, the terminating resistor (R_T) is equal to the line impedance. The placement of the termination resistor must be as close to the load as possible to be efficient. The current loading of this termination is highest at a high-output state. You can estimate the current load (I_L) with the following equation:

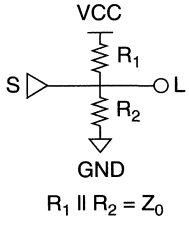
$$I_L = I_{OH} \times \frac{R_{DS}}{R_{TOTAL}}$$

R_{DS} is the pull-up resistance from the I_{OH} curve (refer to Figure 1 on page 448) of the output drive characteristic. R_{TOTAL} is the sum of R_{DS} and R_T. For example, the current load for a 50-Ω parallel termination on a MAX 7000 device at 2.4 V is as follows:

$$I_L = 45\ mA \times \frac{25\Omega}{75\Omega} = 15\ mA$$

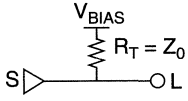
The current load cannot exceed the maximum DC limit per output pin. In this case, the 15-mA current load is less than the maximum DC limit of 25 mA per output pin for MAX 7000 devices.

Thevenin Parallel Termination



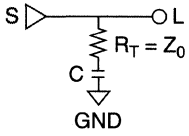
An alternative parallel termination scheme uses a Thevenin voltage divider. The terminating resistor is split between R_1 and R_2, which equal the line impedance when combined. Although this scheme reduces the current draw from the source device, it adds current drawn from the power supply because the resistors are tied between V_{CC} and GND.

Active Parallel Termination



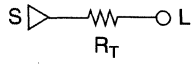
In an active parallel termination scheme, the terminating resistor ($R_T = Z_0$) is tied to a bias voltage (V_{BIAS}). The bias voltage is selected so that the output drivers are capable of drawing current from the high- and low-level signals. However, this scheme requires a separate voltage source that can sink and retain currents to match the output transfer rates.

Series-RC Parallel Termination



In a parallel termination scheme, a resistor and capacitor (series-RC) network is used as the terminating impedance. The terminating resistor (R_T) is equal to Z_0; the capacitor must be greater than 100 pF. The capacitor blocks low-frequency signals while passing high-frequency signals. Therefore, the DC loading effect of R_T does not impact the driver.

Series Termination



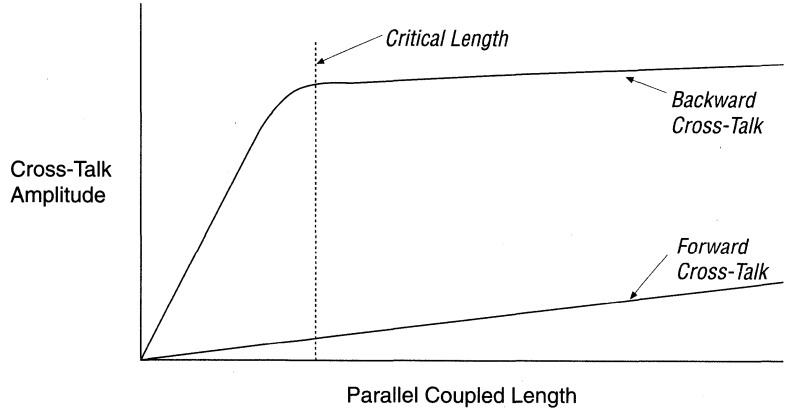
A series termination scheme matches the impedance at the signal source instead of matching the impedance at each load. Because the output impedance of Altera devices is low, you must add a series impedance to match the signal source to the line impedance.

On an unmatched line, the source eventually reduces the reflections; adding the series termination helps attenuate secondary reflections. The source impedance varies from 10 Ω to 25 Ω, and the line impedance varies depending on the distribution of the load. Therefore, you cannot choose a single resistor value that applies to all conditions. Altera recommends using a 33-Ω series resistor to cover most impedances. This method requires only a single component at the source rather than multiple components at each load, but delays the signal path as it increases the RC time constant.

Cross-Talk

Cross-talk is the unwanted coupling of signals between parallel traces. Two types of cross-talk exist: forward (capacitive) and backward (inductive). Figure 2 illustrates the effect of each type of cross-talk as a function of the parallel length.

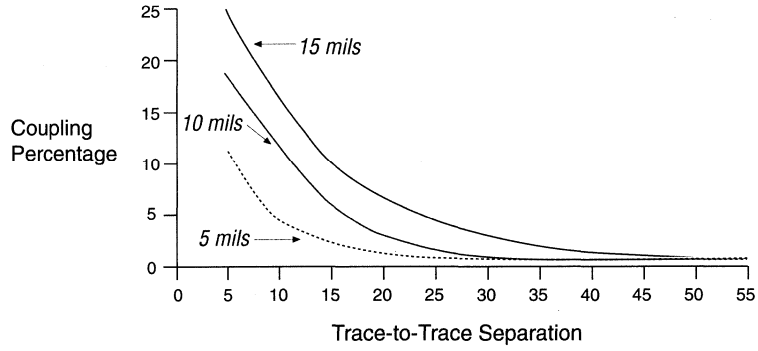
Figure 2. Cross-Talk as a Function of Parallel Length



Backward cross-talk, which has a more dramatic effect than forward cross-talk, occurs when the magnetic field from one trace induces a signal in a neighboring trace. In logic systems, the current flow through a trace is significant when the signals are switching or non-static. The magnetic fields created by switching currents induce the coupling transients.

You can dramatically reduce cross-talk by limiting the trace distance to 10 mils above the GND plane. Figure 3 shows the effect of trace height on trace-to-trace coupling.

Figure 3. Effect of Trace Height on Trace-to-Trace Coupling



Ground Bounce

As digital devices become faster, their output switching times decrease. Faster switching times cause higher transient currents in outputs as they discharge load capacitances. These higher currents, which are generated when multiple outputs of a device switch simultaneously from a logic high to a logic low, can cause a board-level phenomenon known as ground bounce.

Many factors contribute to ground bounce. Therefore, no standard test method allows you to predict its magnitude for all possible PCB environments. You can only test the device under a given set of conditions to determine the relative contributions of each condition and of the device itself. Load capacitance, socket inductance, and the number of switching outputs are the predominant factors that influence the magnitude of ground bounce in programmable logic devices.

Design Recommendations

Altera recommends that you take the following steps to reduce ground bounce:

- Turn on the Slow Slew Rate logic option for FLEX 10K, FLEX 8000, MAX 9000, MAX 7000E, and MAX 7000S designs.
- Limit load capacitance by buffering loads with an external device such as the 74244 IC bus driver or by reducing the number of devices that drive the bus.
- Eliminate sockets whenever possible.
- Reduce the number of outputs that can switch simultaneously and/or distribute them evenly throughout the device.
- Move switching outputs close to a package GND pin.
- Eliminate pull-up resistors, or use pull-down resistors.
- Use multi-layer PCBs that provide separate V_{CC} and GND planes.
- Add 10-Ω to 30-Ω resistors in series to each of the switching outputs to limit the current flow into each of the outputs.

Go to "Slow Slew Rate" using **Search for Help on** (Help menu) in MAX+PLUS II for more information about this logic option.

These design recommendations, many of which are described in detail later in this application note, should help you create effective high-speed logic designs that operate over a wide range of PCB conditions.

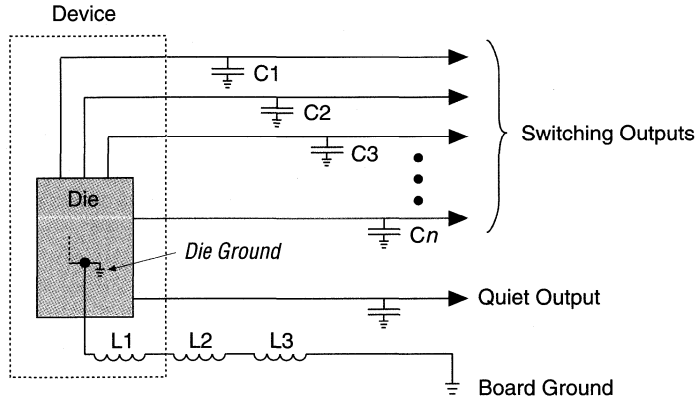
Analyzing Ground Bounce

Figure 4 shows a simple model for analyzing ground bounce. The external components driven by the device appear to that device as capacitive loads (C1 to C*n*). These capacitive loads store a charge that is determined by the following equation:

charge (Q) = [voltage (V) × capacitance (C)]

Thus, the charge increases as the voltage and/or load capacitance increases.

Figure 4. Ground Bounce Model



The environment and ground path of a device have intrinsic inductances (shown in Figure 4 as L1, L2, and L3). L1 is the inductance of the bond wire from the device's die to its package pin, and of the pin itself. L2 is the inductance of the connection mechanism between the device's ground pin and the PCB. This inductance is greatest when the device is connected to the PCB through a socket. L3 is the inductance of the PCB trace between the device and the PCB location where the power supply's reference ground is connected.

Ground bounce occurs when multiple outputs switch from high to low. The transition causes the charge stored in the load capacitances to flow into the device. The sudden rush of current ($\partial i/\partial t$) exits the device through the inductances (L) to board ground, generating a voltage (V) determined by the equation $V = L \times (\partial i/\partial t)$. This voltage difference between board ground and device ground causes the relative ground level for low or quiet outputs to temporarily rise or bounce. Although the rush of current is brief, the magnitude of the bounce can be large enough to trigger other devices on the PCB.

In synchronous designs, ground bounce is less often a problem because synchronous outputs have enough time to settle before the next clock edge. Also, synchronous circuits are not as likely to be falsely triggered by a voltage spike on a quiet output.

Ground bounce is affected differently by capacitive loading on the switching outputs and quiet outputs.

Switching Outputs

When the capacitive loading on the switching outputs increases, the amount of charge available for instantaneous switching increases, which in turn increases the magnitude of ground bounce. Depending on the device, ground bounce increases with capacitive loading until the loading is approximately 100 pF per device output. At this point, the device output buffers reach their maximum current-carrying capacity and inductive factors become dominant.

One method of reducing the capacitive load, and consequently ground bounce, is to connect the device's switching outputs to a bus driver integrated circuit (IC). The outputs of the bus driver IC drive the heavy capacitive loads, reducing the loading on the device, thus minimizing ground bounce for the device's quiet outputs.

Some bus applications use pull-up resistors to create a default high value for the bus. These resistors cause the load capacitances to charge up to the maximum voltage. Consequently, the driving device produces a higher level of ground bounce. Therefore, you should eliminate pull-up resistors in applications in which ground bounce is a concern, or design a bus logic that uses pull-down resistors instead.

The number of switching outputs also affects ground bounce. As the number of switching outputs increases, the total charge stored also increases. The total charge is equal to the sum of the stored charges for each switching output. Therefore, the amount of current that must sink to ground increases as the number of switching outputs increases. Ground bounce can increase by as much as 40 mV to 50 mV for each additional output that is switching.

To counteract these effects, Altera devices provide multiple VCC and GND pin pairs. You can reduce ground bounce by moving switching outputs close to a package GND pin, and by distributing simultaneously switching outputs throughout the device.

Many Altera devices have slew rate options for the output drivers. Turning on the Slow Slew Rate option for all or most of the drivers slows down the drivers, decreasing $\partial i/\partial t$ and reducing ground bounce.

To further reduce ground bounce, limit the number of outputs that can switch simultaneously in your design. For functions such as counters, you can use Gray coding as an alternative to standard sequential binary coding, since only one bit switches at a time.

In extreme cases, adding resistors (10 Ω to 30 Ω is usually adequate) in series to each of the switching outputs in a high-speed logic device can limit the current flow into each of the outputs, and thus reduce ground bounce to an acceptable level.

Quiet Outputs

An increase in capacitive loading on quiet outputs acts as a low-pass filter and tends to dampen ground bounce. Capacitive loading on a quiet output can reduce ground bounce by as much as 200 to 300 mV. However, an increase in capacitive loading on a quiet output can increase the noise seen on other quiet outputs.

Minimizing Lead Inductance

Socket usage and PCB trace length are two elements of L2, the inductance of the connection mechanism between the device's ground pin and the PCB shown in Figure 4 on page 454. Sockets can cause ground bounce voltage to increase by as much as 100%. You can often dramatically reduce the ground bounce on the PCB by eliminating sockets. The length of the PCB trace has a much smaller effect on ground bounce than sockets. For PCBs with a ground plane, the voltage drop across the inductance (L3) of the PCB trace between the device and the PCB location where other devices in the system reference ground is negligible, because L3 is significantly less than L2. The inductance in a 3-inch trace increases ground bounce for a quiet output by approximately 100 mV. Therefore, trace length should be kept to a minimum. As traces become longer, transmission line effects may cause other noise problems.

You can also reduce ground bounce due to PCB trace inductance by using multi-layer PCBs that provide separate V_{CC} and GND planes. Wire-wrapping the V_{CC} and GND supplies usually increases the amount of ground bounce. To reduce unwanted inductance, you should use low-inductance bypass capacitors between the V_{CC} supply pins and the board GND plane, as close to the package supply pins as possible. A standard decoupling capacitor (0.02 µF to 0.2 µF) used in parallel with a high-frequency decoupling capacitor (470 pF is a standard value) gives the best results.

References

Knack, Kella. *Debunking High-Speed PCB Design Myths.* ASIC & EDA, Los Altos: James C. Uhl, July 1993.

Understanding FLEX 8000 Timing

June 1996, ver. 1 Application Note 76

Introduction

Altera devices provide predictable performance that is consistent from simulation to application. Before configuring a device, you can determine the worst-case timing delays for any design. You can calculate propagation delays either with the MAX+PLUS II Timing Analyzer or with the timing models given in this application note and the timing parameters listed in the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book.

For the most precise timing results, you should use the MAX+PLUS II Timing Analyzer, which accounts for the effects of secondary factors such as placement and fan-out.

This application note defines device internal and external timing parameters, and illustrates the timing model for the FLEX 8000 device family.

Familiarity with FLEX 8000 architecture and characteristics is assumed. Refer to the *FLEX 8000 Programmable Logic Device Family Data Sheet* for a complete description of the FLEX 8000 architecture and for specific values for timing parameters listed in this application note.

Internal Timing Parameters

The timing delays contributed by individual FLEX 8000 architectural elements are called internal timing parameters, which cannot be measured explicitly. All internal timing parameters are shown in italic type. The following list defines the internal timing parameters for the FLEX 8000 device family.

t_{IN} I/O input pad and buffer delay. The time required for a signal on an I/O pin, used as an input, to reach a row or column channel of the FastTrack Interconnect.

t_{DIN_D} Dedicated input data delay. The time required for a signal, used as a data input, to reach a logic element (LE) from a dedicated input pin. The t_{DIN_D} delay is a function of fan-out and the distance between the source pin and destination LEs. The value shown in the *FLEX 8000 Programmable Logic Device Family Data Sheet* is the longest delay possible for a pin with a fan-out of four LEs. However, the value generated by the MAX+PLUS II Timing Analyzer is more accurate because it includes considerations of the

fan-out and the relative locations of the source pin and destination LEs of the design.

t_{DIN_C} Dedicated input control delay. The delay of a signal coming from a dedicated input pin that is used as an LE register control. These signals include the clock, clear, and preset inputs to the LE register.

t_{DIN_IO} Dedicated input I/O control delay. The delay of a signal from a dedicated input pin that is used as an I/O element (IOE) register control. These signals include the clock and clear inputs to the IOE register and the output enable control of the IOE's tri-state buffer.

t_{COL} FastTrack Interconnect column delay. The delay incurred by a signal that requires routing through a column channel in the FastTrack Interconnect.

t_{ROW} FastTrack Interconnect row delay. The delay incurred by a signal that requires routing through a row channel in the FastTrack Interconnect. The t_{ROW} delay is a function of fan-out and the distance between the source and destination LEs. The value shown in the *FLEX 8000 Programmable Logic Device Family Data Sheet* is the longest delay possible for an LE with a fan-out of four LEs. However, the value generated by the MAX+PLUS II Timing Analyzer is more accurate because it includes considerations of the fan-out and the relative locations of the source and destination LEs of the design.

t_{LOCAL} Local interconnect delay. The delay incurred by a signal routed between LEs in the same logic array block (LAB).

$t_{LABCARRY}$ Carry chain delay to the next LAB. The delay incurred by a carry-out signal that carries into the next LAB in the row.

$t_{LABCASC}$ Cascade chain delay to the next LAB. The delay incurred by a cascade-out signal that cascades into the next LAB in the row.

t_{LUT} Look-up table (LUT) delay. The delay incurred by generating an LUT output from the local LAB interconnect signal.

t_{RLUT} LUT for LE feedback delay. The time required for the output of an LE to be fed back and used to generate the LUT output in the same LE.

t_{CLUT}	Carry chain LUT delay. The delay incurred by a carry chain signal that is used to generate the LUT output.
t_{CGEN}	Carry-out generation delay. The delay incurred by generating a carry-out signal from a local LAB interconnect signal.
t_{CGENR}	Carry-out generation using LE feedback delay. The delay incurred by generating a carry-out signal from the feedback of the LE.
t_{CICO}	Carry-in, carry-out delay. The delay incurred by generating a carry-out signal that uses the carry-in signal from the previous LE.
t_{C}	Register control delay. The time required for a signal to be routed to the clock, preset, or clear input of an LE register.
t_{GATE}	Cascade gate delay. The time required for a signal to pass through the cascade-generating AND gate in the LE. This delay is incurred, regardless of whether or not the cascade output is used.
t_{CASC}	Cascade chain delay. The time required for a cascade-out signal to be routed to the next LE in the same LAB. This delay, along with $t_{LABCASC}$, is also used to calculate the delay for a cascade-out signal to be routed to an LE in the next LAB in the row.
t_{CO}	LE clock-to-output delay. The delay from the rising edge of the LE register's clock to the time the data appears at the register output.
t_{COMB}	Combinatorial output delay. The time required for a combinatorial signal to bypass the LE register and become the output of the LE.
t_{SU}	LE register setup time. The minimum time that a signal is required to be stable at the LE register input before the register clock's rising edge to ensure that the register correctly stores the input data.
t_{H}	LE register hold time. The minimum time that a signal is required to be stable at the LE register input after the register clock's rising edge to ensure that the register correctly stores the input data.

t_{PRE}	LE register preset delay. The delay from the assertion of the LE register's asynchronous preset input to the time the register output stabilizes at a logic high.
t_{CLR}	LE register clear delay. The delay from the assertion of the LE register's asynchronous clear input to the time the register output stabilizes at a logic low.
t_{IOD}	Output data delay. The delay incurred by a signal routed from the FastTrack Interconnect to an IOE.
t_{IOC}	IOE control delay. The delay for a signal used to control the I/O register's clock or clear input, or for the output enable control of the IOE's tri-state buffer.
t_{IOCO}	I/O register clock-to-output delay. The delay from the rising edge of the I/O register's clock to the time the data appears at the register output.
t_{IOCOMB}	I/O register bypass delay. The delay for a combinatorial signal to bypass the I/O register.
t_{IOSU}	I/O register setup time. The time required for a signal to be stable at the I/O register input before the register clock's rising edge to ensure that the register correctly stores the input data.
t_{IOH}	I/O register hold time. The time required for a signal to be stable at the I/O register input after the register clock's rising edge to ensure that the register correctly stores the input data.
t_{IOCLR}	I/O register clear delay. The delay from the time the I/O register's asynchronous clear input is asserted to the time the register output stabilizes at logical low.
t_{OD1}	Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V.
t_{OD2}	Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3 V.
t_{OD3}	Output buffer and pad delay with the Slow Slew Rate logic option turned on.

t_{XZ} Output buffer disable delay. The delay required for high impedance to appear at the output pin after the tri-state buffer's enable control is disabled.

t_{ZX1} Output buffer enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

t_{ZX2} Output buffer enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

t_{ZX3} Output buffer enable delay with the Slow Slew Rate logic option turned on and V_{CCIO} = 5.0 V or 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

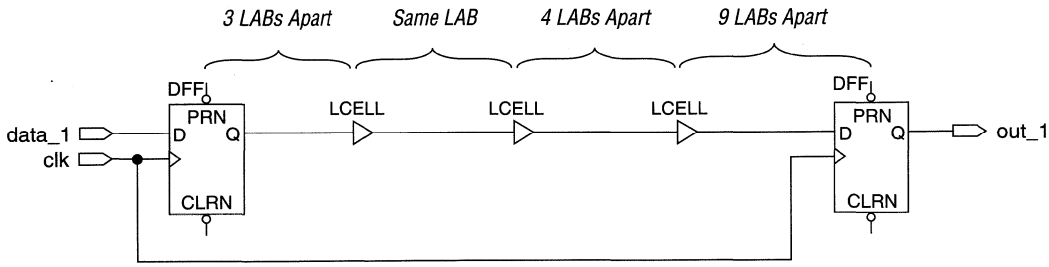
External Timing Parameters

External timing parameters represent actual pin-to-pin timing characteristics. Each external timing parameter consists of a combination of internal delay elements. For example, t_{DRR} is the AC operating specification. This is a worst-case value, derived from extensive performance measurements and is ensured by device testing. Other external timing parameters can be estimated by using the timing model or the equations in "Calculating Timing Delays" on page 464 of this application note.

t_{DRR} Register-to-register delay. The time required for the signal from one register to pass through four LEs via three row interconnects and four local interconnects to reach the D input of a second register. The test circuit used for this parameter is a register with an output that goes through three LCELL primitives in two different LABs; the last LCELL feeds another register in another LAB. Figure 1 shows this path. The relationship is also described in Figure 1.

The test circuit file (contained in **tdrr.exe**) is available on the Altera electronic bulletin board service (BBS) at (408) 954-0104 and on the Altera FTP site at **ftp.altera.com**. You can also access the Altera FTP site through Altera's world-wide web site at **http://www.altera.com**.

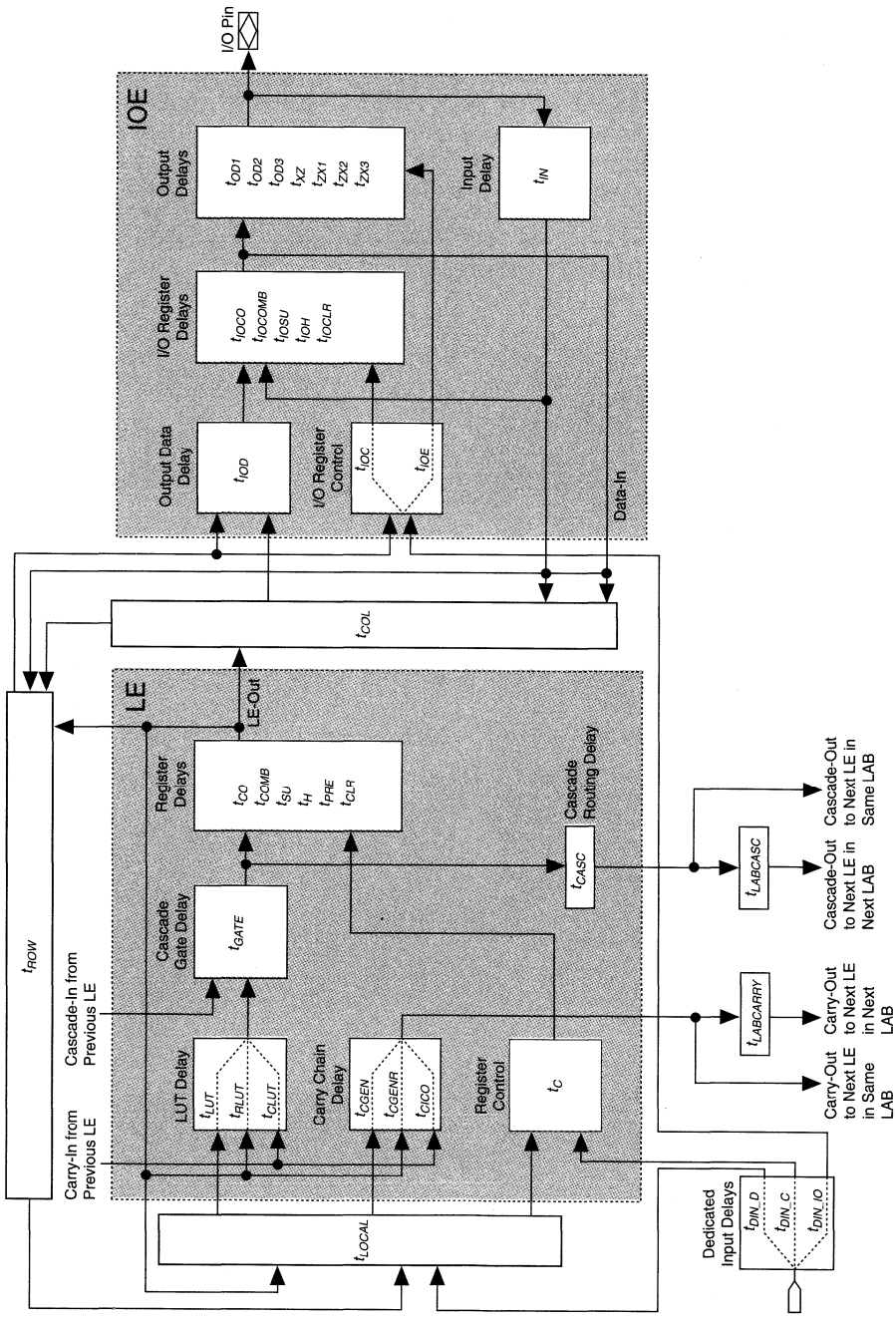
Figure 1. Path for t_{DRR} Circuit for 21-Column FLEX 8000 Devices



FLEX 8000 Timing Model

Timing models are simplified block diagrams that illustrate the propagation delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your FLEX 8000 device by examining the equations listed in the MAX+PLUS II Report File (**.rpt**) for the project. You can then add up the appropriate internal timing parameters to calculate the approximate propagation delays through the FLEX 8000 device. However, the MAX+PLUS II Timing Analyzer provides the most accurate timing information. Figure 2 shows the timing model for FLEX 8000 devices.

Figure 2. FLEX 8000 Timing Model



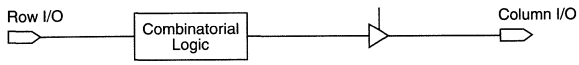
Calculating Timing Delays

You can calculate approximate pin-to-pin timing delays for FLEX 8000 devices with the timing model shown in Figure 2 and the internal timing parameters in the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book. Each external timing parameter is calculated from a combination of internal timing parameters. Figure 3 shows the FLEX 8000 device family LE external timing parameters. To calculate the delay for a signal that follows a different path through the FLEX 8000 device, refer to the timing model to determine which internal timing parameters to add together.

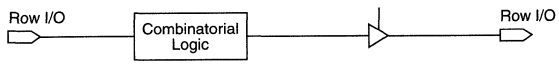
Figure 3. Logic Element External Timing Parameters (Part 1 of 3)

Combinatorial Delay

t_1



t_2



From Row I/O Inputs:

$t_1 = t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{COL} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

$t_2 = t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

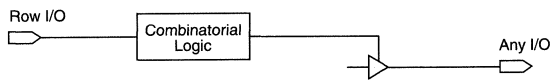
From Dedicated Inputs:

$t_1 = t_{DIN\_D} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{COL} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

$t_2 = t_{DIN\_D} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

Tri-State Enable/Disable Delay

t_{XZ} or t_{ZX}



From Row I/O Inputs through logic:

$t_{XZ}, t_{ZX} = t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOC} + (t_{XZ} \text{ or } t_{ZX1})$

Directly from Dedicated Inputs:

$t_{XZ}, t_{ZX} = t_{DIN\_IO} + t_{IOE} + (t_{XZ} \text{ or } t_{ZX1})$

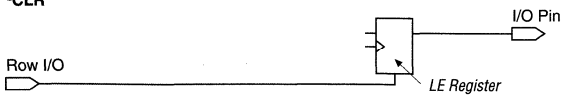
Directly from Row I/O Inputs:

$t_{XZ}, t_{ZX} = t_{IN} + t_{ROW} + t_{IOE} + (t_{XZ} \text{ or } t_{ZX1})$

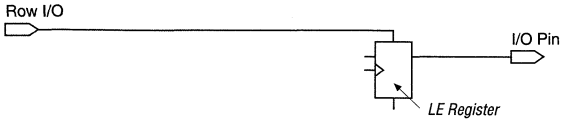
Figure 3. Logic Element External Timing Parameters (Part 2 of 3)

LE Register Clear & Preset Time

t_{CLR}



t_{PRE}



From Row I/O Inputs to Row or Column Outputs:

$$t_{CLR} = t_{IN} + t_{ROW} + t_{LOCAL} + t_C + t_{CLR} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

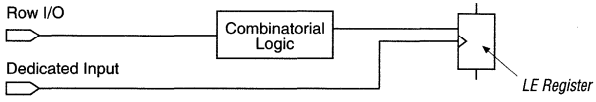
$$t_{PRE} = t_{IN} + t_{ROW} + t_{LOCAL} + t_C + t_{PRE} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

From Dedicated Inputs to Row or Column Outputs:

$$t_{CLR} = t_{DIN\_C} + t_C + t_{CLR} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

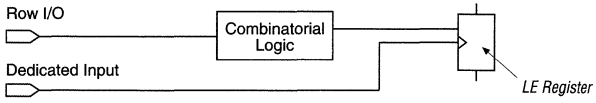
$$t_{PRE} = t_{DIN\_C} + t_C + t_{PRE} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

Register Setup Time from a Global Clock & Row I/O Data Input



$$t_{SU} = (t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE}) - (t_{DIN\_C} + t_C) + t_{SU}$$

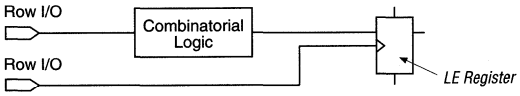
Register Hold Time from a Global Clock & Row I/O Data Input



$$t_H = (t_{DIN\_C} + t_C) - (t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE}) + t_H$$

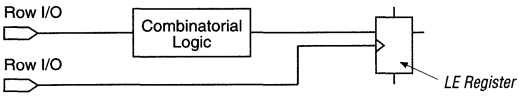
Figure 3. Logic Element External Timing Parameters (Part 3 of 3)

Asynchronous Setup Time from a Row I/O Clock & Row I/O Data Input



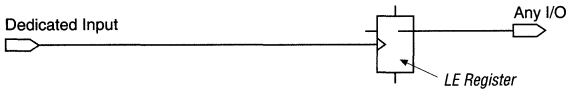
$$t_{ASU} = (t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE}) - (t_{IN} + t_{ROW} + t_{LOCAL} + t_C) + t_{SU}$$

Asynchronous Hold Time from a Row I/O Clock & Row I/O Data Input



$$t_{AH} = (t_{IN} + t_{ROW} + t_{LOCAL} + t_C) - (t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE}) + t_H$$

Clock-to-Output Delay from a Global Clock to Any Output



$$t_{CO} = t_{DIN\_C} + t_C + t_{CO} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

Asynchronous Clock-to-Output Delay from a Row I/O Clock to Any Output

$$t_{ACO} = t_{IN} + t_{ROW} + t_{LOCAL} + t_C + t_{CO} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

Figure 4 shows the FLEX 8000 device family I/O element (IOE) external timing parameters. To calculate the delay for a signal that follows a different path through the FLEX 8000 device, refer to the FLEX 8000 timing model shown in Figure 2 to determine which internal timing parameters to add together.

Figure 4. I/O Element External Timing Parameters (Part 1 of 2)

I/O Element Clear Time

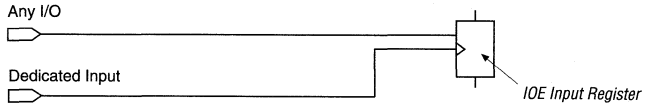
From I/O Inputs:

$$t_{CLR} = t_{IN} + t_{ROW} + t_{IOC} + t_{IOCLR} + t_{OD1}$$

From Dedicated Inputs:

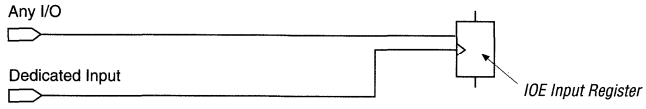
$$t_{CLR} = t_{DIN\_IO} + t_{IOC} + t_{IOCLR} + t_{OD1}$$

Register Setup Time from a Global Clock & Any I/O Data Input



$$t_{SU} = t_{IN} - (t_{DIN\_IO} + t_{IOC}) + t_{IOSU}$$

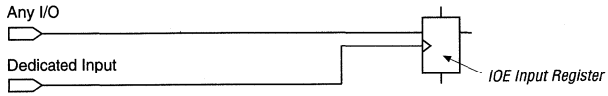
Register Hold Time from a Global Clock & Any I/O Data Input



$$t_{H} = (t_{DIN\_IO} + t_{IOC}) - t_{IN} + t_{IOH}$$

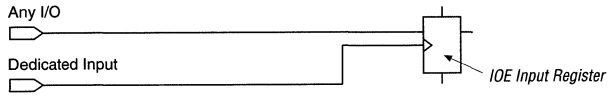
Figure 4. I/O Element External Timing Parameters (Part 2 of 2)

Asynchronous Setup Time from a Row I/O Clock & Any I/O Data Input



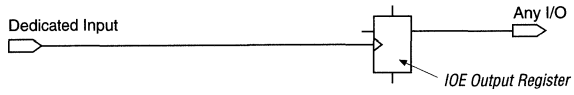
$$t_{ASU} = t_{IN} - (t_{IN} + t_{ROW} + t_{IOC}) + t_{SU}$$

Hold Time from a Row I/O Clock & Any I/O Data Input



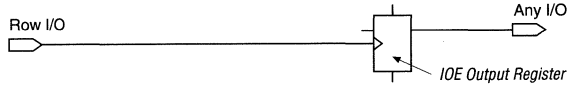
$$t_{AH} = (t_{IN} + t_{ROW} + t_{IOC}) - t_{IN} + t_{H}$$

Clock-to-Output Delay from a Global Clock to Any Output



$$t_{CO} = t_{DIN\_IO} + t_{IOC} + t_{IOCO} + t_{OD1}$$

Clock-to-Output Delay from a Row I/O Clock to Any Output



$$t_{ACO} = t_{IN} + t_{ROW} + t_{IOC} + t_{IOCO} + t_{OD1}$$

Timing Model vs. MAX+PLUS II Timing Analyzer

The MAX+PLUS II Timing Analyzer always provides the most accurate information on the performance of a design. However, hand calculations based on the timing model also provide a good estimate of the design performance. The MAX+PLUS II Timing Analyzer is more accurate because it takes into account three secondary factors that influence the t_{ROW} and t_{DIN_D} parameters:

- Fan-out for each signal in the delay path
- Positions of other loads relative to the source and destination
- Distance between signal source and destination

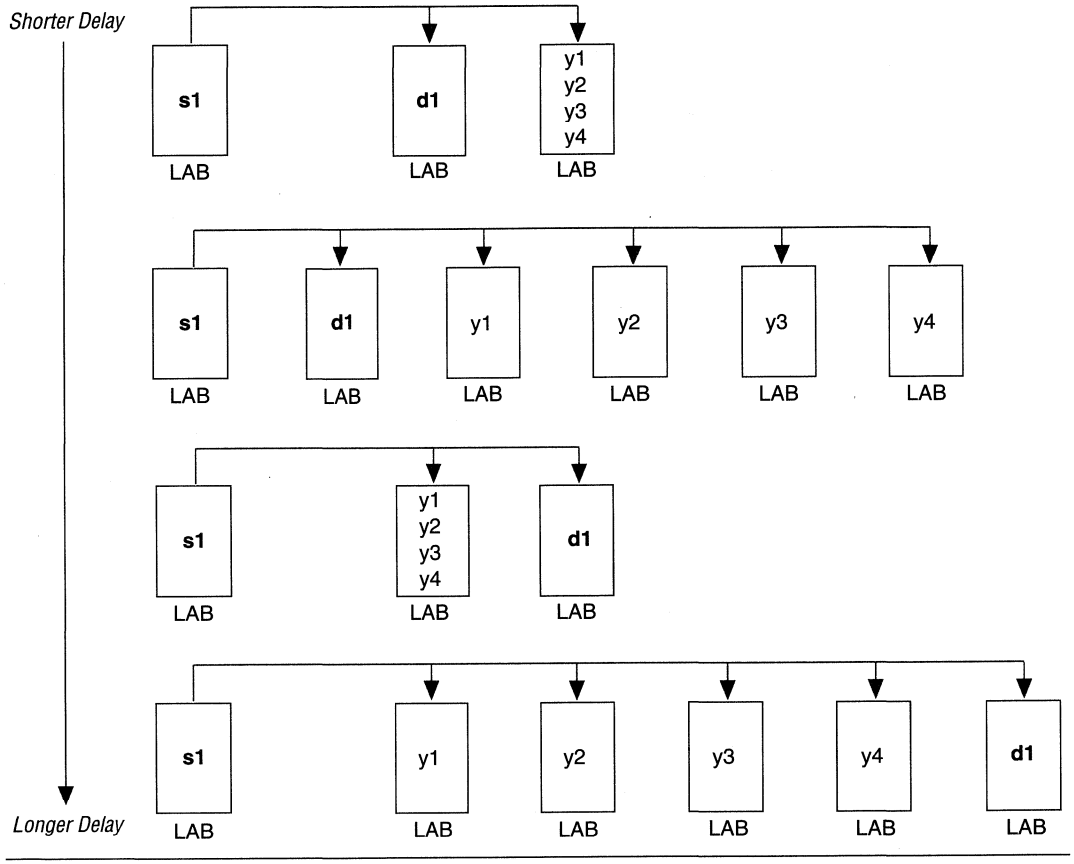
Fan-Out

The more loads a signal has to drive, the longer the delay across t_{ROW} and t_{DIN_D}. This delay is a function of the number of LABs that a signal source has to drive, as well as of the number of LEs in the LAB that use the signal. The number of LABs that a signal drives has a greater effect on the delay than the number of cells in the LAB that use the signal.

Load Distribution

The load distribution relative to the source and destination also affects the t_{ROW} and t_{DIN_D} delays. Consider a signal `s1` that feeds destination `d1` and logic elements `y[4..1]`. If `y[4..1]` are in different LABs, then `s1` has four additional loads. If, however, they are all in the same LAB, then `s1` has four shorter-delay loads. Therefore, the row interconnect delay from `s1` to `d1` is greater when each load `y[4..1]` is in a different LAB. Figure 5 illustrates the change in the t_{ROW} and t_{DIN_D} delays caused by variations in the position of `d1` and the distribution of `y[4..1]`.

Figure 5. Delay from s1 to d1 as a Function of Relative Position & Load Distribution



Distance

The distance between the source and destination LEs also affects the t_{ROW} and t_{DIN_D} parameters. For example, if s1 and d1 are pins on the left and right sides of a device, respectively, then the delay from s1, through one LCELL on the same row to d1 (i.e., the time required to traverse the length of the device) is the same no matter where the LCELL is placed. On the other hand, if s1 and d1 are both on the left side, then the delay from s1 to d1 depends on where the LCELL is placed. If the LCELL is on the right side (far from s1 and d1), then the delay is longer than if it is on the left side (close to s1 and d1).

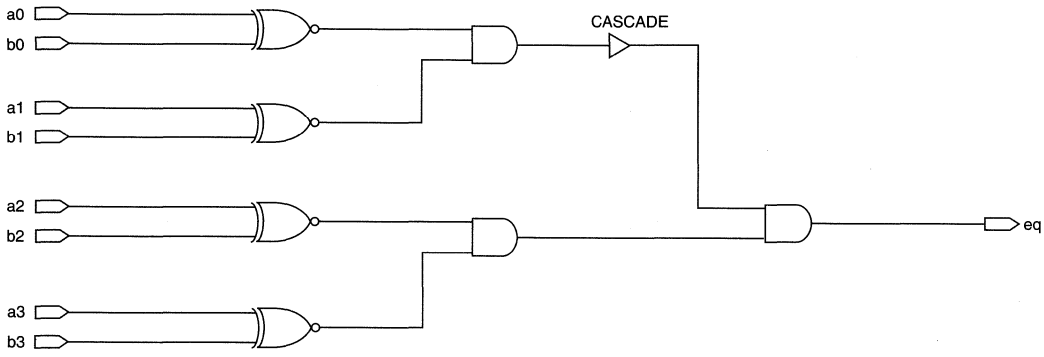
Examples

The following examples show how to use internal timing parameters to estimate the delays for real applications.

Example 1: 4-Bit Equality Comparator with Cascade

You can analyze the timing delays for circuits that have been subjected to minimization and logic synthesis. The synthesized equations are available in the MAX+PLUS II Report File (**.rpt**) for the project. These equations are structured so that you can quickly determine the logic implementation of any signal. For example, Figure 6 shows a 4-bit equality comparator.

Figure 6. 4-Bit Equality Comparator Circuit



The MAX+PLUS II Report File for the circuit in Figure 6 gives the equations for eq, the output of the comparator:

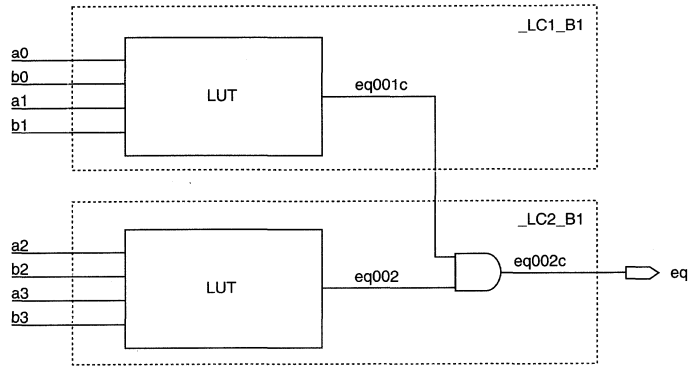
```
eq      =  _LC2_B1;
_LC2_B1 =  LCELL( _EQ002C);
_EQ002C =  _EQ002 & CASCADE( _EQ001C);
_EQ002  =  a2 & a3 & b2 & b3
           # a2 & !a3 & b2 & !b3
           # !a2 & a3 & !b2 & b3
           # !a2 & !a3 & !b2 & !b3;
```

The equation for _EQ001C cascades into the previous equation:

```
% _LC1_B1 =  LCELL( _EQ001C); %
_EQ001C   =  _EQ001;
_EQ001    =  a0 & a1 & b0 & b1
             # a0 & !a1 & b0 & !b1
             # !a0 & a1 & !b0 & b1
             # !a0 & !a1 & !b0 & !b1;
```

Figure 7 shows a synthesized 4-bit equality comparator.

Figure 7. Synthesized 4-Bit Equality Comparator



The output pin, eq, is the output of the second LE of a cascade chain. The combinatorial LE, _LC1_B1, implements the comparison of the first two bits. The second two bits are implemented in the LUT of _LC2_B1. The outputs of these two LEs are then cascaded together to form the output of _LC2_B1.

If a2 and eq are row I/O pins, then the timing delay from a2 to eq can be estimated by adding the following parameters:

$t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

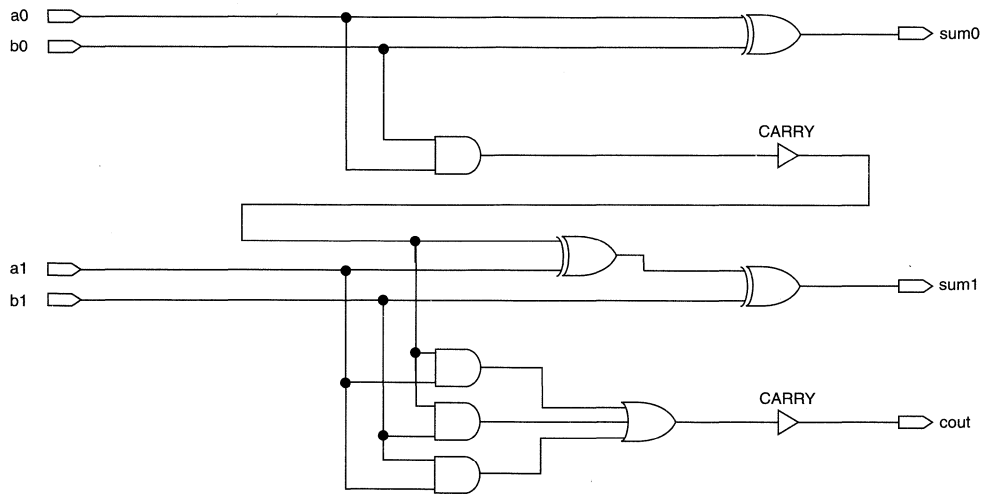
If a0 is a row I/O pin, the timing delay from a0 to eq can be estimated by adding the following parameters:

$t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{CASC} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

Example 2: 2-Bit Adder Using Carry Chain

FLEX 8000 devices have specialized resources that implement complex arithmetic functions. For instance, adders and counters require a carry function to determine whether or not to increment the next significant bit. The FLEX 8000 architecture has a built-in carry chain that performs this function. This example explains how to estimate the delay for a 2-bit adder that uses the carry chain, shown in Figure 8.

Figure 8. 2-Bit Adder Implemented with a Carry Chain



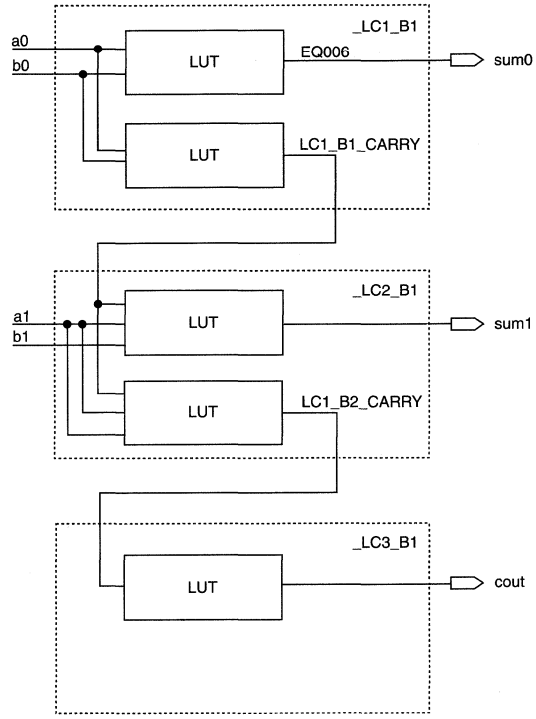
The MAX+PLUS II Report File contains the following equations for the 2-bit adder in Figure 8:

```
cout            =  _LC3_B1;
sum0            =  _LC1_B1;
sum1            =  _LC2_B1;
_LC3_B1         =  LCELL(_LC2_B1_CARRY);
_LC1_B1_CARRY   =  CARRY(_EQ001);
_EQ001          = a0 & b0;
_LC2_B1_CARRY   = CARRY(_EQ002);
EQ002           = b1 & _LC1_B1_CARRY
                   # a1 & _LC1_B1_CARRY
                   # a1 & b1;

_LC2_B1_CARRY   = LCELL(_EQ003);
_EQ003          = !a1 & !b1 & _LC1_B1_CARRY
                   # !a1 & b1 & !_LC1_B1_CARRY
                   # a1 & b1 & _LC1_B1_CARRY
                   # a1 & !b1 & !_LC1_B1_CARRY
_LC1_B1         =  LCELL(_EQ004);
_EQ004          =  a0 & !b0
                   # !a0 & b0;
```

Figure 9 shows a synthesized 2-bit adder.

Figure 9. Synthesized 2-Bit Adder



The cin input carries into _LC2_B1, and the output of the LE _LC2_B1 is SUM1 and _LC2_B1_CARRY. These signals are then used to generate sum2 and _LC3_B1_CARRY. The output pin, COUT, must pass through the LCELL _LC4_B1 because a CARRY buffer cannot directly feed a pin.

If cin to sum1 are on a row IOE, the pin-to-pin delay between them can be estimated by adding the following parameters:

$t_{IN} + t_{ROW} + t_{LOCAL} + t_{CGEN} + t_{CLUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

If cin to cout are on a row IOE, the pin-to-pin delay between them can be estimated by adding the following parameters:

$t_{IN} + t_{ROW} + t_{LOCAL} + t_{CGEN} + t_{CICO} + t_{CICO} + t_{CLUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

Conclusion

The FLEX 8000 device architecture has predictable internal timing delays that can be estimated based on signal synthesis and placement. Using the FLEX 8000 timing model shown in Figure 2 and the timing parameters in the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book, you can estimate the performance of a design before compilation. However, the MAX+PLUS II Timing Analyzer provides the most accurate timing information. These methods enable you to accurately predict your design's in-system timing performance.

Notes:

Understanding MAX 9000 Timing

June 1996, ver. 1 Application Note 77

Introduction

Altera devices provide predictable device performance that is consistent from simulation to application. Before placing a device in a circuit, you can determine the worst-case timing delays for any design. You can calculate propagation delays either with the MAX+PLUS II Timing Analyzer or with the timing models given in this application note and the timing parameters listed in the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book.

☞ For the most precise timing results, you should use the MAX+PLUS II Timing Analyzer, which accounts for the effects of secondary factors such as placement and fan-out.

This application note defines MAX 9000 device internal and external timing parameters, and illustrates the timing model for the MAX 9000 device family.

Familiarity with MAX 9000 architecture and characteristics is assumed. Refer to the *MAX 9000 Programmable Logic Device Family Data Sheet* for a complete description of the MAX 9000 architecture, and for the specific values of the timing parameters listed in this application note.

Internal Timing Parameters

The timing delays contributed by individual MAX 9000 architectural elements are called internal timing parameters, which cannot be measured explicitly. All internal timing parameters are shown in italic type. The following list defines the internal timing parameters for the MAX 9000 device family.

t_{INCOMB} I/O input pad and buffer delay. This delay applies to I/O pins used as inputs, and represents the time required for a signal on an I/O pin to reach a row or column interconnect on the FastTrack Interconnect.

t_{INREG} I/O input pad to I/O register delay. This delay applies to I/O pins used as inputs, and represents the time required for a signal on an I/O pin to reach the data input of an I/O register.

t_{DIN_D}	Dedicated input data delay. This delay represents the time required for a signal originating from a dedicated input pin and used as a data input to a macrocell to reach a row interconnect on the FastTrack Interconnect.
t_{DIN_CLK}	Dedicated input clock delay. The delay for a signal that originates from a dedicated input pin and is used as a macrocell register clock.
t_{DIN_CLR}	Dedicated input clear delay. The delay for a signal that originates from a dedicated input pin and is used as a macrocell register clear.
t_{DIN_IO}	Dedicated input I/O control delay. The delay for a signal that originates from a dedicated input pin (including the enable and clear inputs to the I/O register, and the output enable control of the I/O cell's tri-state buffer) and is used as an I/O register control.
t_{DIN_IOC}	Dedicated input I/O clock delay. The delay for a signal that originates from a dedicated input pin and is used as an I/O register clock.
t_{COL}	FastTrack Interconnect column delay. The delay incurred by a signal that requires routing through a column interconnect. The t_{COL} delay is a function of fan-out and of the distance between the source and destination macrocells. t_{COL} is a worst-case value for most column signals.
t_{ROW}	FastTrack Interconnect row delay. The delay incurred by a signal that requires routing through a row interconnect. The t_{ROW} delay is a function of fan-out and of the distance between the source and destination macrocells. t_{ROW} is a worst-case value for most row signals.
t_{LOCAL}	Logic array block (LAB) local array delay. The delay incurred by a signal that is routed from one macrocell to another macrocell in the same LAB.
t_{LAD}	Logic array delay. The time required for a logic signal to propagate through a macrocell's AND-OR-XOR structure.
t_{LAC}	Logic array control delay. The AND array delay for register control functions, including the clear and preset inputs to the macrocell register.

t_{IC}	Array clock delay. The delay through a macrocell's clock product term to the register's clock input.
t_{EN}	Register enable delay. The AND array delay for the macrocell register enable.
t_{SEXP}	Shared expander delay. The delay of a signal through the AND-NOT structure of the shared expander product-term array that is fed back into the local array.
t_{PEXP}	Parallel expander delay. The additional delay incurred by adding parallel expander product terms to the macrocell product terms. An additional t_{PEXP} delay is added to the timing path for each group of up to five parallel expanders added to a macrocell.
t_{RD}	Macrocell clock-to-output delay. The delay from the rising edge of the macrocell register's clock to the time the data appears at the register output.
t_{COMB}	Macrocell combinatorial output delay. The delay required for a signal to bypass the macrocell register and become the macrocell output.
t_{SU}	Macrocell register setup time. The time required for a signal to be stable at the macrocell register input before the register clock's rising edge to ensure that the register correctly stores the input data.
t_{H}	Macrocell register hold time. The time required for a signal to be stable at the macrocell register input after the register clock's rising edge to ensure that the register correctly stores the input data.
t_{PRE}	Macrocell register preset delay. The delay from the assertion of the macrocell register's asynchronous preset input to the stabilization of the register output at logical high.
t_{CLR}	Macrocell register clear delay. The delay from the assertion of the macrocell register's clear input to the stabilization of the register output at logical low.
t_{FTD}	FastTrack Interconnect drive delay. The delay from the time when a signal is available on the macrocell output to the time that signal is driven onto the row or column interconnect.

t_{IODR}	Output data delay for the row. The delay incurred by signals routed from a row to an I/O cell.
t_{IODC}	Output data delay for the column. The delay incurred by signals routed from a column to an I/O cell.
t_{IOC}	I/O cell control delay. The delay incurred by a signal that requires routing on the peripheral bus and controls the I/O register's enable or clear input or controls the output enable of the I/O cell's tri-state buffer. The t_{IOC} delay is a function of fan-out and the distance between the source row and the destination I/O cells (IOCs). The t_{IOC} delay is a worst-case value for a fan-out of 8.
t_{IORD}	I/O register clock-to-output delay. The delay from the rising edge of the I/O register's clock to the time the data appears at the register output.
t_{IOCOMB}	I/O register bypass delay. The delay for a signal to bypass the I/O register.
t_{IOSU}	I/O register setup time. The time required for a signal to be stable at the I/O register input before the register clock's rising edge to ensure that the register correctly stores the input data.
t_{IOH}	I/O register hold time. The time required for a signal to be stable at the I/O register input after the register clock's rising edge to ensure that the register correctly stores the input data.
t_{IOCLR}	I/O register clear delay. The delay from the time when the I/O register's asynchronous clear input is asserted to the time the register output stabilizes at logical low.
t_{IOFD}	I/O register feedback delay. The delay from the output of the I/O register to the row and column interconnect.
t_{OD1}	Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V.
t_{OD2}	Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3 V.
t_{OD3}	Output buffer and pad delay with the Slow Slew Rate logic option turned on.

t_{XZ} Output buffer disable delay. The delay required for high impedance to appear at the output pin after the tri-state buffer's enable control is disabled.

t_{ZX1} Output buffer enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

t_{ZX2} Output buffer enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

t_{ZX3} Output buffer enable delay with the Slow Slew Rate logic option turned on and V_{CCIO} = 5.0 V or 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

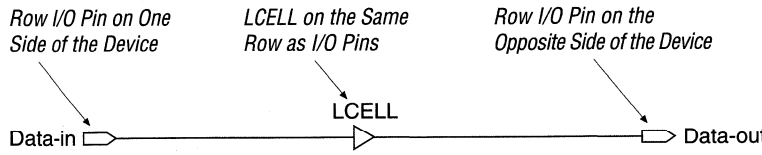
t_{LPA} Low-power adder. The delay associated with macrocells in low-power operation. In low-power mode, t_{LPA}, must be added to the LAB local array delay (t_{LOCAL}).

External Timing Parameters

External timing parameters represent actual pin-to-pin timing characteristics. Each external timing parameter consists of a combination of internal timing parameters. The *MAX 9000 Programmable Logic Device Family Data Sheet* gives the values of the external timing parameters. These external timing parameters are worst-case values, derived from extensive performance measurements and ensured by device testing. All external timing parameters are shown in bold type. The following list defines external timing parameters for the MAX 9000 family.

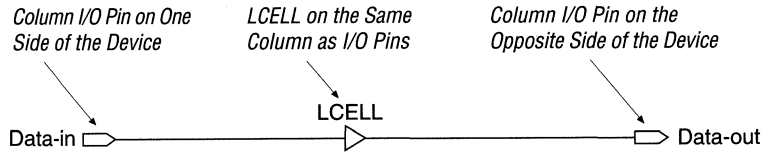
t_{PD1} Row I/O pin to non-registered row pin delay. The time required for a signal on any row input to propagate through the combinatorial logic in a macrocell and appear at a row output pin. The test circuit for this parameter is a row input pin on one side of the device that feeds a row output on the opposite side of the device through an LCELL in that row. See Figure 1.

Figure 1. Test Circuit for t_{PD1}



t_{PD2} Column I/O pin to non-registered column pin delay. The time required for a signal on any column input to propagate through the combinatorial logic in a macrocell and appear at a column output pin. The test circuit for this parameter is a column input pin on one side of the device that feeds a column output on the opposite side of the device through an LCELL in that column. See Figure 2.

Figure 2. Test Circuit for t_{PD2}



t_{FSU} Global clock setup time for I/O cell register. The time the input data must be present at the I/O pin before the global (synchronous) clock signal is asserted at the clock pin.

t_{FH} Global clock hold time for I/O cell register. The time the input data must be present at the I/O pin after the global clock signal is asserted at the clock pin.

t_{CO} Global clock to output delay for macrocell registers. The time required to obtain a valid row output after the global clock is asserted at the clock pin.

t_{FCO} Global clock to output delay for I/O cell register. The time required to obtain a valid output after the global clock is asserted at the clock pin.

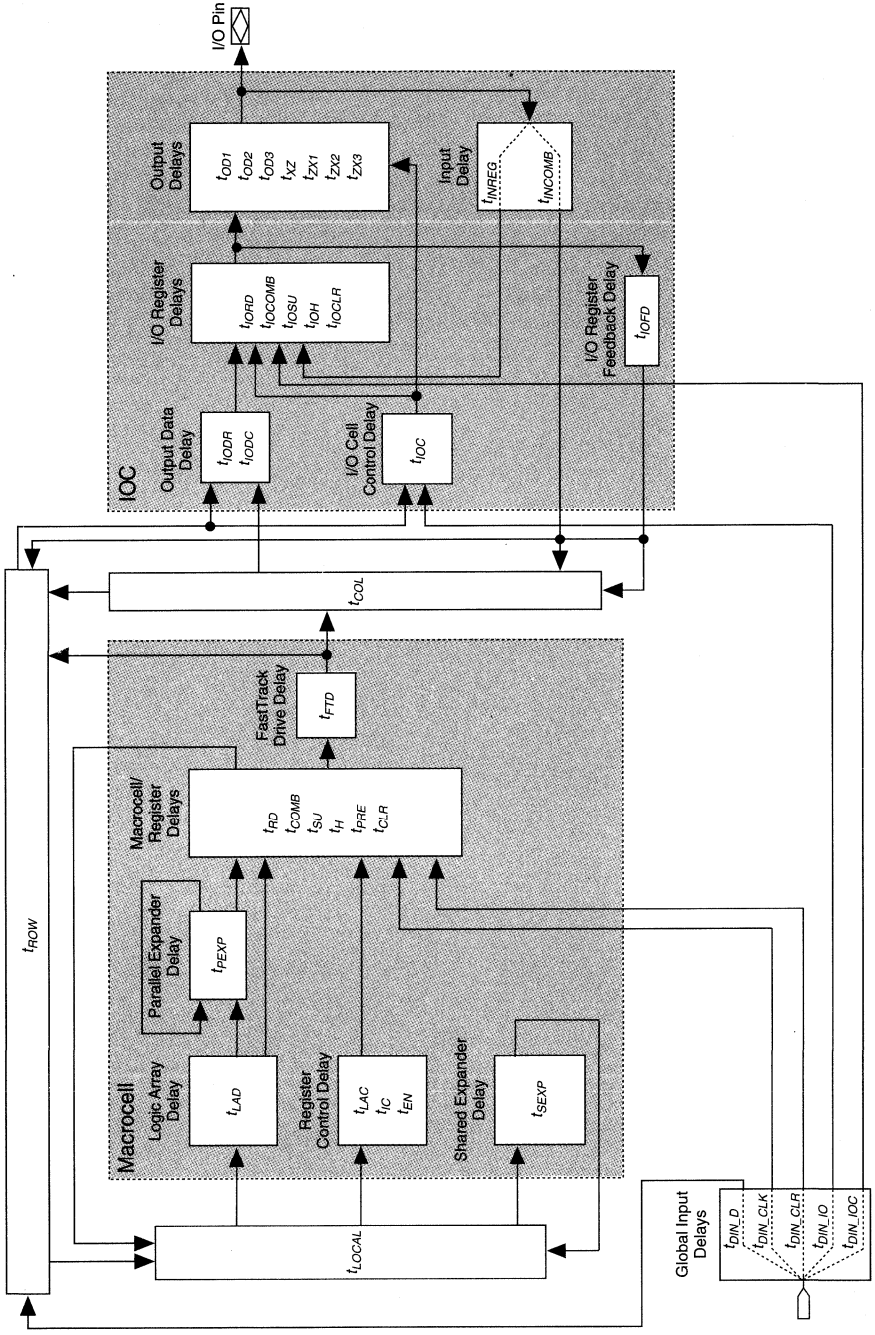
t_{CNT} Minimum global clock period. The minimum period maintained by a globally clocked, 16-bit loadable, enabled, up/down counter.

t_{ACNT}	Minimum array clock period. The minimum period maintained by a 16-bit loadable, enabled, up/down counter when it is clocked by a signal from the array.

MAX 9000 Timing Model

Timing models are simplified block diagrams that illustrate the propagation delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your MAX 9000 device by examining the equations listed in the MAX+PLUS II Report File (**.rpt**) for the project. You can then add up the appropriate internal timing parameters to calculate the approximate propagation delays through the MAX 9000 device. However, the MAX+PLUS II Timing Analyzer provides the most accurate timing information. Figure 3 shows the timing model for MAX 9000 devices.

Figure 3. MAX 9000 Timing Model



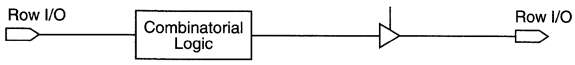
Calculating Timing Delays

You can calculate approximate pin-to-pin timing delays for MAX 9000 devices with the timing model shown in Figure 3 and the internal timing parameters in the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book. Each external timing parameter is calculated from a combination of internal timing parameters. Figure 4 shows the MAX 9000 device family macrocell external timing parameters. To calculate the delay for a signal that follows a different path through the MAX 9000 device, refer to the timing model to determine which internal timing parameters to add together.

Figure 4. Macrocell External Timing Parameters (Part 1 of 3)

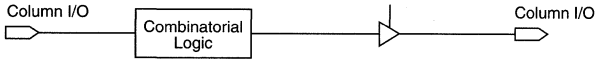
Combinatorial Delay

From Row I/O Inputs to Row I/O Outputs:



$$t_{PD1} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

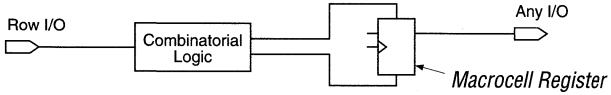
From Column I/O Inputs to Column I/O Outputs:



$$t_{PD2} = t_{INCOMB} + t_{COL} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{COL} + t_{IODC} + t_{IOCOMB} + t_{OD1}$$

Macrocell Register Clear & Preset Time

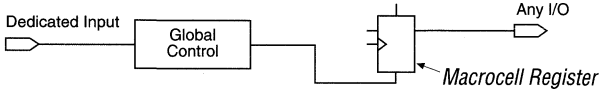
From Row I/O Inputs to Row or Column Outputs:



$$t_{CLR} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAC} + t_{CLR} + t_{FTD} + (t_{ROW} \text{ or } t_{COL}) + (t_{IODR} \text{ or } t_{IODC}) + t_{IOCOMB} + t_{OD1}$$

$$t_{PRE} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAC} + t_{PRE} + t_{FTD} + (t_{ROW} \text{ or } t_{COL}) + (t_{IODR} \text{ or } t_{IODC}) + t_{IOCOMB} + t_{OD1}$$

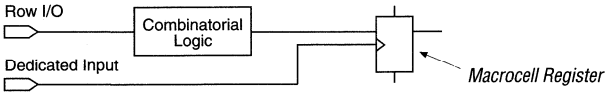
From Dedicated Inputs to Row or Column Outputs:



$$t_{CLR} = t_{DIN\_CLR} + t_{CLR} + t_{FTD} + (t_{ROW} \text{ or } t_{COL}) + (t_{IODR} \text{ or } t_{IODC}) + t_{IOCOMB} + t_{OD1}$$

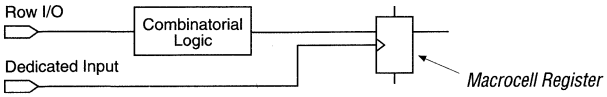
Figure 4. Macrocell External Timing Parameters (Part 2 of 3)

Register Setup Time from a Global Clock & Row I/O Data Input



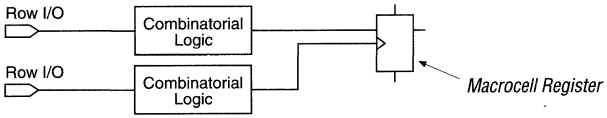
$$t_{SU} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) - t_{DIN\_CLK} + t_{SU}$$

Register Hold Time from a Global Clock & Row I/O Data Input



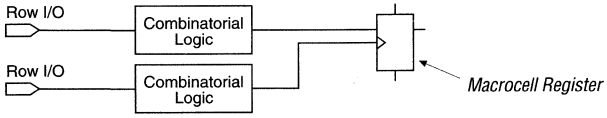
$$t_{H} = t_{DIN\_CLK} - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) + t_{H}$$

Asynchronous Setup Time from a Row I/O Clock & Row I/O Data Input



$$t_{ASU} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{IC}) + t_{SU}$$

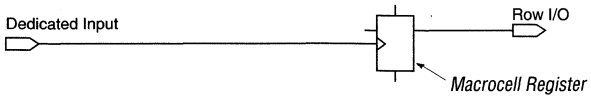
Asynchronous Hold Time from a Row I/O Clock & Row I/O Data Input



$$t_{AH} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{IC}) - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) + t_{H}$$

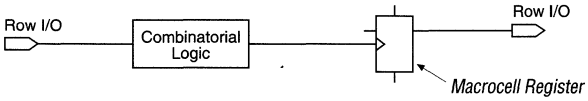
Figure 4. Macrocell External Timing Parameters (Part 3 of 3)

Clock-to-Output Delay from a Global Clock & Row Output



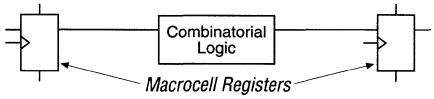
$$t_{CO} = t_{DIN\_CLK} + t_{RD} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

Asynchronous Clock-to-Output Delay from a Row I/O Clock & Row Output



$$t_{ACO} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{IC} + t_{RD} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

Counter Frequency



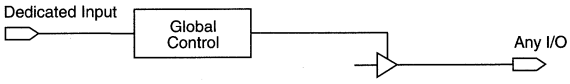
$$t_{CNT} = t_{RD} + t_{LOCAL} + t_{LAD} + t_{SU}$$

Figure 5 shows the MAX 9000 device family I/O cell (IOC) external timing parameters. To calculate the delay for a signal that follows a different path through the device, refer to the MAX 9000 timing model shown in Figure 3 on page 484 to determine which internal timing parameters to add together.

Figure 5. I/O Cell External Timing Parameters (Part 1 of 2)

Tri-State Enable & Disable Delay

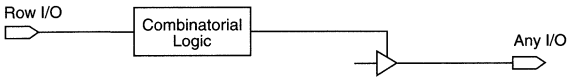
For Global Output Enable:



$t_{XZ} = t_{DIN\_IO} + t_{IOC} + t_{XZ}$

$t_{ZX} = t_{DIN\_IO} + t_{IOC} + t_{ZX1}$

For Row Output Enable:

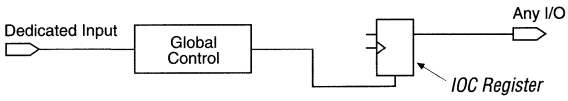


$t_{PXZ} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{XZ}$

$t_{PZX} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{ZX1}$

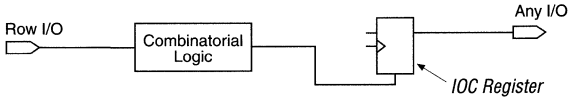
I/O Register Clear Time

From Dedicated Inputs:



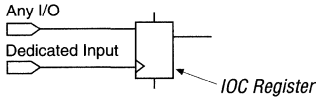
$t_{CLR} = t_{DIN\_IO} + t_{IOC} + t_{IOCLR} + t_{OD1}$

From Row I/O Inputs:



$t_{CLR} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{IOCLR} + t_{OD1}$

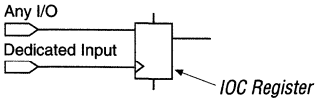
Register Setup Time from a Global Clock



$t_{FSU} = t_{INREG} - t_{DIN\_IOC} + t_{IOSU}$

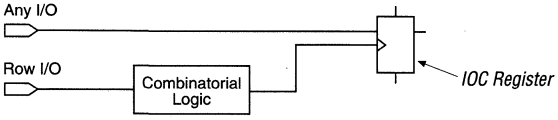
Figure 5. I/O Cell External Timing Parameters (Part 2 of 2)

Register Hold Time from a Global Clock



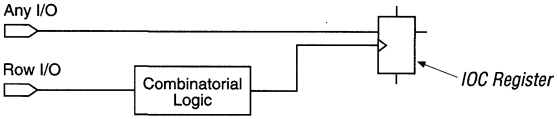
$$t_{FH} = t_{DIN\_IOC} - t_{INREG} + t_{IOH}$$

Asynchronous Setup Time from a Row I/O Clock



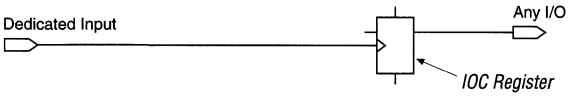
$$t_{FASU} = t_{INREG} - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC}) + t_{IOSU}$$

Asynchronous Hold Time from a Row I/O Clock



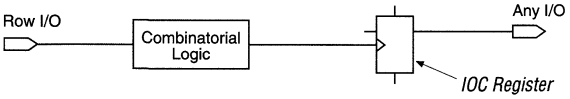
$$t_{FAH} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC}) - t_{INREG} + t_{IOH}$$

Clock-to-Output Delay from a Global Clock



$$t_{FCO} = t_{DIN\_IOC} + t_{IORD} + t_{OD1}$$

Asynchronous Clock-to-Output Delay from a Row I/O Clock



$$t_{ACO} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{IORD} + t_{OD1}$$

Timing Model vs. MAX+PLUS II Timing Analyzer

The MAX+PLUS II Timing Analyzer always provides the most accurate information on the performance of a design. However, hand calculations based on the timing model also provide a good estimate of the design performance. The MAX+PLUS II Timing Analyzer is more accurate because it takes into account two factors that affect the t_{ROW}, t_{COL}, and t_{IOC} internal timing parameters:

- Fan-out for each signal in the delay path
- Distance between signal source and destination

Fan-Out

The more loads a signal has to drive, the longer the delay across t_{ROW}, t_{COL}, and t_{IOC}. For t_{ROW}, this loading is a function of the number of LABs that a signal source has to drive. For t_{COL}, this loading is a function of the number of rows that a signal source has to reach. For t_{IOC}, this loading is a function of the number of IOCs that a signal source controls. For example, consider a signal `s1` going to destination `d1` that also goes to macrocells `y[4..1]`. If `y[4..1]` are in different LABs, then `s1` has four loads. If, however, they are all in the same LAB, then `s1` has only one load. Therefore, the row interconnect delay from `s1` to `d1` is greater when each macrocell `y[4..1]` is in a different LAB. The same is true for a column delay. If `y[4..1]` are in different rows, then the delay will be longer than if they are in the same row.

Distance

The distance between the source and destination also affects the t_{ROW}, t_{COL}, and t_{IOC} parameters. For example, if `s1` and `d1` are pins on the left and right sides of a device, respectively, then the delay from `s1` through one `LCELL` on the same row to `d1` (i.e., the time required to traverse the length of the device) is the same no matter where the `LCELL` is placed. On the other hand, if `s1` and `d1` are both on the same side, then the delay from `s1` to `d1` depends on where the `LCELL` is placed. If the `LCELL` is on the opposite side from `s1` and `d1`, then the delay is longer than if the `LCELL` is on the same side as `s1` and `d1`. The same is true for the delay incurred by traversing a column. For t_{IOC}, as the IOC becomes farther away from the source row, the delay incurred by traversing the peripheral bus increases.

Examples

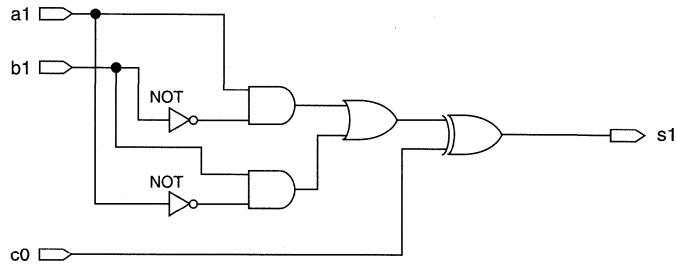
The following examples show how to use internal timing parameters to estimate the delays for real applications.

Example 1: First Bit of 7483 TTL Macrofunction

You can analyze the timing delays for circuits that have been subjected to minimization and logic synthesis. A MAX+PLUS II Report File (**.rpt**) lists the synthesized equations for the project. These equations are structured so that you can quickly determine the logic implementation of any signal. Figure 6 shows part of a 7483 TTL macrofunction (a 4-bit full adder). The Report File for this TTL macrofunction circuit gives the following equations for s1, the least significant bit of the adder:

```
% s1       = _LC9_B1 %
s1         = LCELL( _EQ002 $ c0);
 _EQ002    = !a1 &  b1
           #  a1 & !b1;
```

Figure 6. Adder Logic Timing for MAX 9000 Architecture



The s1 output is the output of macrocell 9 in LAB b1 (LC9_B1), which contains combinatorial logic. The combinatorial logic LCELL (_EQ002 $ c0) represents the XOR of the intermediate equation _EQ002 and the carry-in c0. In turn, _EQ002 is logically equivalent to the XOR of inputs b1 and a1. Therefore, the timing delay for s1 can be estimated by adding the following parameters:

$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$

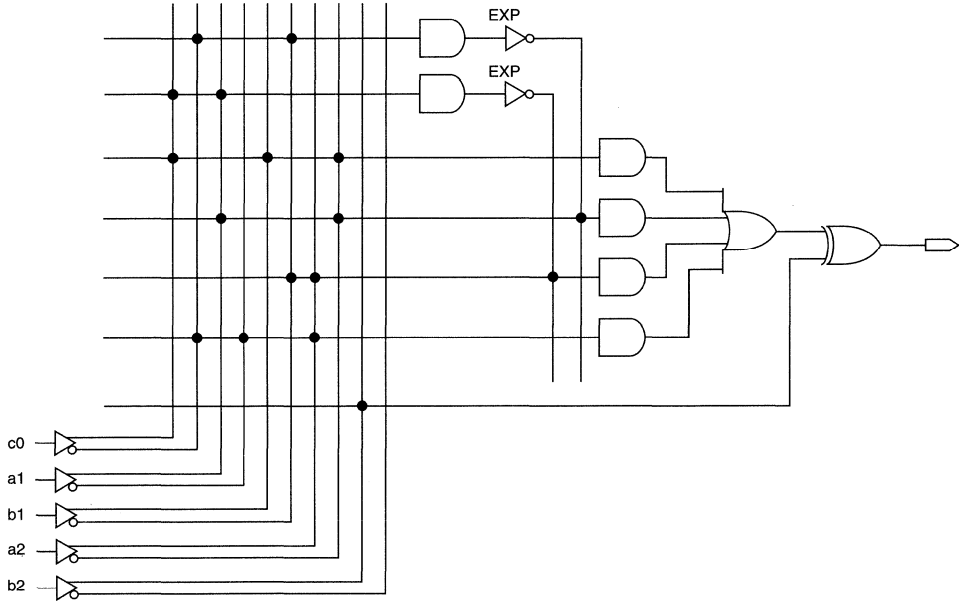
Example 2: Second Bit of 7483 TTL Macrofunction

The expander array delay, t_{SEXP}, is added to the delay element for complex logic that requires expanders (represented as _X<*number*> in Report Files). The second bit of the 7483 adder macrofunction, s2, requires shared expanders. The equations are as follows:

```
% s2       = _LC8_B1 %
s2         = LCELL( _EQ003 $ b2);
 _EQ003    = !a2 &  b1 &  c0
           #  a1 & !a2 &  _X005
           #  a2 & !b1 &  _X006
           # !a1 &  a2 & !c0;
 _X005     = EXP(!b1 & !c0);
 _X006     = EXP( a1 &  c0);
```

Figure 7 shows how to map the logic structure onto the MAX 9000 architecture with this equation.

Figure 7. Adder Equations Mapped to MAX 9000 Architecture



Therefore, the timing delay for s2 can be estimated by adding the following parameters:

$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{SEXP} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$

Example 3: Second Bit of 7483 TTL Macrofunction with Parallel Expanders

The MAX+PLUS II Compiler uses parallel expanders if the Parallel Expanders logic option is turned on when a project is compiled for MAX 9000 devices. When parallel expanders are used and no sharable expanders are used, the equation for s2 is as follows:

```
% _LC10_B1 borrows parallel expanders from _LC9_B1 %
% s2       = _LC10_B1 %
s2         = LCELL( _EQ003 $ b2);
 _EQ003    =  a1 & !a2 &  c0
           #  a1 & !a2 &  b1
           # !a2 &  b1 &  c0
           # !a1 &  a2 & !b1
           #  a2 & !b1 & !c0
           # !a1 &  a2 & !c0;
```

Therefore, the timing delay for the s2 bit of the 7483 adder macrofunction can be estimated by adding the following parameters:

$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{PEXP} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$

Example 4: First Bit of 7483 TTL Macrofunction in Low-Power Mode

If a macrocell in a MAX 9000 device is set for low-power mode, you must add the low-power adder delay to the total delay through that macrocell. The estimated s1 delay becomes:

$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LPA} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$

Conclusion

The MAX 9000 device architecture has predictable internal timing delays that can be estimated based on signal synthesis and placement. Using the MAX 9000 timing model shown in Figure 3 and the timing parameters in the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book, you can estimate the performance of a design before compilation. However, the MAX+PLUS II Timing Analyzer provides the most accurate timing information. These two methods enable you to accurately predict your design's in-system timing performance.

Understanding MAX 7000, MAX 5000 & Classic Timing

June 1996, ver. 1 Application Note 78

Introduction

Altera devices provide performance that is consistent from simulation to application. Before programming a device, you can determine the worst-case timing delays for any design. You can calculate propagation delays either with the MAX+PLUS II Timing Analyzer or with the timing models given in this application note and the timing parameters listed in individual device data sheets. Both methods yield the same results.

This application note defines internal timing parameters, external timing parameters, and illustrates the timing models for the MAX 7000 (including MAX 7000E and MAX 7000S devices), MAX 5000, and Classic device families.

Familiarity with device architecture and characteristics is assumed. Refer to specific device or device family data sheets in this data book for complete descriptions of the architectures, and for the specific values of the timing parameters listed in this application note.

Internal Timing Parameters

Within a device, the timing delays contributed by individual architectural elements are called internal timing parameters, which cannot be measured explicitly. All internal timing parameters are shown in italic type. The following list defines the internal timing parameters for MAX 7000, MAX 5000, and Classic devices, and apply to all three device families unless otherwise indicated.

t_{IN} Input pad and buffer delay. In MAX 7000 devices, t_{IN} represents the time required for a dedicated input pin to drive the input signal into the programmable interconnect array (PIA) or into the global control array. In MAX 5000 and Classic devices, t_{IN} represents the time required for a dedicated input pin to drive the true and complement data input signal into the logic array(s).

t_{IO} I/O input pad and buffer delay. The t_{IO} delay applies to I/O pins used as inputs. In MAX 7000 and multi-LAB MAX 5000 devices, t_{IO} is the delay from the I/O pin to the PIA. In MAX 5000 devices with a single logic array block (LAB), t_{IO} is the delay from the I/O pin to the logic arrays. In Classic devices, t_{IO} is the delay added to t_{IN}.

t_{PIA} Programmable interconnect array (PIA) delay. The delay incurred by signals that require routing through the PIA. MAX 7000 and multi-LAB MAX 5000 devices only.

t_{SEXP} Shared expander array delay. The delay of a signal through the AND-NOT structure of the shared expander product-term array that is fed back into the logic array. MAX 7000 and MAX 5000 devices only.

t_{PEXP} Parallel expander delay. The additional delay incurred by adding parallel expander product terms to the macrocell product terms. For each group of up to five parallel expanders added to a single function, an additional t_{PEXP} delay is added to the timing path. MAX 7000 devices only.

t_{ICS} Global clock delay. The delay from the dedicated clock pin to a register's clock input. MAX 5000 and Classic devices only.

t_{GLOB} Global control delay. The delay from a dedicated input pin to any global control function in a macrocell or I/O control block. MAX 7000 devices only.

t_{IOE} Internally generated output enable delay. The delay from an internally generated signal on the PIA to the output enable of the tri-state buffer. MAX 7000E and MAX 7000S devices only.

t_{LAC} Logic array control delay. The AND array delay for register control functions such as preset, clear, and output enable. MAX 7000 and MAX 5000 devices only.

t_{IC} Array clock delay. The delay through a macrocell's clock product term to the register's clock input.

t_{EN} Register enable delay. The AND array delay from the PIA to the register enable input. MAX 7000 devices only.

t_{CLR} Register clear time. The delay from the assertion of the register's asynchronous clear input to the time the register output stabilizes at logical low.

t_{PRE} Register preset time. The delay from the assertion of the register's asynchronous preset input to the time the register output stabilizes at logical high.

t_{LAD} Logic array delay. The time a logic signal requires to propagate through a macrocell's AND-OR-XOR structure.

t_{RD} Register delay. The delay from the rising edge of the register's clock to the time the data appears at the register output. MAX 7000 and MAX 5000 devices only.

t_{SU} Register setup time. The time required for a signal to be stable at the register input before the register clock's rising edge to ensure that the register correctly stores the input data.

t_{H} Register hold time. The time required for a signal to be stable at the register input after the register clock's rising edge to ensure that the register correctly stores the input data.

t_{FSU} Fast-input register setup time. When the fast-input register is used, t_{FSU} is the time required for a signal to be stable at the register input before the register clock's rising edge to ensure that the register correctly stores the input data.

t_{FH} Fast-input register hold time. When the fast-input register is used, t_{FH} is the time required for a signal to be stable at the register input after the register clock's rising edge to ensure that the register correctly stores the input data.

t_{FIN} Fast input delay. The delay from the I/O pin to the macrocell register when fast input registers are used. MAX 7000E and MAX 7000S devices only.

t_{COMB} Combinatorial buffer delay. The delay from the time when a combinatorial logic signal bypasses the programmable register to the time it becomes available at the macrocell output. MAX 7000 and MAX 5000 devices only.

t_{LATCH} Latch delay. The propagation delay through the programmable register when t_{LATCH} is configured as a flow-through latch. MAX 5000 devices only.

t_{FD} Feedback delay. In single-LAB MAX 5000 devices, t_{FD} is the delay of a macrocell output fed back into the logic array. In multi-LAB MAX 5000 devices, t_{FD} is the delay of a macrocell output fed back into the LAB's logic array or to a PIA input. In Classic devices, t_{FD} is the delay of a macrocell output fed back into the logic array.

t_{OD} Output buffer and pad delay. MAX 5000 and Classic devices only.

t_{OD1} Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V. MAX 7000 devices only.

t_{OD2} Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3 V. MAX 7000 devices only.

t_{OD3} Output buffer and pad delay with the Slow Slew Rate logic option turned on. MAX 7000E and MAX 7000S devices only.

t_{XZ} Output buffer disable delay. The delay required for high impedance to appear at the output pin after the output buffer's enable control is disabled.

t_{ZX} Output buffer enable delay. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled. MAX 5000 and Classic devices only.

t_{ZX1} Output buffer enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled. MAX 7000 devices only.

t_{ZX2} Output buffer enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled. MAX 7000 devices only.

t_{ZX3} Output buffer enable delay with the Slow Slew Rate logic option turned on and V_{CCIO} = 5.0 V or 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled. MAX 7000E and MAX 7000S devices only.

t_{LPA} Low-power adder. The delay associated with macrocells in low-power operation. In low-power mode, t_{LPA} must be added to the logic array delay (t_{LAD}), the register control delay (t_{LAC}, t_{IC}, t_{ACL}, or t_{EN}), and the shared expander delay (t_{SEXP}) paths. MAX 7000 devices only.

External Timing Parameters

External timing parameters represent actual pin-to-pin timing characteristics. Each external timing parameter consists of a combination of internal timing parameters. The data sheet for each device gives the values of the external timing parameters. These external timing parameters are worst-case values, derived from extensive performance measurements and ensured by testing. All external timing parameters are shown in bold type. The following list defines external timing parameters for MAX 7000, MAX 5000, and Classic devices.

t_{PD1} Dedicated input pin to non-registered output delay. The time required for a signal on any dedicated input pin to propagate through the combinatorial logic in a macrocell and appear at an external device output pin.

t_{PD2} I/O pin input to non-registered output delay. The time required for a signal on any I/O pin input to propagate through the combinatorial logic in a macrocell and appear at an external device output pin.

t_{PZX} Tri-state to active output delay. The time required for an input transition to change an external output from a tri-state (high-impedance) logic level to a valid high or low logic level.

t_{PXZ} Active output to tri-state delay. The time required for an input transition to change an external output from a valid high or low logic level to a tri-state (high-impedance) logic level.

t_{CLR} Time to clear register delay. The time required for a low signal to appear at the external output, measured from the input transition.

t_{SU} Global clock setup time. The time that data must be present at the input pin before the global (synchronous) clock signal is asserted at the clock pin.

t_{H} Global clock hold time. The time that data must be present at the input pin after the global clock signal is asserted at the clock pin.

t_{FSU} Fast-input clock setup time. When the fast-input path is used, t_{FSU} is the time that data must be present at the input pin before the global (synchronous) clock signal is asserted at the clock pin.

t_{FH} Fast-input clock hold time. When the fast-input path is used, t_{FH} is the time that data must be present at the input pin after the global clock signal is asserted at the clock pin.

t_{CO1} Global clock to output delay. The time required to obtain a valid output after the global clock is asserted at the clock pin.

t_{CNT} Minimum global clock period. The minimum period maintained by a globally clocked counter.

t_{ASU} Array clock setup time. The time data must be present at an input pin before an array (asynchronous) clock signal is asserted at the input pin.

t_{AH} Array clock hold time. The time data must be present at an input pin after an array clock signal is asserted at the input pin.

t_{ACO1} Array clock to output delay. The time required to obtain a valid output after an array clock signal is asserted at an input pin.

t_{ACNT} Minimum array clock period. The minimum period maintained by a counter when it is clocked by a signal from the array.

Timing Models

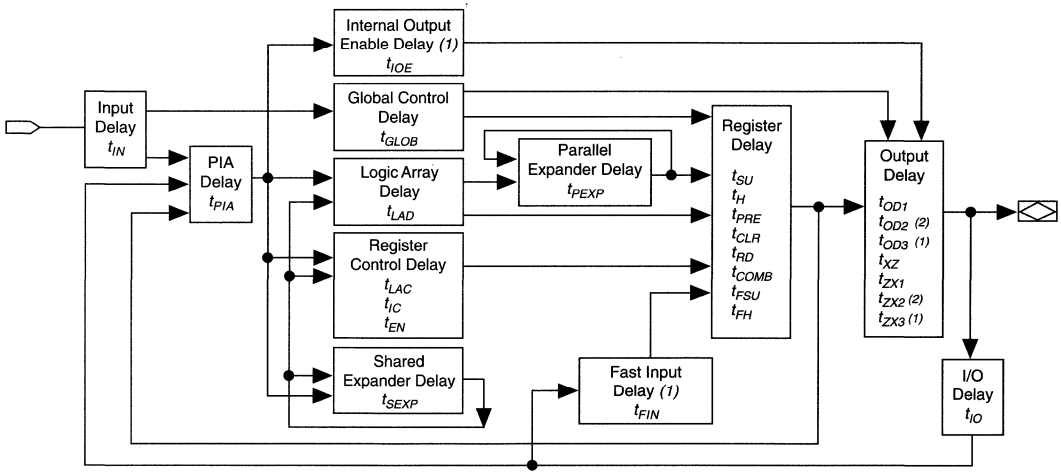
Timing models are simplified block diagrams that illustrate the propagation delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your design by examining the equations listed in the MAX+PLUS II Report File (**.rpt**) for the project. You can then add up the appropriate internal timing parameters to calculate the propagation delays through the device.

MAX 7000 Devices

MAX 7000 architecture has globally routed register clock, clear, and tri-state buffer output enable signals. Two types of expander product terms—shared and parallel—can be used to implement complex logic. Each macrocell can be set for low-power operation to reduce power dissipation in the device.

Figure 1 shows the timing model for MAX 7000 devices.

Figure 1. MAX 7000 Device Timing Model



Notes:
(1) This parameter is only available in MAX 7000E and MAX 7000S devices.
(2) This parameter is not available in 44-pin devices.

MAX 5000 Devices

The MAX 5000 architecture supports many functions. The macrocell array provides registered, combinatorial, or flow-through latch operation. The registers can be clocked from a global clock or through product-term array clocks, and can be asynchronously preset and cleared. Separate product terms control the output enable and logic inversion signals. The array of shared expander product terms provides additional product terms to implement complex logic.

MAX 5000 devices are divided into single- and multi-LAB devices. Figure 2 shows the timing model for the single-LAB MAX 5000 device, the EPM5032.

Figure 2. Single-LAB MAX 5000 Device Timing Model

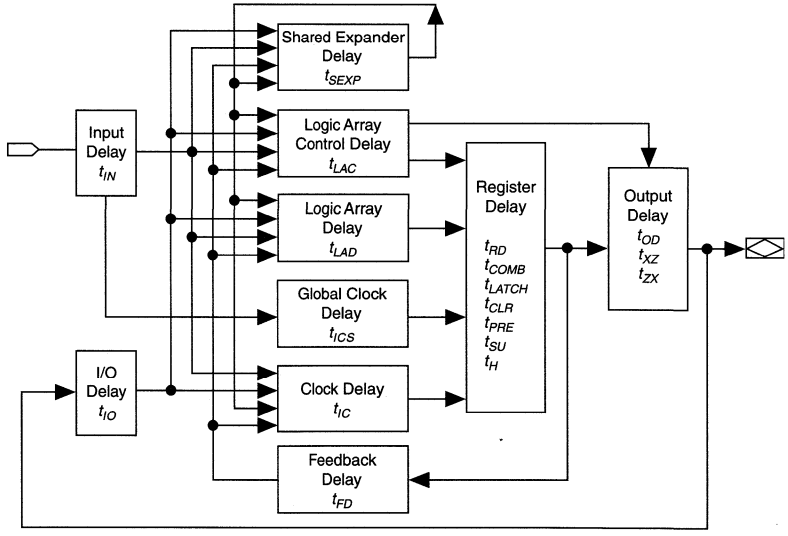
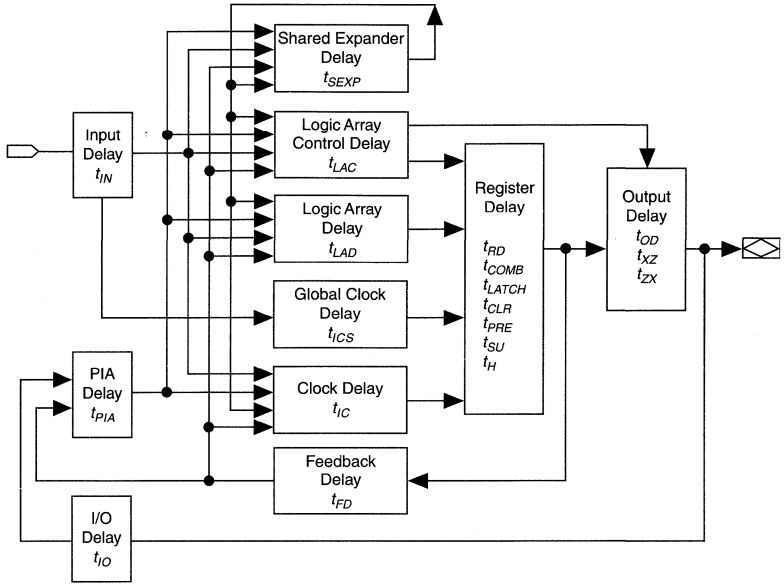


Figure 3 shows the timing model for the multi-LAB MAX 5000 devices: the EPM5064, EPM5128, EPM5130, and EPM5192 devices. In multi-LAB devices, the PIA routes signals between different LABs. All I/O inputs enter the logic array through the PIA. Signals routed through the PIA incur an additional delay.

Figure 3. Multi-LAB MAX 5000 Device Timing Model

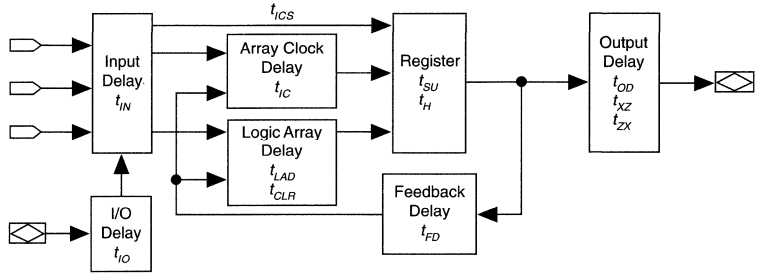


Classic Devices

The architecture of the EP610, EP610I, EP910, EP910I, and EP1810 devices provides registered and combinatorial capabilities. Registers can be clocked from a global clock or through a product-term array clock, and can be asynchronously cleared. When the global clock is used, the output enable signal can be controlled by a product term. Figure 4 shows the timing model for these Classic devices.

Figure 4. EP610, EP610I, EP910, EP910I & EP1810 Device Timing Model

If the register is bypassed, the delay between the logic array and the output buffer is zero.

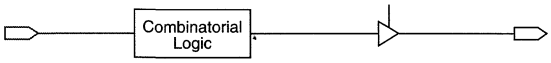


Calculating Timing Delays

You can calculate pin-to-pin timing delays for any device with the appropriate timing model and internal timing parameters. Each external timing parameter is calculated from a combination of internal timing parameters. Figure 5 shows the external timing parameters for the MAX 7000, MAX 5000, and Classic device families. To calculate the delay for a signal that follows a different path through the device, refer to the timing models shown in Figures 1 through 4 to determine which internal timing parameters to add together.

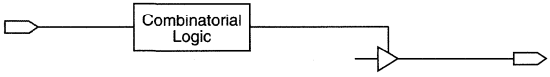
Figure 5. External Timing Parameters (Part 1 of 4)

Combinatorial Delay

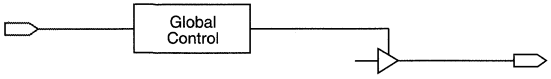


MAX 7000	$t_{PD1} = t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD1}$ $t_{PD2} = t_{IO} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD1}$
MAX 5000 (single-LAB)	$t_{PD1} = t_{IN} + t_{LAD} + t_{COMB} + t_{OD}$ $t_{PD2} = t_{IO} + t_{LAD} + t_{COMB} + t_{OD}$
MAX 5000 (multi-LAB)	$t_{PD1} = t_{IN} + t_{LAD} + t_{COMB} + t_{OD}$ $t_{PD2} = t_{IO} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD}$
EP610, EP610I, EP910, EP910I, EP1810	$t_{PD1} = t_{IN} + t_{LAD} + t_{OD}$ $t_{PD2} = t_{IO} + t_{IN} + t_{LAD} + t_{OD}$

Tri-State Enable/Disable Delay



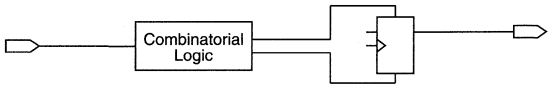
MAX 5000	$t_{PXZ}, t_{PZX} = t_{IN} + t_{LAC} + (t_{XZ} \text{ or } t_{ZX})$
EP610, EP610I, EP910, EP910I, EP1810	$t_{PXZ}, t_{PZX} = t_{IN} + t_{LAD} + (t_{XZ} \text{ or } t_{ZX})$



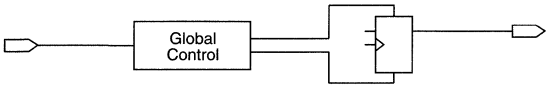
MAX 7000	$t_{PXZ}, t_{PZX} = t_{IN} + t_{GLOB} + (t_{XZ} \text{ or } t_{ZX1})$

Figure 5. External Timing Parameters (Part 2 of 4)

Register Clear & Preset Time

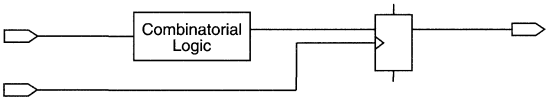


MAX 7000	$t_{PRE}, t_{CLR} = t_{IN} + t_{PIA} + t_{LAC} + (t_{PRE} \text{ or } t_{CLR}) + t_{OD1}$
MAX 5000	$t_{PRE}, t_{CLR} = t_{IN} + t_{LAC} + (t_{PRE} \text{ or } t_{CLR}) + t_{OD}$
EP610, EP610I, EP910, EP910I, EP1810	$t_{CLR} = t_{IN} + t_{CLR} + t_{OD}$



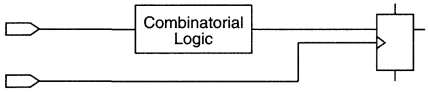
MAX 7000	$t_{GCLR} = t_{IN} + t_{GLOB} + t_{CLR} + t_{OD1}$

Setup Time



MAX 7000	$t_{SU} = (t_{IN} + t_{PIA} + t_{LAD}) - (t_{IN} + t_{GLOB}) + t_{SU}$
MAX 5000	$t_{SU} = (t_{IN} + t_{LAD}) - (t_{IN} + t_{ICS}) + t_{SU}$
EP610, EP610I, EP910, EP910I, EP1810	$t_{SU} = (t_{IN} + t_{LAD}) - (t_{IN} + t_{ICS}) + t_{SU}$

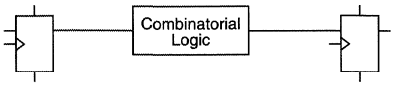
Hold Time



MAX 7000	$t_{H} = (t_{IN} + t_{GLOB}) - (t_{IN} + t_{PIA} + t_{LAD}) + t_{H}$
MAX 5000	$t_{H} = (t_{IN} + t_{ICS}) - (t_{IN} + t_{LAD}) + t_{H}$
EP610, EP610I, EP910, EP910I, EP1810	$t_{H} = (t_{IN} + t_{ICS}) - (t_{IN} + t_{LAD}) + t_{H}$

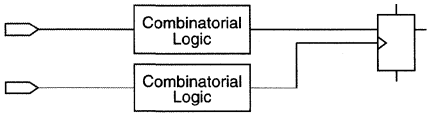
Figure 5. External Timing Parameters (Part 3 of 4)

Counter Frequency



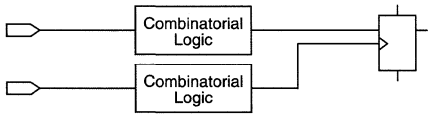
MAX 7000	$t_{CNT} = t_{RD} + t_{PIA} + t_{LAD} + t_{SU}$
MAX 5000	$t_{CNT} = t_{RD} + t_{FD} + t_{LAD} + t_{SU}$
EP610, EP610I, EP910, EP910I, EP1810	$t_{CNT} = t_{FD} + t_{LAD} + t_{SU}$

Asynchronous Setup Time



MAX 7000	$t_{ASU} = (t_{IN} + t_{PIA} + t_{LAD}) - (t_{IN} + t_{PIA} + t_{IC}) + t_{SU}$
MAX 5000	$t_{ASU} = (t_{IN} + t_{LAD}) - (t_{IN} + t_{IC}) + t_{SU}$
EP610, EP610I, EP910, EP910I, EP1810	$t_{ASU} = (t_{IN} + t_{LAD}) - (t_{IN} + t_{IC}) + t_{SU}$

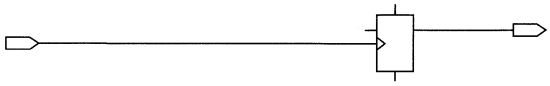
Asynchronous Hold Time



MAX 7000	$t_{AH} = (t_{IN} + t_{PIA} + t_{IC}) - (t_{IN} + t_{PIA} + t_{LAD}) + t_{H}$
MAX 5000	$t_{AH} = (t_{IN} + t_{IC}) - (t_{IN} + t_{LAD}) + t_{H}$
EP610, EP610I, EP910, EP910I, EP1810	$t_{AH} = (t_{IN} + t_{IC}) - (t_{IN} + t_{LAD}) + t_{H}$

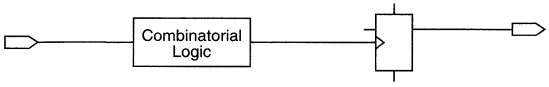
Figure 5. External Timing Parameters (Part 4 of 4)

Clock-to-Output Delay



MAX 7000	$t_{CO1} = t_{IN} + t_{GLOB} + t_{RD} + t_{OD1}$
MAX 5000	$t_{CO1} = t_{IN} + t_{ICS} + t_{RD} + t_{OD}$
EP610, EP610I, EP910, EP910I, EP1810	$t_{CO1} = t_{IN} + t_{ICS} + t_{OD}$

Array Clock-to-Output Delay



MAX 7000	$t_{ACO1} = t_{IN} + t_{PIA} + t_{IC} + t_{RD} + t_{OD1}$
MAX 5000	$t_{ACO1} = t_{IN} + t_{IC} + t_{RD} + t_{OD}$
EP610, EP610I, EP910, EP910I, EP1810	$t_{ACO1} = t_{IN} + t_{IC} + t_{OD}$

Examples

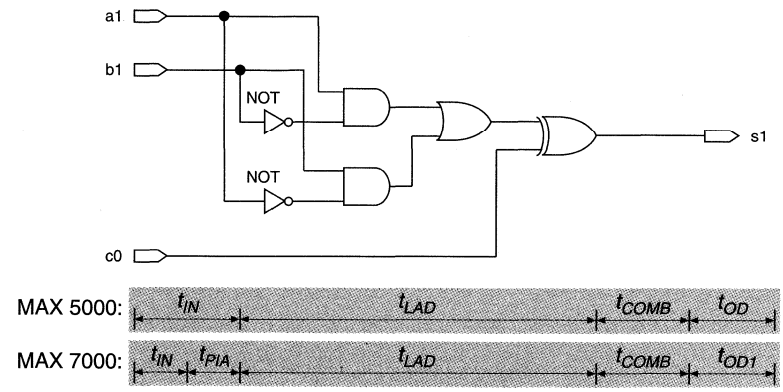
The following examples show how to use internal timing parameters to calculate the delays for real applications.

Example 1: First Bit of 7483 TTL Macrofunction

You can analyze the timing delays for macrofunctions that have been subjected to minimization and logic synthesis. A MAX+PLUS II Report File (**.rpt**) that includes the optional Equations Section lists the synthesized logic equations for the project. These equations are structured so you can quickly determine the logic implementation of any signal. For example, Figure 6 shows part of a 7483 TTL macrofunction (a 4-bit full adder). The Report File gives the following equations for s1, the least significant bit of the adder:

```
s1      = OUTPUT ( _LC021 , VCC );
LC021   = LCELL  ( _EQ026 $ C0  );
_EQ026  = b1 & !a1
        # !b1 &  a1;
```

Figure 6. Adder Logic Timing for MAX 7000 & MAX 5000 Architectures



The s1 output is the output of macrocell 21 (_LC021), which contains combinatorial logic. The combinatorial logic LCELL(_EQ026 $ C0) represents the XOR of the intermediate equation _EQ026 and the carry-in, c0. In turn, _EQ026 is logically equivalent to the XOR of inputs b1 and a1. Therefore, the timing delay for s1 in MAX 7000 devices is as follows:

$t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD1}$

The timing delay for s1 in MAX 5000 devices is as follows:

$t_{IN} + t_{LAD} + t_{COMB} + t_{OD}$

Example 2: Second Bit of 7483 TTL Macrofunction

For complex logic that requires expanders (represented as _X<*number*> in Report Files), the expander array delay, t_{SEXP}, is added to the delay element. The second bit of the 7483 adder macrofunction, s2, requires shared expanders. The equations are as follows:

```
s2      =  _LC019;
_LC019  =  LCELL( _EQ023  $  _EQ024 );
_EQ023  =  _X029  &  _X030  &  _X031;
_X029   =  EXP( !b1  &  !a1 );
_X030   =  EXP( !b1  &  !c0 );
_X031   =  EXP( !a1  &  !c0 );
_EQ024  =  _X032  &  _X033;
_X032   =  EXP( !b2  &   a2  );
_X033   =  EXP(  b2  &   a2  );
```

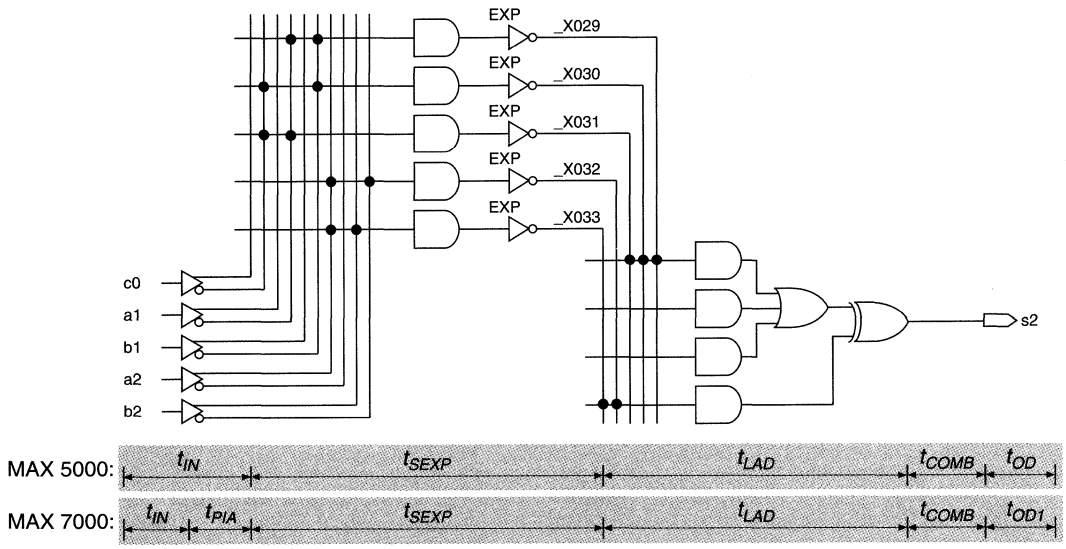
Figure 7 shows how you can map the logic structure onto the MAX 7000 and MAX 5000 architectures with these equations. Therefore, the timing delay for s2 in MAX 7000 devices is as follows:

$$t_{IN} + t_{PIA} + t_{SEXP} + t_{LAD} + t_{COMB} + t_{OD1}$$

The timing delay for s2 in MAX 5000 devices is as follows:

$$t_{IN} + t_{SEXP} + t_{LAD} + t_{COMB} + t_{OD}$$

Figure 7. Adder Equations Mapped to MAX 7000 & MAX 5000 Architectures



Example 3: Second Bit of 7483 TTL Macrofunction with Parallel Expanders (MAX 7000 Devices)

The Compiler implements logic with parallel expanders if the Parallel Expanders logic option is turned on when a project is compiled for MAX 7000 devices. When parallel expanders are used, no shareable expanders are used, so the timing delay for the s2 bit of the 7483 becomes:

$$t_{IN} + t_{PIA} + t_{LAD} + t_{PEXP} + t_{COMB} + t_{OD1}$$

Example 4: First Bit of 7483 TTL Macrofunction in Low-Power Mode (MAX 7000 Devices)

If a macrocell in a MAX 7000 device is set for low-power mode, then you must add the low-power adder delay to the total delay through that macrocell. Thus, the s1 delay in Figure 6 becomes:

$$t_{IN} + t_{PIA} + t_{LPA} + t_{LAD} + t_{COMB} + t_{OD1}$$

Conclusion

The MAX 7000, MAX 5000, and Classic device architectures have fixed internal timing delays that are independent of routing. Therefore, you can determine the worst-case timing delays for any design before programming a device. Total delay paths can be expressed as the sums of internal timing delays. Timing models illustrate the internal delay paths for devices and show how these internal timing parameters affect each other. You can use the MAX+PLUS II Timing Analyzer to automatically calculate delay paths, or hand-calculate delay paths by adding the internal timing parameters for an appropriate timing model. With the ability to predict worst-case timing delays, you can be confident of a design's in-system timing performance.

Notes:

Understanding FLASHlogic Timing

June 1996, ver. 1 Application Note 79

Introduction

Altera devices provide device performance that is consistent from simulation to application. Before programming or configuring a device, you can determine the worst-case timing delays for any design. You can calculate propagation delays with the timing models given in this application note and the timing parameters listed in the *FLASHlogic Programmable Logic Device Family Data Sheet* in this data book.

This application note defines internal and external timing parameters, and illustrates the timing model for the FLASHlogic device family.

Familiarity with FLASHlogic device architecture and characteristics is assumed. Refer to the *FLASHlogic Programmable Logic Device Family Data Sheet* for a complete description of the FLASHlogic device architecture, and for specific values of the timing parameters listed in this application note.

Internal Timing Parameters

The timing delays contributed by individual FLASHlogic architectural elements are called internal timing parameters, which cannot be measured explicitly. All internal timing parameters are shown in italic type. Each FLASHlogic logic array block (LAB) has two modes of operation: logic (24V10) mode and SRAM mode, and the internal timing parameters for each mode are provided in this section.

Logic (24V10) Mode

The following list defines the internal timing parameters for FLASHlogic devices in logic (24V10) mode.

t_{IN} Input pad and buffer delay. The time required for a dedicated input and clock pin to drive the input signal into the programmable interconnect array (PIA) and the global clock delay.

t_{IO} I/O input pad and buffer delay. The delay from the I/O pin to the PIA when the I/O pin is used as an input.

t_{PIA} Programmable interconnect array (PIA) delay. The delay incurred by signals that are routed through the PIA.

t_{GLOB} Global clock delay. The delay from the dedicated clock pin to a register's clock input.

t_{DGLOB} Delayed global clock delay. The delay from the dedicated clock pin to a register's clock input through the delayed global clock path.

t_{LAC} Logic array control delay. The AND array delay for register control functions such as preset, clear, and output enable.

t_{SOE} SRAM output enable control delay. The delay that activates the output enable control when the LAB is used as SRAM.

t_{ICOMP} Identity comparator delay. The delay for a signal that propagates through the identity comparator in an LAB.

t_{IC} Array clock delay. The delay through a macrocell's clock product term to the register's clock input.

t_{CLR} Register clear time. The delay from the assertion of the register's array clear input to the time the register output stabilizes at logical low.

t_{PRE} Register preset time. The delay from the assertion of the register's array preset input to the time the register output stabilizes at logical high.

t_{LAD} Logic array delay. The time required for a logic signal to propagate through a macrocell's AND-OR-XOR structure.

t_{RD} Register delay. The delay from the rising edge of the register's clock to the time the data appears at the register output.

t_{ISU} Register setup time. The time required for a signal to stabilize at the register input before the clock's rising edge to ensure that the register correctly stores the input data.

t_{IH} Register hold time. The time required for a signal to remain stable at the register input after the clock's rising edge to ensure that the register correctly stores the input data.

t_{IASU} Internal array setup time. The time required for a signal to stabilize at the register input before the clock's rising edge to ensure that the register correctly stores the input data.

t_{IAH} Internal array hold time. The time required for a signal to remain stable at the register input after the clock's rising edge to ensure that the register correctly stores the input data.

t_{COMB} Combinatorial buffer delay. The delay from the time a combinatorial logic signal bypasses the programmable register to the time it becomes available at the macrocell output.

t_{FD} Feedback delay. The delay of the macrocell output fed back into the PIA input.

t_{OD} Output buffer and pad delay. In FLASHlogic devices, the value of V_{CCIO} for 5.0-V or 3.3-V devices are the same.

t_{XZ} Output buffer disable delay. The delay required for high impedance to appear at the output pins after the output buffer's enable control is disabled.

t_{ZX} Output buffer enable delay. The delay required for the output signal to appear at the output pins after the tri-state buffer's enable control is enabled.

SRAM Mode

The following list defines the internal timing parameters for FLASHlogic devices in SRAM mode.

t_{IDD} Internal data-in to data-out delay. The data delay at the SRAM output when the SRAM is in read cycle after a write cycle, i.e., the delay from the time data is written into the SRAM to the time it appears at the SRAM output.

t_{AA} SRAM address access delay. The delay from an address change at the SRAM input to the time data appears at the SRAM output.

t_{WASU} Write address setup. The time required for the address signal to stabilize at the SRAM input before the beginning of the write pulse.

t_{WAH} Write address hold. The time between the end of the write pulse to when the address lines are allowed to change.

t_{WDSU} Write data setup. The time required for the data signals to stabilize at the SRAM input before the end of the write pulse.

t_{WDH} Write data hold. The time between the end of the write pulse to when the data lines are allowed to change.

t_{SISU} SRAM internal register setup. The time required for the SRAM output to stabilize at the register input before the register clock's rising edge to ensure that the register correctly stores the input data.

t_{SIH} SRAM internal register hold. The time required for the SRAM output to remain stable at the register input after the register clock's rising edge to ensure that the register correctly stores the input data.

t_{WP} SRAM write pulse width. The time during which both the block enable (BE) signal and the write enable (WE) signal are asserted.

External Timing Parameters

External timing parameters represent actual pin-to-pin timing characteristics. Each external timing parameter consists of a combination of internal timing parameters. The *FLASHlogic Programmable Logic Device Family Data Sheet* gives the values of the external timing parameters. These external timing parameters are worst-case values, derived from extensive performance measurements and ensured by device testing. All external timing parameters are shown in bold type.

Logic (24V10) Mode

The following list defines the external timing parameters for a FLASHlogic LAB in logic (24V10) mode.

t_{PD1} Dedicated input pin to non-registered output delay. The time required for a signal on any dedicated input pin to propagate through the combinatorial logic in a macrocell and appear at an external device output pin.

t_{PD2} I/O pin input to non-registered output delay. The time required for a signal on any I/O pin input to propagate through the combinatorial logic in a macrocell and appear at an external device output pin.

t_{COMP} Dedicated input pin or I/O pin input to non-registered output delay. The time required for a signal on any dedicated input pin or I/O pin input to propagate through the identity comparator in an LAB and appear at an external device output pin.

t_{PZX} Tri-state to active output delay. The time required for an input transition to change an external output from a tri-state (high-impedance) logic level to a valid high or low logic level.

t_{PXZ} Active output to tri-state delay. The time required for an input transition to change an external output from a valid high or low logic level to a tri-state (high-impedance) logic level.

t_{CLR} Time to clear register delay. The time required for a low signal to appear at the external output, measured from the input transition.

t_{SU} Global clock setup time. The time data must be present at the input pin before the global clock signal is asserted at the clock pin.

t_{H} Global clock hold time. The time the data must be present at the input pin after the global clock signal is asserted at the clock pin.

t_{DSU} Delayed global setup time. The time data must be present at the input pin before the delayed global clock signal is asserted at the clock pin.

t_{DH} Delayed global hold time. The time the data must be present at the input pin after the delayed global clock signal is asserted at the clock pin.

t_{CO1} Global clock to output delay. The time required to obtain a valid output after the global clock is asserted at the clock pin.

t_{DCO1} Delayed global clock to output delay. The time required to obtain a valid output after the global clock is asserted at the clock pin.

t_{CNT} Minimum global clock period. The minimum period maintained by a globally clocked counter.

t_{ASU} Array clock setup time. The time when data must be present at the input pin before an array clock signal is asserted at an input pin.

t_{AH} Array clock hold time. The time when data must be present at the input pin after an array clock signal is asserted at an input pin.

t_{ACO1} Array clock to output delay. The time required to obtain a valid output after an array clock signal is asserted at an input pin.

t_{ACNT} Minimum array clock period. The minimum period maintained by a counter that is clocked by a signal from the array.

SRAM Mode

The following list defines the external timing parameters for the read and write cycles of a FLASHlogic LAB in SRAM mode.

SRAM Read Cycle Timing Parameters

t_{RC} Read cycle time. The time required for the address lines to remain stable during a read operation.

t_{DD} Data-in to data-out delay. The time required for the written data to appear at the output pins.

t_{AA} Address access time. The delay from an address change at the input pins to the time data appears at the external device output pins. This parameter is valid only when the block enable (BE) and output enable (OE) signals are asserted.

t_{ABE} Block enable access time. The delay from the time BE is asserted to the time data appears at the output pins. This parameter is valid only when OE is asserted.

t_{OE} Output enable to output valid. The time required for an input transition to change an external output from a tri-state (high-impedance) logic level to a valid high or low logic level.

t_{OH} Output hold from address change. The minimum delay from an address change at the input pins to the time data appears at the external device output pins.

t_{BLZ} Block enable to output in low impedance. The minimum delay from the time BE is asserted to the time the output pins are driven.

t_{BHZ} Block disable to output in high impedance. The delay from the time the BE is de-asserted to the time the SRAM outputs are tri-stated.

t_{OLZ} Output enable to output in low impedance. The minimum delay from the time the OE is asserted to the time the output pins are driven.

t_{SSU} SRAM global clock setup time. The time when the address must be present at the input pins before the global clock signal is asserted at the clock pin.

t_{SH} SRAM global clock hold time. The time when the address must be present at the input pins after the global clock signal is asserted at the clock pin.

t_{SDSU} SRAM delayed global clock setup time. The time when the address must be present at the input pins before the delayed global clock signal is asserted at the clock pin.

t_{SDH} SRAM delayed global clock hold time. The time when the address must be present at the input pins after the delayed global clock signal is asserted at the clock pin.

SRAM Write Cycle Timing Parameters

t_{WC} Write cycle time. The time when the address signals must remain constant.

t_{BW} Block enable to end of write. The time during which both the WE and BE signals are asserted. The WE signal is asserted before the BE signal.

t_{AW} Address valid to end of write. The setup time required for the address lines to stabilize before the end of the write pulse.

t_{AS} Address setup time. The time when the address lines must have stabilized before the beginning of the write pulse.

t_{WP} Write pulse width. The minimum time when both the BE and WE signals are asserted. The BE signal is asserted before the WE signal.

t_{WR} Write recovery time. The time after the end of the write pulse during which the address lines to must remain stable.

t_{DW} Data valid to end of write. The setup time required for the data lines to stabilize before the end of the write pulse.

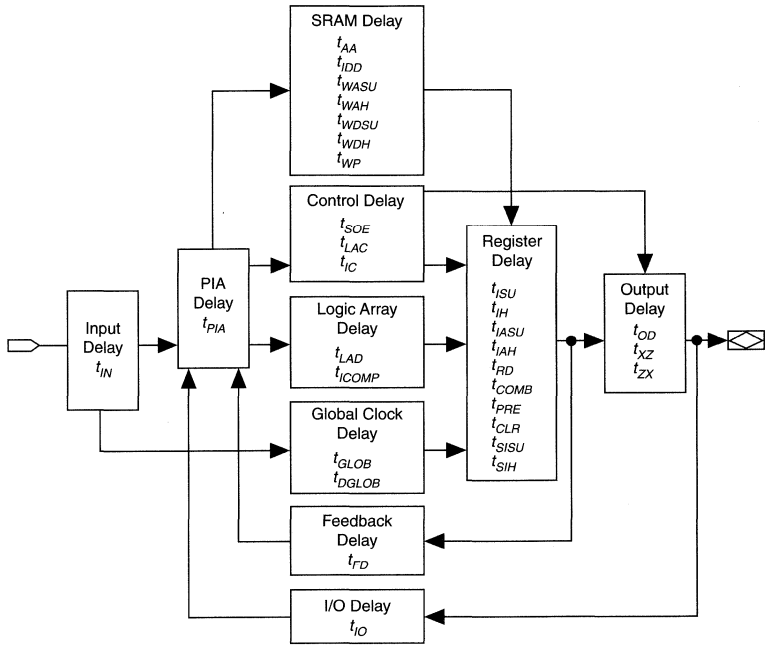
t_{DH} Data hold time. The time required for the data lines to stabilize after the end of the write pulse.

t_{OHZ} Output disable to valid data-in. The delay from the time OE is de-asserted to the end of valid data output.

Timing Models

Timing models are simplified block diagrams that illustrate the propagation delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your FLASHlogic device by examining the equations listed in the PLDshell Plus Report File (**.rpt**) for the project. You can then add up the appropriate internal timing parameters to calculate the propagation delays through the device. Figure 1 shows the timing model for FLASHlogic devices.

Figure 1. FLASHlogic Timing Model



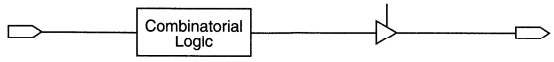
Calculating Timing Delays

You can calculate approximate pin-to-pin timing delays for any FLASHlogic device with the timing model shown in Figure 1 and the internal timing parameters in the *FLASHlogic Programmable Logic Device Family Data Sheet* in this data book. Each external timing parameter is calculated from a combination of internal timing parameters. Figure 2 shows the external timing parameters for FLASHlogic devices. To calculate the delay for a signal that follows a different path through the device, refer to the timing model shown in Figure 1 to determine which internal timing parameters to add together.

Figure 2. External Timing Parameters (Part 1 of 3)

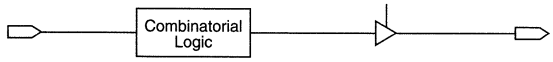
When an input pin is used instead of an I/O pin, t_{IN} can be substituted for t_{IO}.

Combinatorial Delay



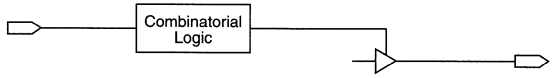
$$t_{PD1} = t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD}$$
$$t_{PD2} = t_{IO} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD}$$

Comparator Delay



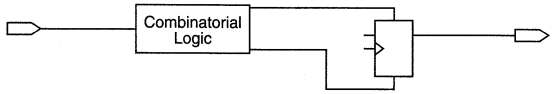
$$t_{COMP} = t_{IO} + t_{PIA} + t_{ICOMP} + t_{COMB} + t_{OD}$$

Tri-State Enable/Disable Delay



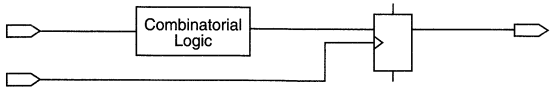
$$t_{PXZ} = t_{IO} + t_{PIA} + t_{LAC} + t_{XZ}$$
$$t_{PZX} = t_{IO} + t_{PIA} + t_{LAC} + t_{ZX}$$

Register Clear & Preset Time



$$t_{PRE} = t_{IO} + t_{PIA} + t_{LAC} + t_{PRE} + t_{OD}$$
$$t_{CLR} = t_{IO} + t_{PIA} + t_{LAC} + t_{CLR} + t_{OD}$$

Setup Time

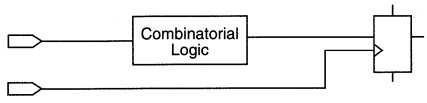


Global Clock $t_{SU} = (t_{IO} + t_{PIA} + t_{LAD}) - (t_{IN} + t_{GLOB}) + t_{ISU}$

Delayed Global Clock $t_{DSU} = (t_{IO} + t_{PIA} + t_{LAD}) - (t_{IN} + t_{DGLOB}) + t_{ISU}$

Figure 2. External Timing Parameters (Part 2 of 3)

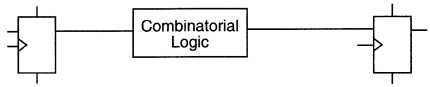
Hold Time



Global Clock $t_H = (t_{IN} + t_{GLOB}) - (t_{IO} + t_{PIA} + t_{LAD}) + t_{IH}$

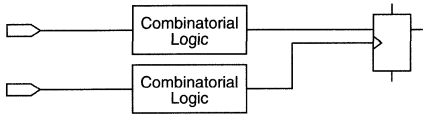
Delayed Global Clock $t_{DH} = (t_{IN} + t_{DGLOB}) - (t_{IO} + t_{PIA} + t_{LAD}) + t_{IH}$

Counter Frequency



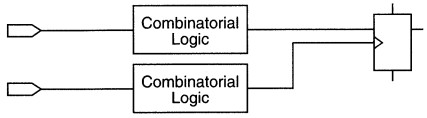
$t_{CNT} = t_{RD} + t_{FD} + t_{PIA} + t_{LAD} + t_{ISU}$

Array Clock Setup Time



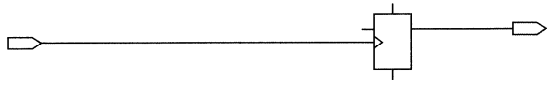
$t_{ASU} = (t_{IO} + t_{PIA} + t_{LAD}) - (t_{IO} + t_{PIA} + t_{IC}) + t_{IASU}$

Array Clock Hold Time



$t_{AH} = (t_{IO} + t_{PIA} + t_{IC}) - (t_{IO} + t_{PIA} + t_{LAD}) + t_{IAH}$

Clock-to-Output Delay

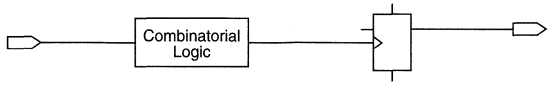


Global Clock $t_{CO1} = t_{IN} + t_{GLOB} + t_{RD} + t_{OD}$

Delayed Global Clock $t_{DCO1} = t_{IN} + t_{DGLOB} + t_{RD} + t_{OD}$

Figure 2. External Timing Parameters (Part 3 of 3)

Array Clock-to-Output Delay



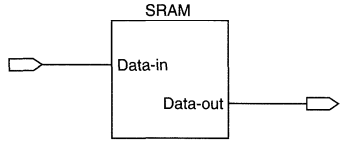
$t_{ACO1} = t_{IO} + t_{PIA} + t_{IC} + t_{RD} + t_{OD}$

Figure 3 illustrates the SRAM read cycle external timing parameters.

Figure 3. SRAM Read Cycle External Timing Parameters (Part 1 of 3)

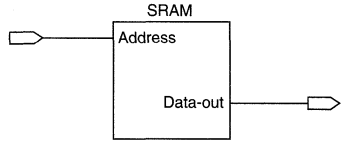
When an input pin is used instead of an I/O pin, t_{IN} can be substituted for t_{IO}.

Data to Output



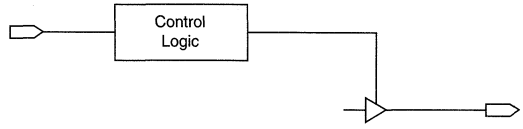
$t_{DD} = t_{IO} + t_{PIA} + t_{IDD} + t_{COMB} + t_{OD}$

Address Access Time



$t_{AA} = t_{IO} + t_{PIA} + t_{AA} + t_{COMB} + t_{OD}$

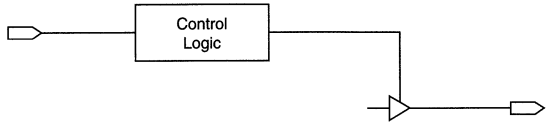
Block Enable Access



$t_{ABE} = t_{IO} + t_{PIA} + t_{SOE} + t_{ZX}$

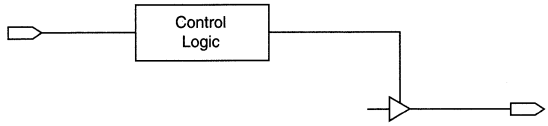
Figure 3. SRAM Read Cycle External Timing Parameters (Part 2 of 3)

Output Enable to Output Valid



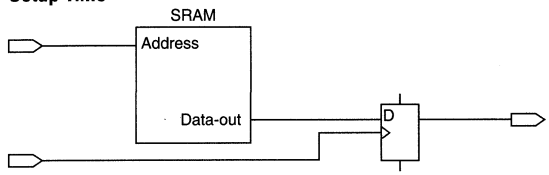
$t_{OE} = t_{IO} + t_{PIA} + t_{SOE} + t_{ZX}$

Block Disable to Output in High Impedance



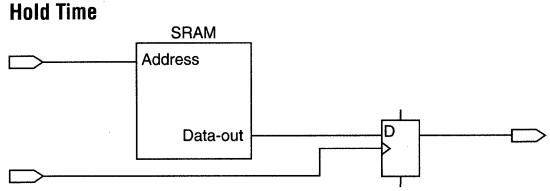
$t_{BHZ} = t_{IO} + t_{PIA} + t_{SOE} + t_{XZ}$

Setup Time



$t_{SSU} = (t_{IO} + t_{PIA} + t_{AA}) - (t_{IN} + t_{GLOB}) + t_{SISU}$

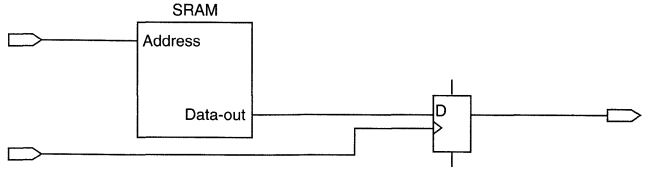
Hold Time



$t_{SH} = (t_{IN} + t_{GLOB}) - (t_{IO} + t_{PIA} + t_{AA}) + t_{SIH}$

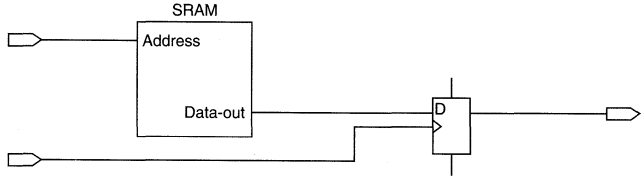
Figure 3. SRAM Read Cycle External Timing Parameters (Part 3 of 3)

Delay Setup Time



$$t_{SDSU} = (t_{IO} + t_{PIA} + t_{AA}) - (t_{IN} + t_{DGLOB}) + t_{SISU}$$

Delay Hold Time



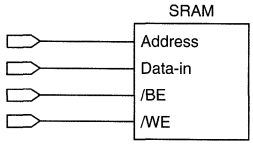
$$t_{SDH} = (t_{IN} + t_{DGLOB}) - (t_{IO} + t_{PIA} + t_{AA}) + t_{SIH}$$

Figure 4 shows the SRAM write cycle external timing parameters.

Figure 4. SRAM Write Cycle External Timing Parameters (Part 1 of 2)

When an input pin is used instead of an I/O pin, t_{IN} can be substituted for t_{IO}.

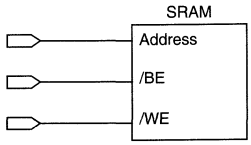
Write Cycle



$$t_{WC} = \text{maximum of } (t_{WASU} + t_{WP} + t_{WAH}) \text{ or } (t_{WDSU} + t_{WDH})$$

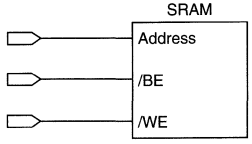
Figure 4. SRAM Write Cycle External Timing Parameters (Part 2 of 2)

Address Valid to End of Write



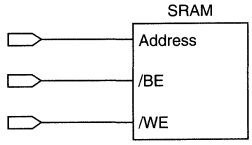
$$t_{AW} = (t_{IO} + t_{PIA}) - (t_{IO} + t_{PIA}) + t_{WASU} + t_{WP}$$

Address Setup Time



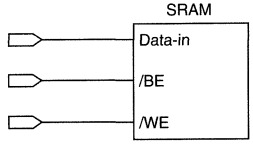
$$t_{AS} = (t_{IO} + t_{PIA}) - (t_{IO} + t_{PIA}) + t_{WASU}$$

Write Recovery Time



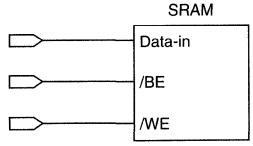
$$t_{WR} = (t_{IO} + t_{PIA}) - (t_{IO} + t_{PIA}) + t_{WAH}$$

Data Valid to End of Write



$$t_{DW} = (t_{IO} + t_{PIA}) - (t_{IO} + t_{PIA}) + t_{WDSU}$$

Data Hold Time



$$t_{DH} = (t_{IO} + t_{PIA}) - (t_{IO} + t_{PIA}) + t_{WDH}$$

Examples

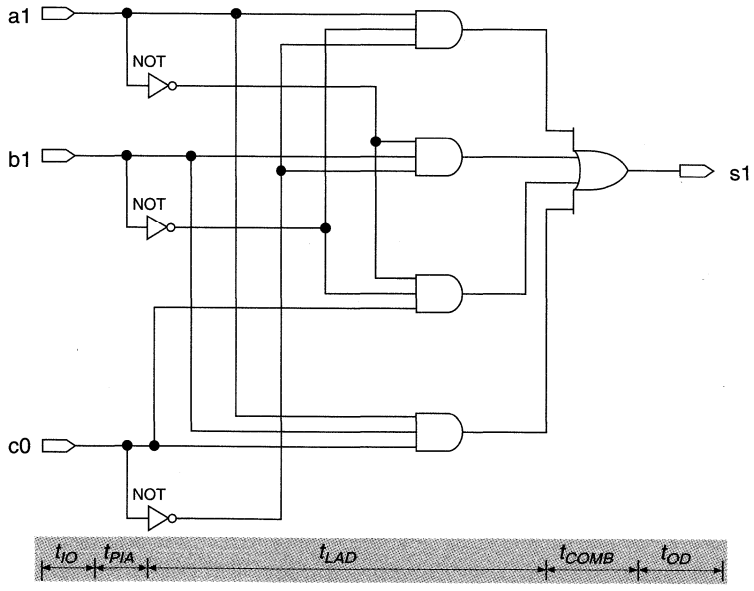
The following examples show how to use internal timing parameters to calculate the delays for real applications.

Example 1: First Bit of 7483 TTL Macrofunction

You can analyze the timing delays for macrofunctions that have been subject to minimization and logic synthesis. The PLDshell Plus Report File (**.rpt**) lists the synthesized logic equations. These equations are structured so that you can quickly determine the logic implementation of any signal. For example, Figure 5 shows part of a 7483 TTL macrofunction (a 4-bit full adder). The PLDshell Report File gives the following equations for s1, the least significant bit of the adder:

```
s1 =  a1 * /b1 * /c0
   + /a1 *  b1 * /c0
   + /a1 * /b1 *  c0
   + /b1 * /a1 *  c0
s1.trst = VCC
```

Figure 5. Adder Logic Timing for FLASHlogic Architecture



The output of the macrocell is s1. To drive the s1 output, the four products terms are ORed together:

(a1 * /b1 * /c0), (/a1 * b1 * /c0), (/a1 * /b1 * c0), and (b1 * a1 * c0).

Because a macrocell can have four or more product terms, the s1 output can be generated in one macrocell. Therefore, the timing delay is as follows:

$t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD}$

Example 2: Second Bit of 7483 TTL Macrofunction

For complex logic that requires additional product terms, product terms from neighboring macrocells can be used. The second bit of the 7483 adder macrofunction, s2, was generated using a macrocell that had only 4 product terms. Because 6 product terms are required to generate this function, 2 product terms were borrowed from a neighboring macrocell. The equations are as follows:

```
s2 =  b1 *  a1 *  a2
   +  b1 *  c0 *  a2
   +  a1 *  c0 *  a2
   + /b1 * /a1 * /a2
   + /b1 * /c0 * /a2
   + /a1 * /c0 * /a2
s2.trst = VCC
```

Product terms borrowed from neighboring macrocells do not have additional delays associated with them. As a result, the timing delay for s2 has the same delay as s1:

$t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD}$

Example 3: 5-Bit Comparator

FLASHlogic devices have a dedicated 12-bit identity comparator in each LAB. This comparator has the same delay regardless of the width of the data bits, i.e., a 1-bit comparator has the same delay as a 12-bit comparator. The following example is a 5-bit comparator between the I/O pins for busa and busb. The result is sent to the output pin equal. The equations are as follows:

```
equal = GND
equal.cmp = [busa4, busa3, busa2, busa1, busa0] == [busb4,
busb3, busb2, busb1, busb0]
equal.trst = VCC
```

Therefore, the timing delay for equal is as follows:

$t_{IN} + t_{PIA} + t_{ICOMP} + t_{COMB} + t_{OD}$

Conclusion

The FLASHlogic device architecture has fixed internal timing delays that are independent of routing. Therefore, you can determine the worst-case timing delays for any design before programming a device. Total delay paths can be expressed as the sums of internal timing delays. The FLASHlogic timing model illustrates the internal delay paths for FLASHlogic devices and shows how these internal timing parameters affect each other. You can calculate delay paths by adding the internal timing parameters in the FLASHlogic timing model. With the ability to predict worst-case timing delays, you can be confident of a design's in-system timing performance.

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Programmable Logic Development System & Software

June 1996, ver. 7 Data Sheet

Introduction

Ideally, a programmable logic design environment satisfies a large variety of design requirements: it should support devices with different architectures, run on multiple platforms, provide an easy-to-use interface, and offer a broad range of features. Moreover, a design environment should give designers the freedom to use the design entry methods and tools of their choice. The Altera MAX+PLUS II development system is a fully integrated programmable logic design environment that meets all of these requirements.

The MAX+PLUS II design environment offers unmatched flexibility and performance. The rich graphical user interface is complemented by complete and instantly accessible on-line documentation, which makes learning and using MAX+PLUS II quick and easy.

MAX+PLUS II includes the following features:

- *Open Interfaces*—Altera works closely with EDA manufacturers to link MAX+PLUS II with other industry-standard design entry, synthesis, and verification tools. The interfaces to EDA tools comply with EDIF 2 0 0 and 3 0 0, library of parameterized modules (LPM), SDF, VITAL, Verilog HDL, VHDL, and other standards. The MAX+PLUS II interfaces allow users to create a logic design with Altera or standard EDA design entry tools, compile the design for an Altera device with the MAX+PLUS II Compiler, and perform device- or board-level simulation with Altera or other EDA verification tools. MAX+PLUS II currently has interfaces to tools from Cadence, Data I/O, Exemplar, Mentor Graphics, MINC, OrCAD, Synopsys, VeriBest, Viewlogic, and others.

- *Architecture-Independence*—MAX+PLUS II supports Altera's FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic programmable logic device families, and offers the industry's only truly architecture-independent programmable logic design environment. The MAX+PLUS II Compiler also provides powerful logic synthesis and minimization to efficiently fit designs with minimal user effort.

- *Multiple Platforms*—MAX+PLUS II runs under Microsoft Windows, Windows for Workgroups, Windows 95, or Windows NT on 486- or Pentium-based PCs, and under X Windows on Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

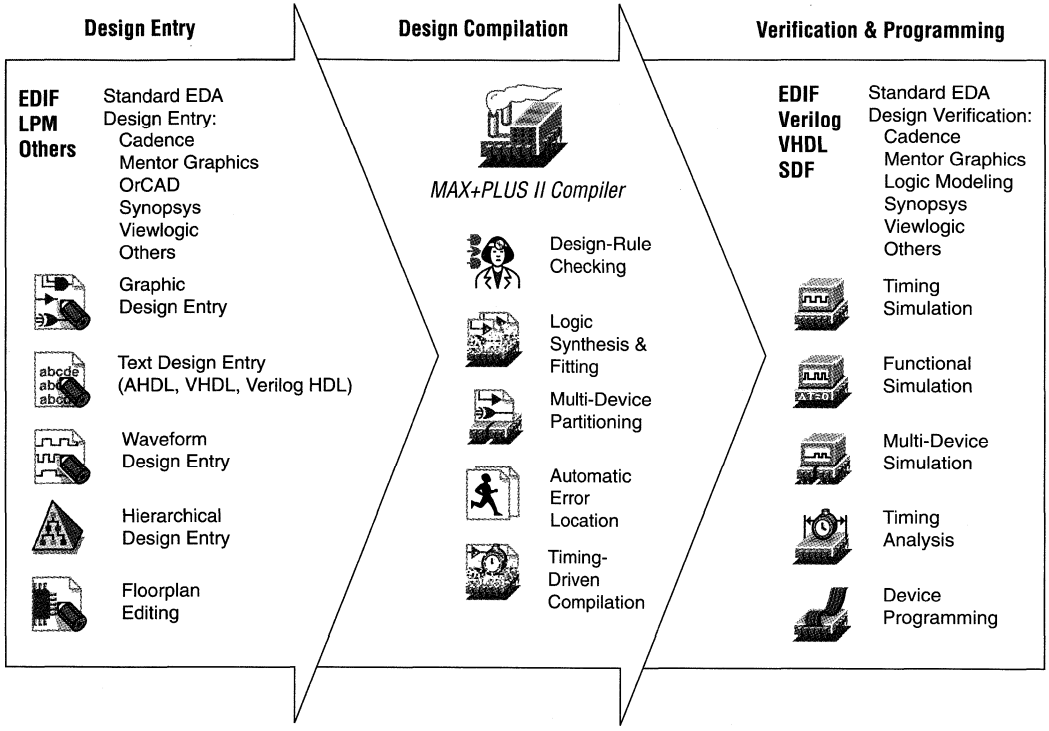
- *Full Integration*—Together, MAX+PLUS II design entry, processing, and verification features offer the most fully integrated suite of programmable logic development tools available, allowing faster debugging and shorter development cycles.

- *Modular Tools*—Designers can customize their development environment by choosing from a variety of design entry, compilation, verification, and device programming options, all of which are described in this data sheet. Additional features can be added as needed, preserving the initial tools investment. Because MAX+PLUS II supports multiple device families, designers can add support for new architectures without having to learn new tools.

- *Hardware Description Languages (HDLs)*—MAX+PLUS II supports a variety of HDL design entry options, including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL).

The MAX+PLUS II design process, shown in Figure 1, consists of four phases: design entry, design compilation, design verification, and device programming.

Figure 1. MAX+PLUS II Design Environment



Design Entry

MAX+PLUS II can integrate multiple design files—generated with MAX+PLUS II design entry tools or with a variety of other industry-standard EDA design entry tools—into a single design hierarchy. The extensive integration between MAX+PLUS II applications allows information to flow freely to and from each application. For example, any errors identified during compilation, simulation, and timing analysis can be automatically located and highlighted in the original design file or in the Floorplan Editor. If a design (called a "project" in MAX+PLUS II) consists of two or more levels of hierarchy, the user can navigate from one design file directly to any other design file in the hierarchy, regardless of whether it is graphic-, text-, or waveform-based.

Industry-Standard LPM Support

Users can create their designs using functions from the industry-standard library of parameterized modules (LPM). The LPM offers scalable logic functions, such as RAM, counters, adders, and multiplexers, and preserves high-level design information for optimal implementation. The MAX+PLUS II Compiler automatically generates optimized, architecture-specific implementations of the LPM functions. LPM functions can be implemented with industry-standard design entry tools, or in schematic or text designs created with MAX+PLUS II.

Industry-Standard EDA Design Entry

The MAX+PLUS II Compiler interfaces with industry-standard EDA tools that generate EDIF 2 0 0 and 3 0 0 netlist files, including files that contain LPM functions. The Compiler uses Library Mapping Files (**.lmf**) to map proprietary symbol and pin names from other EDA tools to MAX+PLUS II logic functions. Altera provides LMFs for over 100 logic functions used with tools from companies such as Cadence, Mentor Graphics, MINC, OrCAD, Viewlogic, and others. VHDL and Verilog HDL design support is also available from Cadence, Exemplar, Mentor Graphics, Synopsys, VeriBest, Viewlogic, and others.

For more information on other industry-standard design entry tools, see *EDA Software Support* in this data book.

MAX+PLUS II can also read OrCAD Schematic Files (**.sch**) or Xilinx Netlist Files (**.xnf**) for compilation or integration into designs for Altera devices.

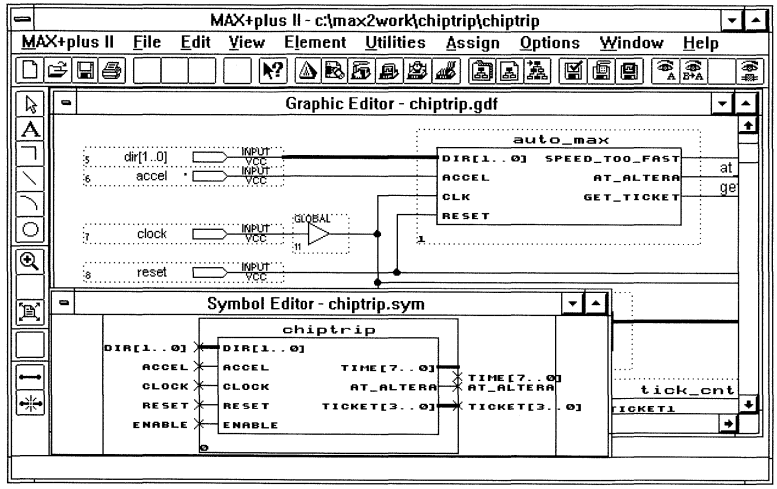
Schematic Capture & Symbol Editing

The MAX+PLUS II Graphic Editor, shown in Figure 2, makes schematic design entry fast and easy. Drag-and-drop editing allows the user to quickly move one or more objects or an entire area. During a move, a net can be preserved with the rubberbanding feature. The designer can also make a design more compact by connecting primitives with buses to create arrays of symbols. MAX+PLUS II provides symbols for over 300 74-series, LPM, and custom functions.

MAX+PLUS II can automatically create a symbol for any design file. With the Symbol Editor (also shown in Figure 2), the designer can modify a symbol to customize its appearance, or create an entirely new symbol.

The MAX+PLUS II Graphic Editor can also open and save OrCAD Schematic Files (**.sch**).

Figure 2. MAX+PLUS II Graphic & Symbol Editors



Hardware Description Language (HDL) Entry

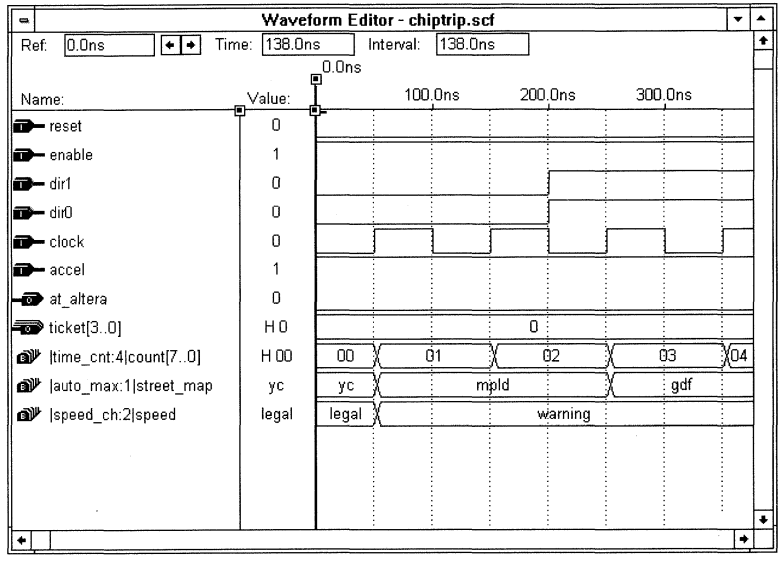
The MAX+PLUS II Text Editor is ideal for entering and editing hardware description language (HDL) design files written in VHDL, Verilog HDL, or the Altera Hardware Description Language (AHDL). The MAX+PLUS II Compiler can synthesize logic from any of these languages and map it to any of Altera's FLEX, MAX, and Classic device families.

Each of these HDLs can implement state machines, truth tables, conditional logic, Boolean equations, and arithmetic operations—including addition, subtraction, equality and magnitude comparison. (In addition, AHDL and VHDL also support the LPM.) Together, these features make it easy to implement complex projects in a concise, high-level description.

Waveform Design Entry

The MAX+PLUS II Waveform Editor (shown in Figure 3) is used to create and edit waveform design files, as well as input vectors for simulation and functional testing. The Waveform Editor also functions as a logic analyzer that allows the designer to view simulation results.

Figure 3. MAX+PLUS II Waveform Editor



Waveform design entry is best suited for sequential and repeating functions. The Compiler's advanced waveform synthesis algorithms automatically generate logic from user-defined input and output waveforms that represent registered, combinatorial, and state machine logic. The Compiler automatically assigns state bits and state variables for state machines.

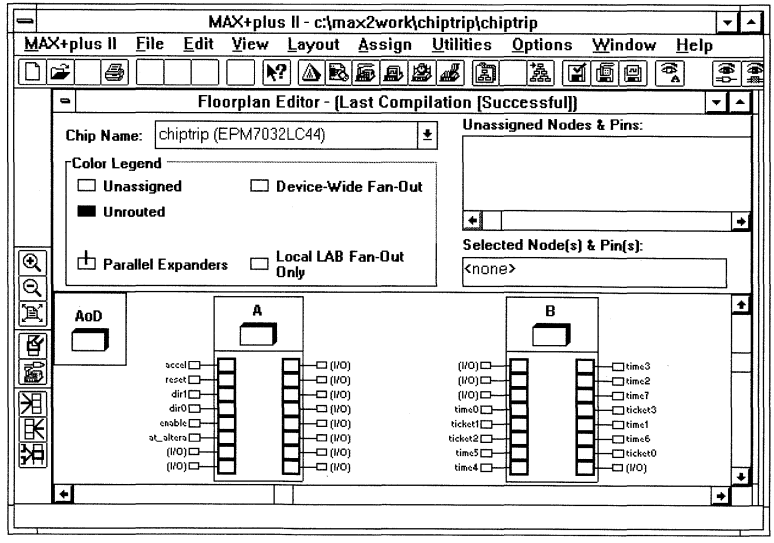
Waveform Editor features allow the designer to copy, cut, paste, repeat, and stretch waveforms; to create design files with internal nodes, flipflops, state machines and memory words; to combine waveforms into groups that display binary, octal, decimal, or hexadecimal values; to compare two sets of simulation results by superimposing one set of waveforms on another; and to annotate files with comments.

Floorplan Editing

The MAX+PLUS II Floorplan Editor (shown in Figure 4) simplifies the process of assigning logic to device pins and logic cells. A graphical image of each device used in a project allows easy logic placement. Both high-level and detailed device views are available. The designer can assign pins and logic cells before compiling a design, and can view and modify the results after compilation.

Floorplan Editor features allow the designer to view all assigned and unassigned logic in a device. The Floorplan Editor provides a color-coded view of all logic resources in the device, as well as user assignments, fan-in and fan-out information, and architecture-specific features. Any node or pin can be dragged to a new location. Logic can be assigned to specific pins and logic cells, or to more general regions within a device. Assignments can also be made with menu commands in any MAX+PLUS II application. All assignments are stored in the text-based Assignment & Configuration File (**.acf**), which can be edited in the MAX+PLUS II Text Editor.

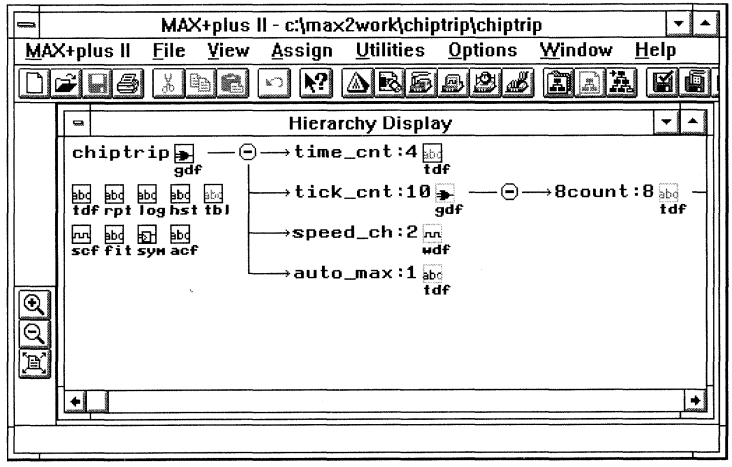
Figure 4. MAX+PLUS II Floorplan Editor



Hierarchical Design Entry

Hierarchical designs can consist of design files created using several different methods, including schematic capture, HDL design entry, waveform design entry, and industry-standard netlist files. MAX+PLUS II supports multiple levels of hierarchy in a single design. This flexibility allows designers to use the design entry method best suited to each portion of the design. The MAX+PLUS II Hierarchy Display, which displays the hierarchical structure of a project, allows designers to easily traverse the hierarchy, automatically opening the appropriate editor for each design file. See Figure 5.

Figure 5. MAX+PLUS II Hierarchy Display

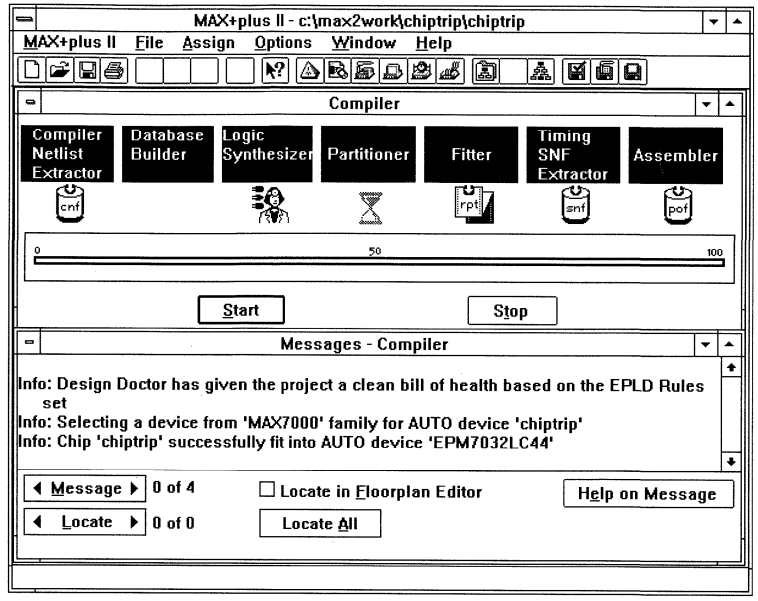


Design Compilation

When MAX+PLUS II processes a design, the Compiler reads in design files and produces output files for programming, simulation, and timing analysis. The Message Processor can automatically locate errors detected during compilation and take users to the source design files. MAX+PLUS II supports FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, MAX 5000, and Classic devices. (Compilation support for FLASHlogic devices is provided by Altera's PLDshell Plus software.)

The MAX+PLUS II Message Processor communicates with all MAX+PLUS II applications, reporting error, information, and warning messages for design problems such as connection and syntax errors, as well as simulation, timing analysis and programming information. Designers can use the Message Processor to automatically open the design file that contains the source of an error and highlight its location. In addition, the Message Processor can locate errors in the floorplan for the current project in the Floorplan Editor. See Figure 6.

Figure 6. MAX+PLUS II Compiler & Message Processor



Logic Synthesis & Fitting

The MAX+PLUS II Compiler's Logic Synthesizer module supports both synthesized and what-you-see-is-what-you-get (WYSIWYG) design implementation. It selects appropriate logic reduction algorithms to minimize and remove redundant logic, ensuring that the device logic resources are used as efficiently as possible for the target device architecture. It also removes unused logic from the project.

Logic synthesis options help the designer guide the outcome of logic synthesis. Altera provides three "ready-made" synthesis styles, which specify the settings for multiple logic synthesis options. The designer can choose a default style to set default synthesis options, create custom styles, and specify individual synthesis options on selected logic functions. Synthesis options can be tailored for a specific device family to take advantage of its architecture. A number of advanced logic options further expand the designer's ability to control logic synthesis.

The Compiler's Fitter module applies heuristic rules to select the best possible implementation for the synthesized project in one or more devices. This automatic fitting relieves the designer of tedious place-and-route tasks. The Fitter generates a Report File (**.rpt**) that shows project implementation as well as any unused resources in the device(s). Fitting results can also be displayed in the MAX+PLUS II Floorplan Editor.

Timing-Driven Compilation

The Compiler can implement user-specified timing requirements for propagation delays (t_{PD}), clock-to-output delays (t_{CO}), setup times (t_{SU}), and clock frequency (f_{MAX}). Designers can specify timing requirements on selected logic functions and for a project as a whole. The Report File and Compiler messages provide detailed information on how the timing requirements have been implemented in the project.

Design-Rule Checking

The MAX+PLUS II Compiler includes the Design Doctor, a design-rule checker. The Design Doctor checks each design file for logic that may cause system-level reliability problems that are usually discovered only after a design has entered production. The user can choose one of three predefined sets of design rules, or create a custom set of rules.

Design rules are based on reliability guidelines that cover potential design problems such as asynchronous inputs, ripple clocks, multi-level logic on clocks, preset and clear configurations, and race conditions. Rule violations are explained to help the designer determine which edits are needed in the design files.

Multi-Device Partitioning

If a project is too large to fit in a single device, the Compiler's Partitioner module divides it into multiple devices from the same device family. The Partitioner attempts to split the project into the fewest possible number of devices while minimizing the number of pins used for inter-device communication. The Fitter automatically fits the logic into the specified devices.

Partitioning can be totally automatic, partially user-controlled, or fully user-controlled. If a project is too large to fit into the target device, the designer can specify the type and number of additional devices.

Industry-Standard Simulation Formats

The MAX+PLUS II Compiler can create netlist files for use in a variety of simulation environments. These netlist files contain post-synthesis functional and timing information that can be used with standard design verification tools for device- or board-level simulation.

The following interfaces are available:

Interface:	MAX+PLUS II Support:
EDIF	Creates EDIF 2 0 0 and 3 0 0 netlist files that provide functionality and timing for third-party simulators.
Verilog HDL	Creates Verilog HDL netlist files that can be used with Verilog-XL simulators.
VHDL	Creates VHDL netlist files that can be used with VHDL simulators.

For each interface, the Compiler can optionally generate a Standard Delay Output Format File (**.sdo**) that includes timing information for simulators that require timing and functional information in separate files.

Programming File Generation

The Assembler module creates one or more Programmer Object Files (**.pof**), SRAM Object Files (**.sof**), JEDEC Files (**.jed**), Hexadecimal (Intel-format) Files (**.hex**), and Tabular Text Files (**.ttf**) for a compiled project. The MAX+PLUS II Programmer uses POFs, SOFs, and JEDEC Files together with standard Altera hardware to program devices. Device programming is also available with other industry-standard programming equipment. In addition, MAX+PLUS II can generate Raw Binary Files (**.rbf**) and Serial Bitstream Files (**.sbf**). These files, as well as Hex files and TTFs can be used for configuring FLEX 10K and FLEX 8000 devices in-system. MAX+PLUS II POFs and Serial Vector Format (**.svf**) files can be used for in-system programming of MAX 9000 and MAX 7000S devices.

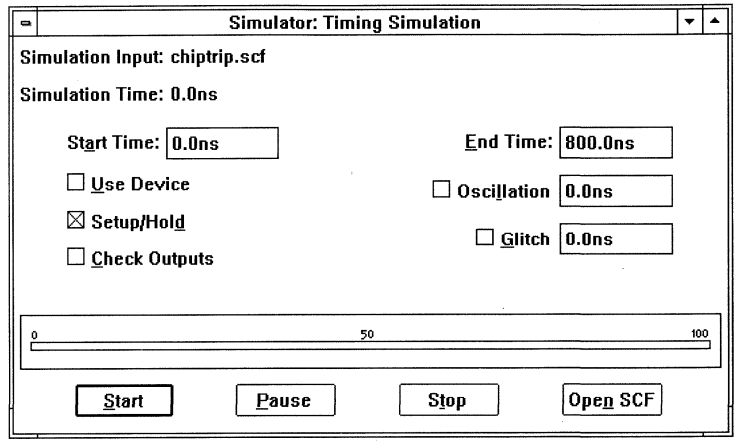
Design Verification

MAX+PLUS II offers design verification capabilities, including design simulation and timing analysis, that test the logical operation and internal timing of a design. Design verification tools for Altera devices are also available from a variety of EDA vendors.

Simulation

The MAX+PLUS II Simulator provides flexibility and control for modeling single- or multi-device projects. The Simulator uses simulation netlist files that are generated during compilation to perform functional, timing, or multi-device simulation for a project. Figure 7 shows the MAX+PLUS II Simulator.

Figure 7. MAX+PLUS II Simulator



The designer either defines input stimuli with a straightforward vector input language or draws waveforms directly with the MAX+PLUS II Waveform Editor. Simulation results can be viewed in the Waveform Editor or Text Editor and printed as waveform or text files.

The designer specifies commands either interactively or in a text-based command file to perform a variety of tasks, such as monitoring the project for glitches, oscillation, and register setup and hold time violations; halting the simulation when user-defined conditions are met; forcing flipflops high or low; performing functional testing; and defining initial memory contents for RAM or ROM blocks. If a setup or hold time, minimum pulse width, or oscillation period is violated, the Message Processor reports the problem. The designer can then use the Message Processor to locate the time at which the problem occurred in the Waveform Editor and to locate the error in the original design file.

For easy comparison, the designer can superimpose the results of two simulations in the Waveform Editor.

Functional Simulation

The MAX+PLUS II Simulator supports functional simulation to test the logical operation of a project before it is synthesized, thereby allowing the designer to quickly identify and correct logical errors. The MAX+PLUS II Waveform Editor displays the results of functional simulation and provides easy access to all nodes in the project, including combinatorial functions.

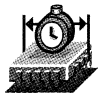
Timing Simulation

In a timing simulation, the MAX+PLUS II Simulator tests the project after it has been fully synthesized and optimized. Timing simulation is performed at 0.1-ns resolution.

Multi-Device Simulation

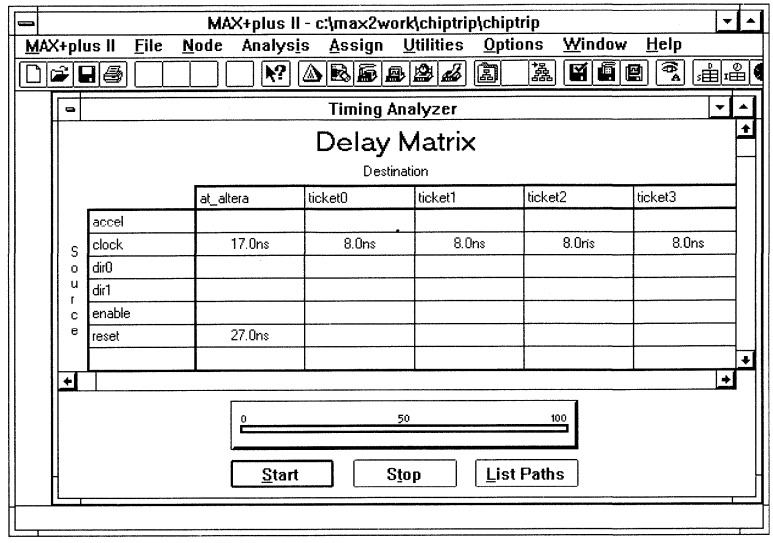
MAX+PLUS II can combine the timing and/or functional information from multiple Altera devices, allowing the designer to simulate several devices operating together. Devices from different Altera device families can be used in the same project.

Timing Analysis



The MAX+PLUS II Timing Analyzer can calculate a matrix of point-to-point device delays, determine setup and hold time requirements at device pins, and calculate maximum clock frequency. MAX+PLUS II design entry tools are integrated with the Timing Analyzer, allowing the designer to simply tag start and end points in the design files or the Floorplan Editor to determine the shortest and longest propagation delays. In addition, the Message Processor can locate and display critical paths identified by the Timing Analyzer in the source design files or in the Floorplan Editor. See Figure 8.

Figure 8. MAX+PLUS II Timing Analyzer

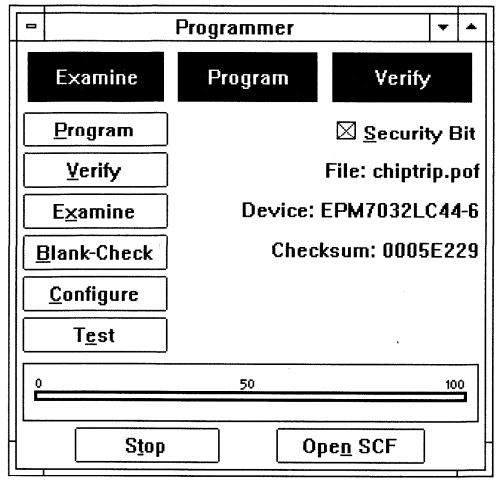


Device Programming

The MAX+PLUS II Programmer, shown in Figure 9, uses programming files generated by the MAX+PLUS II Compiler or PLDshell Plus compiler to program Altera devices. The Programmer allows the designer to program, verify, examine, blank-check, and functionally test devices.

Altera provides all hardware and software necessary for programming and verifying devices, including a Logic Programmer Card and Master Programming Unit (MPU). The add-on Logic Programmer card (for PC-AT or compatible computers) drives the MPU. The MPU performs continuity checking to ensure adequate electrical contact between the programming adapter and the device. With the appropriate programming adapter, the MPU also supports functional testing, so that vectors created for simulation can be applied to a programmed device to verify its functionality.

Figure 9. MAX+PLUS II Programmer



Altera also provides the FLEX Download Cable and the BitBlaster for device programming and configuration. The FLEX Download Cable can connect any Configuration EPROM programming adapter, which is installed on the MPU, to a single target FLEX 10K or FLEX 8000 device in a prototype system. The BitBlaster serial download cable is a hardware interface to a standard PC or UNIX workstation RS-232 port that provides configuration/programming data to FLEX 10K, FLEX 8000, MAX 9000, MAX 7000S, and FLASHlogic devices on system boards. The BitBlaster also allows users to configure a FLEX 10K or FLEX 8000 device independent of the MAX+PLUS II Programmer.

With the BitBlaster, designers can also configure/program multiple FLEX 10K, FLASHlogic, MAX 9000, and MAX 7000S devices using the multi-device JTAG chain mode and the MAX+PLUS II Programmer.

For more information on the BitBlaster, Altera programming hardware and software, other programming hardware manufacturers, or multi-device JTAG chain programming and configuration, refer to the following sources:

- *BitBlaster Serial Download Cable Data Sheet* in this data sheet
- *Altera Programming Hardware Data Sheet* in this data sheet
- *Programming Hardware Manufacturers* in this data sheet
- "Setting Up Multi-Device JTAG Chains" in MAX+PLUS II Help

On-Line Help

On-line help provides access to all information on MAX+PLUS II. It includes complete, up-to-date documentation on all MAX+PLUS II applications, causes and suggested actions for messages, references to related Altera documentation, text file formats (e.g., AHDL), and information on Altera devices and adapters.

On-line help is only a keystroke or a mouse click away. The F1 key provides instant access to information on a dialog box, highlighted menu command, or pop-up message. Typing Shift+F1 or choosing the context-sensitive help button on the toolbar turns the mouse pointer into a question mark pointer that allows the designer to click on any item on the screen—including logic functions and AHDL keywords—for context-sensitive help on that item.

Software Maintenance Agreement

To guarantee timely upgrades for software and documentation, Altera offers a Software Maintenance Agreement that entitles the customer to software updates, discounts on selected software products, and Applications Engineering support.

Recommended System Configurations

To run MAX+PLUS II software with optimum results, Altera recommends the following system configurations:

PC System Configuration

- Pentium-based PC-AT or compatible computer
- The following shows the available memory requirements (i.e., combined RAM and virtual memory) for Altera device families:
  - FLEX 10K devices, 128 Mbytes of available memory, including 64 Mbytes of RAM
  - FLEX 8000 devices, 64 Mbytes of available memory, including 32 Mbytes of RAM
  - MAX 9000 devices, 64 Mbytes of available memory, including 32 Mbytes of RAM
  - All other devices, 32 Mbytes of available memory, including 16 Mbytes of RAM
- Microsoft Windows NT version 3.51 or higher, Windows 95, Windows version 3.1, or Windows for Workgroups version 3.11
- Microsoft Windows-compatible graphics card and monitor
- CD-ROM drive
- Microsoft Windows-compatible 2- or 3-button mouse
- Full-length 8-bit ISA slot for a Logic Programmer card
- Parallel port
- RS-232 serial port for the BitBlaster

Sun SPARCstation System Configuration

- Sun SPARCstation with color monitor
- 32 Mbytes of RAM (for FLEX 10K and large FLEX 8000 device projects, 64 Mbytes of RAM)
- Sun OS 4.1.2 or higher
- Sun OpenWindows 3.0 or higher
- Solaris 2.4 or higher
- ISO 9660-compatible CD-ROM drive
- RS-232 serial port for the BitBlaster

HP 9000 Series 700 Workstation System Configuration

- HP 9000 Series 700 workstation with color monitor
- 32 Mbytes of RAM (for FLEX 10K and large FLEX 8000 device projects, 64 Mbytes of RAM)
- HP-UX version 9.03 or higher
- HP-VUE
- ISO 9660-compatible CD-ROM drive
- RS-232 serial port for the BitBlaster

IBM RISC System/6000 Workstation System Configuration

- IBM RISC System/6000 workstation with color monitor
- 32 Mbytes of RAM (for FLEX 10K and large FLEX 8000 device projects, 64 Mbytes of RAM)
- AIX version 3.2.5 or higher
- AIX Windows version 1.2.5 or higher
- ISO 9660-compatible CD-ROM drive
- RS-232 serial port for the BitBlaster

Go to the MAX+PLUS II **read.me** file for the most-up-to-date information regarding system requirements.

Software Package Options

Altera offers a variety of tool configurations and add-on migration products for PC- and UNIX workstation-based versions of MAX+PLUS II. In addition, any customer who purchases a PC-based MAX+PLUS II software product receives a site license to install an unlimited number of copies of the PLS-ES feature set for the MAX+PLUS II development software.

For up-to-date information on MAX+PLUS II software packages and development systems, contact your local sales representative or Altera Literature Services.

Notes:

BitBlaster Serial Download Cable

June 1996, ver. 3 — Data Sheet

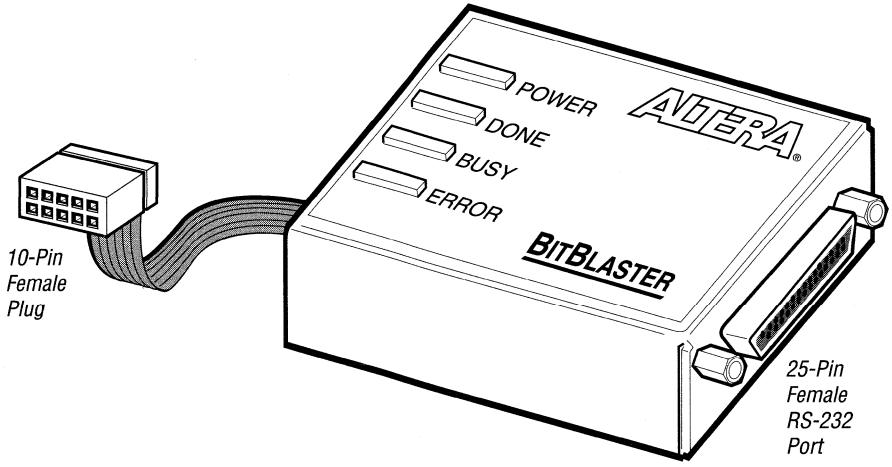
Features

- Allows PC and workstation users to:
  - Program MAX 9000, MAX 7000S, and FLASHlogic devices in-system via a standard RS-232 serial port
  - Configure FLEX 10K, FLEX 8000, and FLASHlogic devices in-circuit via a standard RS-232 serial port
- Downloads data from:
  - MAX+PLUS II development software on UNIX workstations and PCs
  - A system prompt on UNIX workstations and PCs
- Provides two download modes: passive serial (PS) and JTAG
- Programs/configures a single device or multiple devices in a chain
- Supports data transfer rates from 9,600 to 230,400 baud

Functional Description

The BitBlaster serial download cable (ordering code: PL-BITBLASTER) is a hardware interface to a standard RS-232 port (called a "COM port" on a PC). This cable channels configuration data to FLEX 10K, FLEX 8000, and FLASHlogic devices as well as programming data to MAX 9000, MAX 7000S, and FLASHlogic devices. Because design changes are downloaded directly to the device, prototyping is easy, and multiple design iterations can be accomplished in quick succession. See Figure 1.

Figure 1. BitBlaster



A-DS-BITBL-03

Download Modes

The BitBlaster provides two download modes:

- Passive serial (PS) mode—Used for configuring FLEX 10K and FLEX 8000 devices
- JTAG mode—Industry-standard JTAG implementation for programming or configuring FLEX 10K, MAX 9000, MAX 7000S, and FLASHlogic devices

BitBlaster Connections

Data is downloaded from the computer's RS-232 port through the BitBlaster to the circuit board via the connections discussed in this section.

BitBlaster Female Port & Plug Connections

The 25-pin female port connects to an RS-232 port with a standard serial cable. See Table 1.

Table 1. BitBlaster 25-Pin Serial Port Pin-Outs

Pin	Signal Name	Description
2	tx	Transmit data
3	rx	Receive data
4	rts	Request to send
5	cts	Clear to send
6	dsr	Data set ready
7	GND	Signal ground
20	dtr	Data terminal ready

The 10-pin female plug connects to a 10-pin male header on the circuit board containing the target device(s). Figure 2 shows the dimensions for the 10-pin female plug, including the 0.1-inch spacing between pin centers.

Figure 2. BitBlaster 10-Pin Female Plug Dimensions

Dimensions are shown in inches.

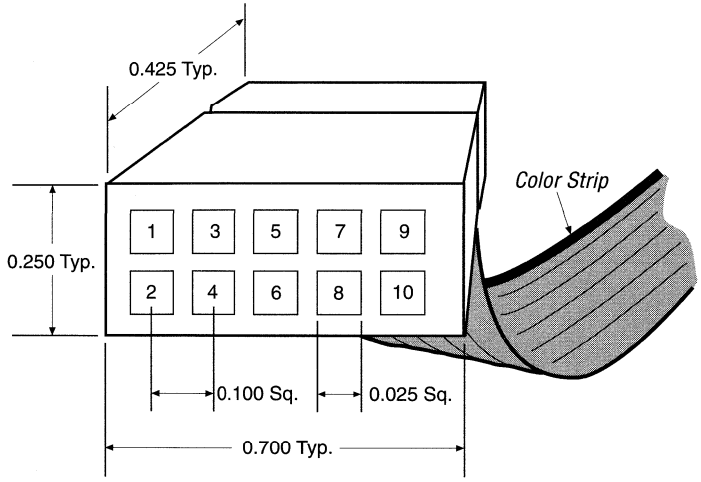


Table 2 identifies the 10-pin female plug's pin names for the corresponding download mode.

Table 2. BitBlaster Pin Names

Pin	Passive Serial Mode *(1)*	JTAG Mode *(1), (2)*
1	DCLK	TCK
2	GND	GND
3	CONF_DONE	TDO
4	VCC	VCC
5	nCONFIG	TMS
6	NC	NC
7	nSTATUS	NC
8	NC	NC
9	DATA0	TDI
10	GND	GND

Notes:

(1) FLEX 10K devices can be configured in either of the BitBlaster download modes.

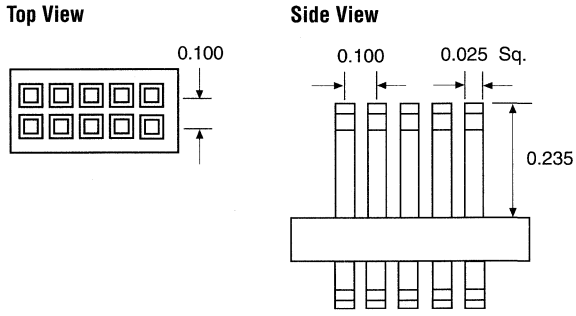
(2) For circuit boards designed with the FLASHlogic download cable (PL-FLDLC) header, Altera provides a BitBlaster-to-FLDLC adapter cable. Contact Altera Applications or your local Altera sales representative for more information.

Circuit Board Header Connection

The BitBlaster 10-pin female plug connects to a 10-pin male header on the circuit board. The 10-pin male header has two rows of five pins connecting the circuit board to the device's programming or configuration pins. The BitBlaster receives power and downloads data via the male header. Figure 3 shows the dimensions of a typical 10-pin male header.

Figure 3. 10-Pin Male Header Dimensions

Dimensions are shown in inches.



BitBlaster Status Lights

The BitBlaster status lights indicate the state of the device configuration or programming. See Table 3.

Table 3. BitBlaster Status Lights

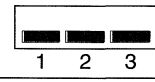
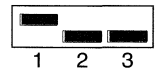
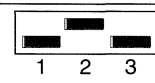
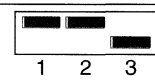
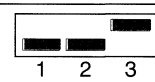
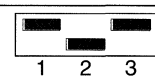
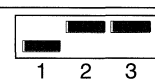
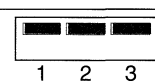
Status Light	Description
POWER	Indicates a connection to the target system's power supply.
DONE	Indicates device configuration or programming is complete.
BUSY	Indicates device configuration or programming is in process.
ERROR	Indicates error detection during configuration or programming.

☞ The circuit board must supply V_{CC} and GND to the BitBlaster.

Data Transfer Rate Control & Operating Conditions

Three DIP-switches on the side panel of the BitBlaster control the baud rate of the serial data. Table 4 shows the on/off dipswitch settings, which can be used to specify transfer rates ranging from 9,600 to 230,400 baud. The configuration time for an EPF81188 device, which has 193,000 bits of configuration data, is also provided for reference.

Table 4. Dipswitch Settings, Note (1)

Baud Rate (BPS)	Dipswitch Positions	EPF81188A Configuration Time (Seconds)
230,400		1.5
115,200		3.0
76,800		4.5
57,600		5.5
38,400		8.5
19,200		17.0
14,400		22.0
9,600		33.0

Note:

(1) The supported baud rate varies depending on the computer system. Refer to the serial port hardware documentation to varify the available baud rates.

BitBlaster Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	With respect to GND	–2.0	7.0	V

BitBlaster Recommended Operating Conditions

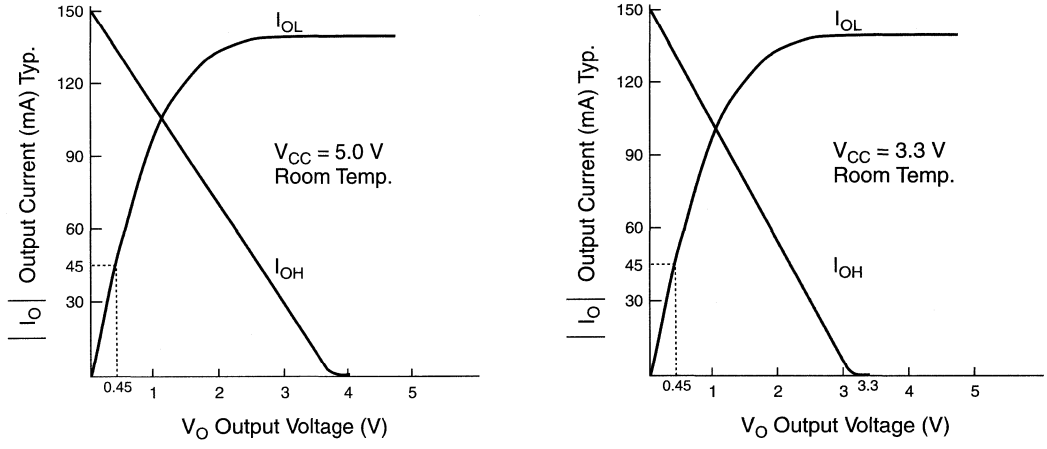
Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage 5.0-V operation		4.75	5.25	V

BitBlaster DC Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA, V_{CC} = 4.75 V	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC		0.45	V

Figure 4 shows the typical 5.0-V and 3.3-V I-V output drive characteristics of the BitBlaster.

Figure 4. Output Drive Characteristics of the BitBlaster



Passive Serial Mode

This section discusses passive serial configuration for single and multiple FLEX devices.

Passive Serial Configuration for Single FLEX Devices

Single FLEX 10K or FLEX 8000 devices can be configured using the passive serial configuration scheme from one of the following:

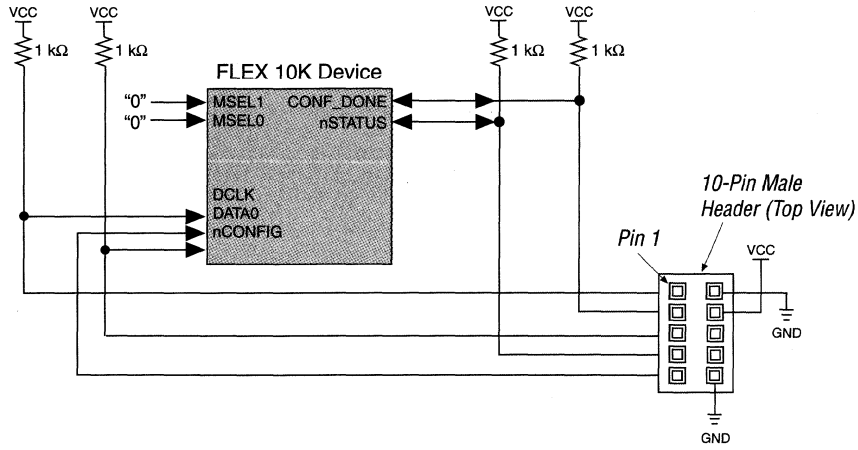
- The MAX+PLUS II Programmer. Devices are configured with an SRAM Object File (**.sof**), which is generated automatically during project compilation.
- A command prompt from a PC or workstation. Devices are configured with a Serial Bitstream File (**.sbf**).

For specific software instructions refer to the "Software Instructions" on page 565 in this data sheet.

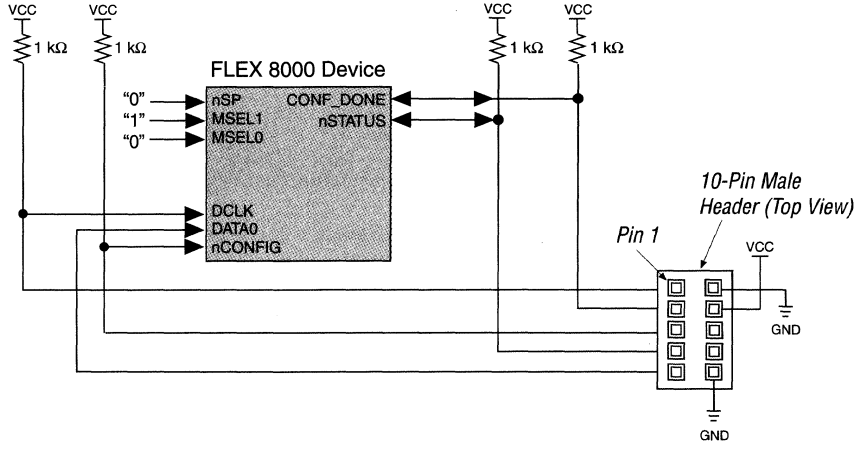
Figure 5 shows how the BitBlaster interfaces to a single FLEX device. (If the DATA0 pin is used in the user mode, it must be isolated during configuration.)

Figure 5. FLEX Device Configuration with the BitBlaster

FLEX 10K Device



FLEX 8000 Device



Passive Serial Configuration for Multiple FLEX Devices

Multiple FLEX 10K or FLEX 8000 devices can be configured via the BitBlaster passive serial mode from a PC or Unix Workstation command prompt. Devices are configured with a Serial Bitstream File (**.sbf**). For specific software instructions, refer to the "Software Instructions" on page 565 in this data sheet.

Figures 6 and 7 show the BitBlaster interface to multiple FLEX 10K and FLEX 8000 devices using the passive serial configuration.

Figure 6. FLEX 10K Multi-Device Configuration with the BitBlaster

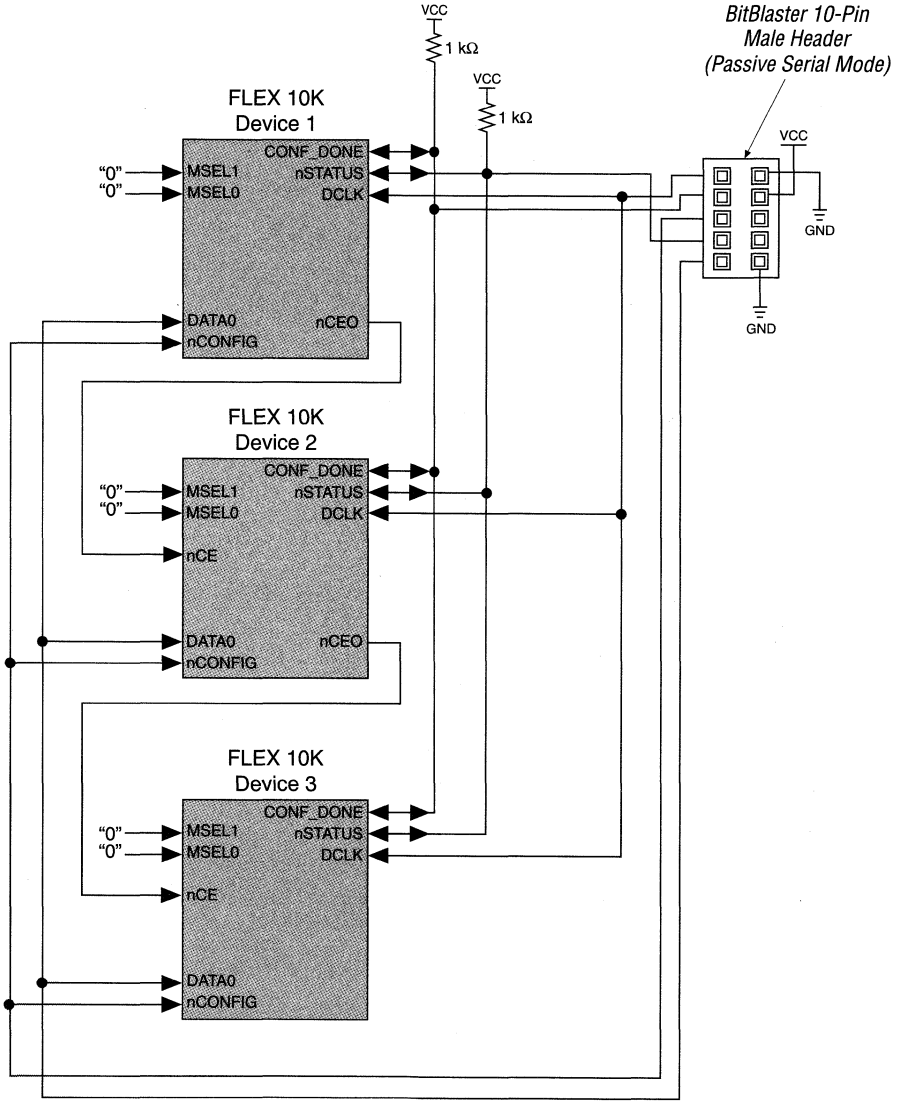
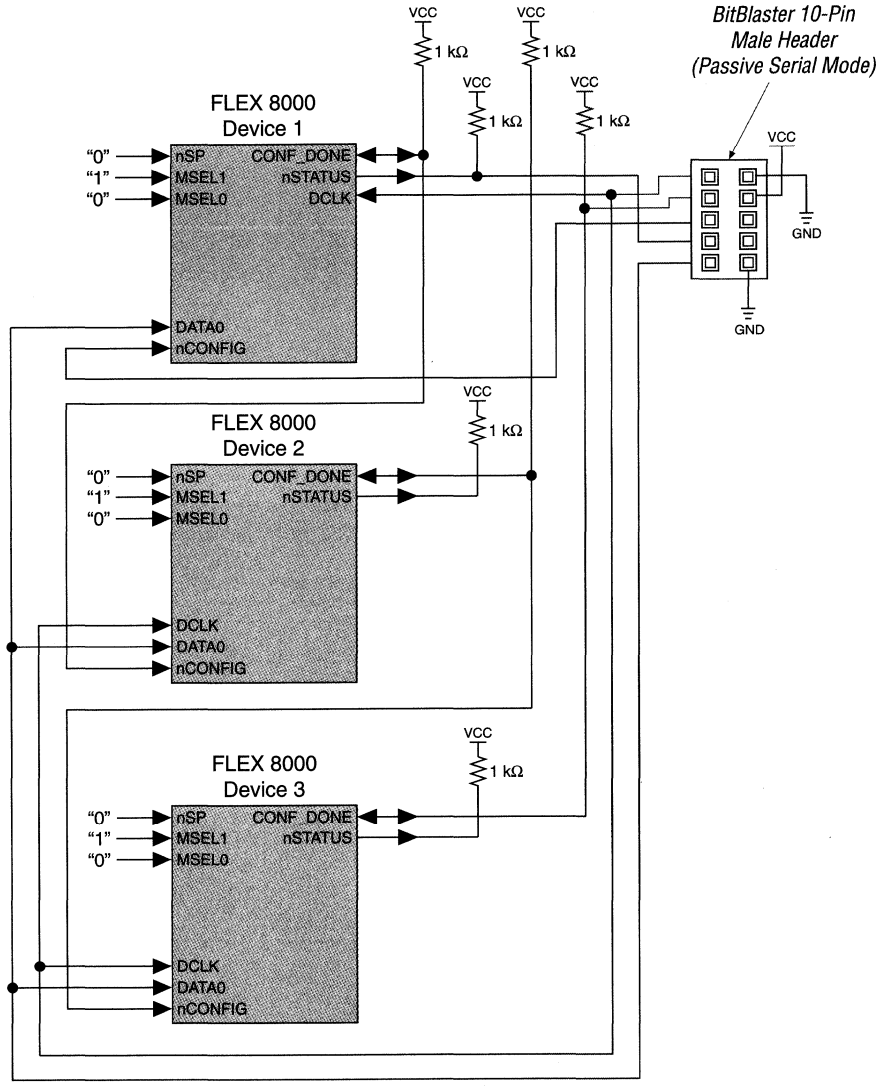


Figure 7. FLEX 8000 Multi-Device Configuration with the BitBlaster



Go to the following sources for additional information:

- *Application Note 33 (Configuring FLEX 8000 Devices)* for information on device configuration with the BitBlaster.
- "Configuring a FLEX 8000 or FLEX 10K Device with the BitBlaster" in MAX+PLUS II Help.

JTAG Mode

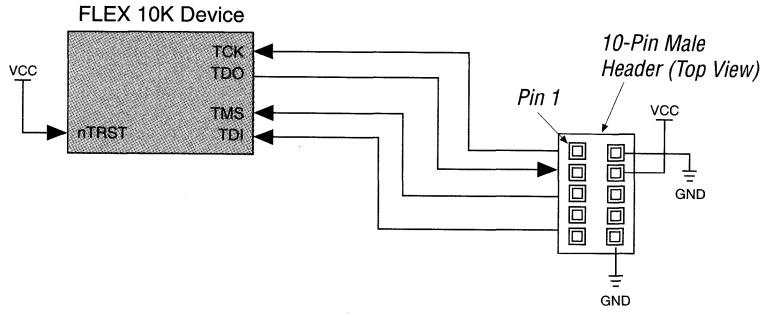
In JTAG mode, the BitBlaster connects to a device on the circuit board via any standard RS-232 port for in-system programming and in-circuit reconfiguration. This section discusses the following:

- JTAG configuration of a single FLEX 10K device
- JTAG programming of a single MAX 9000 and MAX 7000 device
- JTAG configuration and programming of a single FLASHlogic device
- JTAG programming and configuration of multiple JTAG-Compatible devices

JTAG Configuration of a Single FLEX 10K Device

The SRAM Object File (**.sof**) automatically created during compilation, can be downloaded directly to the device via the BitBlaster. Refer to "Software Instructions" on page 565 for more information. Configuration is accomplished via the following device JTAG pins: TCK,TMS, TDI, and TDO. Figure 8 shows how the BitBlaster interfaces with a MAX 9000 or MAX 7000S device. All other I/O pins are tristated during this configuration.

Figure 8. JTAG Configuration of a Single FLEX 10K Device



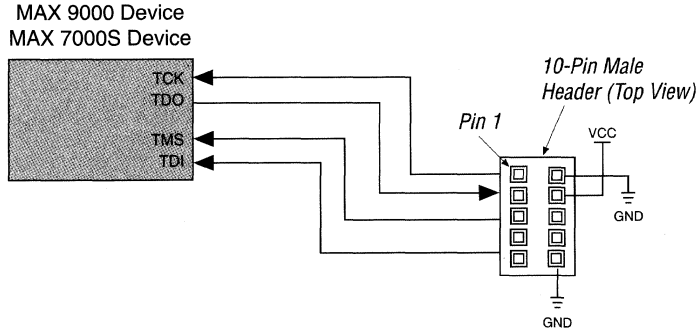
Search for "Configuring a Device with the BitBlaster" in MAX+PLUS II Help for more information.

JTAG Programming of a Single MAX 9000 & MAX 7000S Device

A Programmer Object File (**.pof**), which is automatically created during compilation, can be downloaded directly to the device via the BitBlaster. Refer to "Software Instructions" on page 565 in this data sheet for more information.

Devices are programmed with the following JTAG pins: TCK, TMS, TDI, and TDO. Figure 9 shows how the BitBlaster interfaces with a MAX 9000 or MAX 7000S device. The I/O pins are tri-stated during in-system programming.

Figure 9. MAX 9000 & MAX 7000S Device Programming with the BitBlaster



Search for "Programming a Device with the BitBlaster" in MAX+PLUS II Help for more information.

JTAG Programming & Configuration of a Single FLASHlogic Device

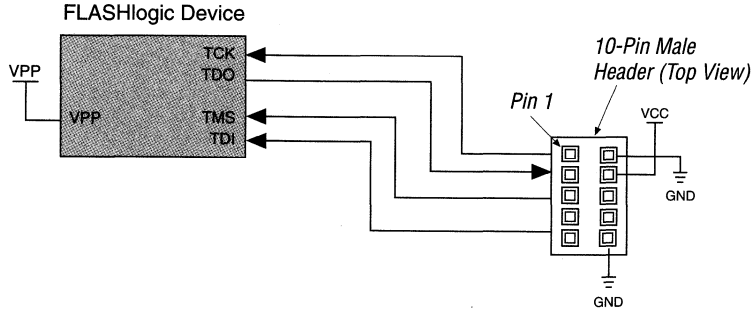
The BitBlaster connects any standard RS-232 port to a single FLASHlogic device in the prototype system. Design entry, compilation, and simulation of FLASHlogic devices is supported by Altera PLDshell Plus development system.

The JEDEC File (**.jed**) generated by PLDshell Plus can be used together with the MAX+PLUS II Programmer to program and configure FLASHlogic devices with the BitBlaster. Refer to "Software Instructions" on page 565 in this data sheet.

When programming, the VPP pin needs to be raised to the appropriate programming voltage as specified in the *FLASHlogic Programmable Logic Device Family Data Sheet* in this data book. During programming and configuration, the I/O pins of FLASHlogic devices are tri-stated. Additionally, EPX8160 device I/O pins have a weak pull-up.

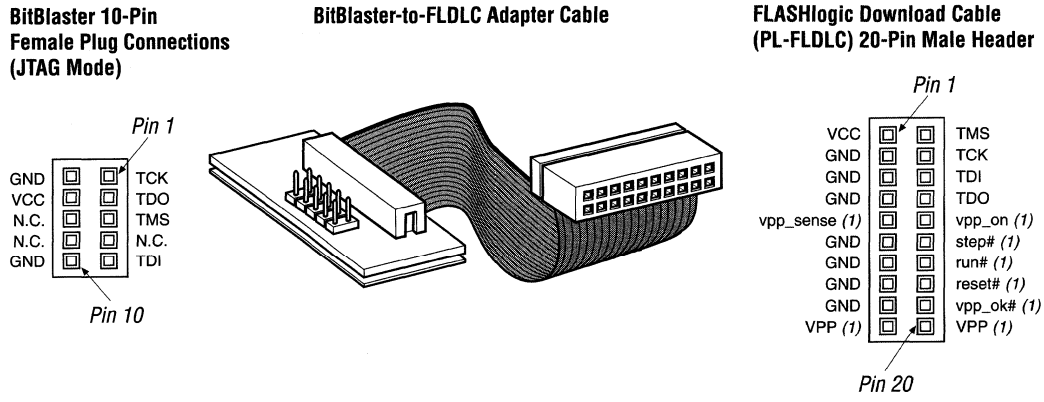
Devices are configured and programmed with the following JTAG pins: TCK, TMS, TDI, and TDO. Figure 10 shows how the BitBlaster interfaces to the target FLASHlogic device.

Figure 10. FLASHlogic Device Programming & Configuration with the BitBlaster



For circuit boards designed with a 20-pin FLASHlogic Download Cable (PL-FLDLC) header, Altera Applications provides a BitBlaster-to-FLDLC adapter cable that converts the 10-pin BitBlaster interface to the 20-pin PL-FLDLC interface. The adapter cable's 20-pin plug is then connected to the 20-pin male header on the circuit board containing the FLASHlogic device. See Figure 11.

Figure 11. BitBlaster-to-FLDC Adapter Cable (Optional)



Note:
(1) This signal is not supported by the BitBlaster.

Table 5 summarizes the FLASHlogic Download Cable pins supported by the BitBlaster.

Table 5. BitBlaster-Supported FLASHlogic Download Cable Pins

FLASHlogic Download Cable Pins	BitBlaster Pins
VCC	VCC
TMS	TMS
GND	GND
TCK	TCK
TDI_PORT	TDO
TDO_PORT	TDI
vpp_sense	–
vpp_on	–
step#	–
run#	–
reset#	–
vpp_ok#	–
VPP	–

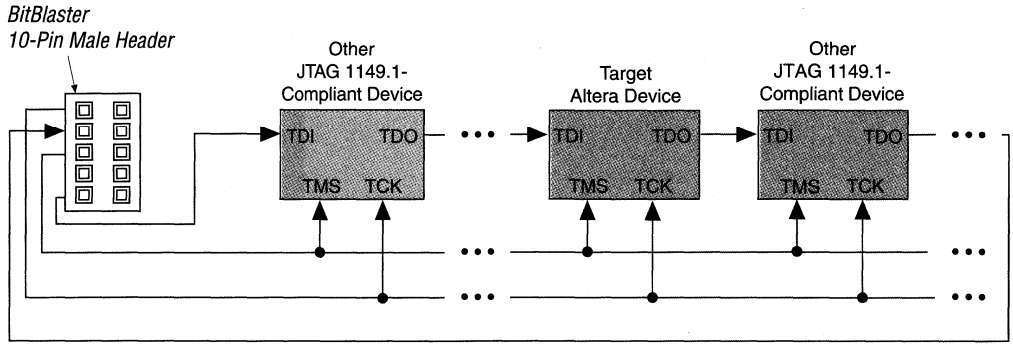
Search for the following topics in MAX+PLUS II Help for more information:

- "Configuring a FLASHlogic Device with the BitBlaster"
- "Programming a Device with the BitBlaster"

JTAG Programming & Configuration of Multiple Devices

When programming a JTAG chain of devices, one JTAG-compatible header, such as the BitBlaster 10-pin male header, is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the BitBlaster. JTAG-chain device programming is ideal when the PCB contains multiple devices, or when the PCB will be tested using JTAG BST. See Figure 12.

Figure 12. JTAG-Chain Device Programming & Configuration with the BitBlaster



To program a single device in a JTAG chain, the programming software places all other devices in the JTAG chain in BYPASS mode. When in BYPASS mode, devices pass programming data from the TDI pin to the TDO pin through a single bypass register without being affected internally, thereby enabling the programming software to program or verify the target device.

MAX 9000, MAX 7000S, and FLASHlogic devices can be programmed in-system using a JTAG chain; FLEX 10K and FLASHlogic devices can be configured in-circuit using a JTAG chain.

Go to the following sources for additional information:

- *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)*
- "Setting Up Multi-Device JTAG Chains" in MAX+PLUS II Help

Software Instructions

The MAX+PLUS II Programmer downloads configuration or programming data. For FLEX 10K and FLEX 8000 devices, configuration data can also be sent directly by copying the SBF to the RS-232 port from the system prompt.

Downloading Configuration or Programming Data from the MAX+PLUS II Programmer

To configure or program one or more devices with the BitBlaster and the MAX+PLUS II Programmer:

1. Compile a project. The MAX+PLUS II Compiler automatically generates an SOF for FLEX 10K and FLEX 8000 device configuration, or a POF for MAX 9000 and MAX 7000S device programming. The PLDShell Plus Compiler automatically generates a JEDEC File for FLASHlogic devices.

2. Attach the BitBlaster to an RS-232 port on a PC or UNIX workstation and plug the 10-pin female header into the prototype system containing the target device. Ensure that the POWER status light is on. The board must supply power to the BitBlaster.

3. If necessary, change the BitBlaster baud rate using the DIP-switches on its side panel. DIP-switch settings are listed in Table 4 on page 553.

4. Open the MAX+PLUS II Programmer, in the **Hardware Setup** dialog box (Options menu) choose **BitBlaster** as the *Hardware Type* and select the appropriate port for the*RS-232 Port* fields. Choose **OK**.

5. When you first open the Programmer, MAX+PLUS II automatically loads the programming file for the current project (either a POF, JEDEC File, or SOF), or the first programming file for a multi-device project. To specify another programming file, choose **Select Programming File** (File menu) and specify the correct file type. For a FLEX 10K or FLEX 8000 device, select an SOF; for a MAX 9000 or MAX 7000S device, select a POF; for a FLASHlogic device, select a JEDEC File.

6. If using a multi-device JTAG chain to program or configure devices, turn on **Multi-Device JTAG-Chain** (JTAG menu) and use the **Multi-Device JTAG Chain Setup** command to specify the devices in the JTAG Chain.

7. Choose the **Program** button to start downloading the configuration or programming data. The BUSY status light on the BitBlaster turns on.

The BitBlaster downloads the data from the SOF, POF, or JEDEC File into the device. When configuration or programming is complete, the BUSY status light turns off, and the DONE status light turns on. After the DONE status light turns on, the BitBlaster can be disconnected.

Downloading Configuration Data from a System Prompt (FLEX Devices Only)

To configure a single FLEX 10K or FLEX 8000 device with the BitBlaster from a system prompt:

1. Compile a project with the MAX+PLUS II Compiler. The Compiler automatically generates an SOF for device configuration.

2. Open the MAX+PLUS II Programmer or Compiler and choose the **Combine Programming Files** command (File menu).

3. Specify the SOF name by selecting it in the *Files* box or by typing its name in the *File Name* box. Choose **Add** to add the file to the *Selected Files* box.

4. Specify the desired configuration file format by selecting SBF *(Sequential)* in the *File Format* drop-down list box. Choose **OK**.

5. Attach the BitBlaster to an RS-232 port on your PC or UNIX workstation, and plug the 10-pin female header into the prototype system that contains the target FLEX 10K or FLEX 8000 device. Ensure that the POWER status light is on. The board must supply power to the BitBlaster.

6. If necessary, change the baud rate of the BitBlaster using the dipswitches on its side panel. Dipswitch settings are listed in Table 4 on page 553.

7. Specify an RS-232 port and set its baud rate.

✓ On a PC, follow these steps:

a. For 9,600 baud, type the following command at the system prompt:

```
mode com<port number>:9600,N,8,1 ↵
```

b. For baud rates greater than 9,600, type the following command at the system prompt:

```
slikmode/b<baud rate>/c<port number> ↵
```

☞ The **slikmode.exe** utility is available on the Altera bulletin board service (BBS) at (408) 954-0104, or from the Altera FTP site at **ftp.altera.com** as a self-extracting executable, **bitmode.exe**. For more detailed instructions on using the **slikmode.exe** utility, type `slikmode ↵` at the system prompt.

✓ Because commands on UNIX workstations differ, the following is provided only as an example: On a UNIX workstation, type the following command from the system prompt:

```
stty <baud rate> </dev/<serial port#> ↵
```

Check the workstation specifications to determine the maximum baud rate allowed by the hardware.

8. Configure the FLEX 10K or FLEX 8000 device by copying the SBF to the serial port to which the BitBlaster is attached.

✓ On a PC, type the following command from the system prompt:

```
copy <filename>.sbf com<port number>: ↵
```

✓ Because commands on UNIX workstations differ, the following is provided only as an example: On a UNIX workstation, type the following command from the system prompt:

```
cp <filename>.sbf /dev/<serial port#> ↵
```

Notes:

Altera Programming Hardware

June 1996, ver. 3 Data Sheet

General Description

Altera offers a variety of hardware to program and configure Altera devices. For conventional device programming, in-system programming, and in-circuit reconfiguration, designers can choose from the hardware options shown in Table 1. The subsequent section describes the hardware options listed in Table 1.

Table 1. Available Hardware Options for Altera Device Programming & Configuration

	External Programming Hardware *Note (1)*	FLEX Download Cable	BitBlaster Serial Download Cable
Conventional device programming	✓	✓	
In-system programming			✓
In-circuit reconfiguration	✓	✓	✓

Note:
(1) External programming hardware includes the Altera Stand-Alone Programmer (PL-ASAP2), LP6 Logic Programmer card, and MPU.

☞ Altera devices are also supported by a variety of third-party programmers. Refer to *Altera Programming Hardware Manufacturers* in this data book for more information.

External Programming Hardware

Altera provides the following external programming hardware: Altera Stand-Alone Programmer, Logic Programmer Card, Master Programming Unit, and programming adapters.

Altera Stand-Alone Programmer

The Altera Stand-Alone Programmer, PL-ASAP2, together with the appropriate programming adapters, provides the hardware and software needed for either programming EPROM-, EEPROM-, and FLASH-based Altera devices, or configuring SRAM-based devices. PL-ASAP2 includes an LP6 Logic Programmer card, an MPU, MAX+PLUS II Programmer software (which requires Microsoft Windows or Windows NT), and complete documentation. The MAX+PLUS II Programmer supports device configuration for FLEX 10K and FLEX 8000 devices, and device programming for MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices.

Ordering Code: *PL-ASAP2*

Logic Programmer Card

The LP6 Logic Programmer card generates programming waveforms and voltages for the MPU. The software-controlled card can be installed into any full-length computer expansion slot in an IBM PC-AT or compatible computer. The LP6 card is available as part of PL-ASAP2 or individually.

Ordering Code: *PLP6*

Master Programming Unit

The Master Programming Unit (MPU) is a hardware module that is used together with an appropriate adapter to program Altera devices. The MPU connects to a Logic Programmer card via a 25-pin ribbon cable. The MPU receives power from the Logic Programmer card installed in an IBM PC-AT or compatible computer and does not require an external power supply. Programming and functional test information is transmitted from the Logic Programmer card through the ribbon cable to the MPU. A programming status light on the MPU lights up when the unit is active.

When used with the appropriate adapter, the MPU automatically tests for continuity between the device leads and the programming socket before programming. It can also apply test vectors to functionally test and verify programmed Altera devices. Test vectors can be created in waveform or text format in the MAX+PLUS II Waveform Editor or Text Editor and applied to the device; results can be viewed in waveform or text format. The MPU is available as part of the PL-ASAP2 or individually.

Ordering Code: *PL-MPU*

Programming Adapters

Altera provides three types of programming adapters for Altera devices: PLM-prefix adapters, PLE-prefix adapters, and the PLAD3-12 compatibility adapter. Each adapter contains one of the following sockets: a zero-insertion-force dual in-line package (DIP), J-lead (PLCC/JLCC), pin-grid array (PGA), small-outline integrated circuit (SOIC), or quad flat pack (QFP). The adapters for QFP devices with 100 or more pins support Altera's QFP carrier technology. Table 2 on page 572 lists the adapters required for each Altera device and package option.

See the *QFP Carrier & Development Socket Data Sheet* in this data book for more information.

PLM-Prefix Adapters

The PLM-prefix adapters plug directly into the MPU. Each adapter provides programming support for a specific device package. Additionally, PLM-prefix (except the PLMJ1213 and PLMT1064) support functional testing of programmed Altera devices. The PLMJ1213 and PLMT1064 adapters can either program the Configuration EPROMs used to configure FLEX 10K and FLEX 8000 devices or download configuration data directly to the FLEX 10K or FLEX 8000 device via the FLEX Download Cable.

PLE-Prefix Adapters

The PLE-prefix adapters plug into the PLAD3-12 compatibility adapter, which in turn plugs into the MPU. Each of these adapters provides programming support for a specific Classic device.

PLAD3-12 Compatibility Adapter

The PLAD3-12 compatibility adapter plugs directly into the MPU. This adapter allows PLE-prefix adapters to be used with the MPU.

Table 2. Programming Adapters (Part 1 of 2)

Device	Package	Adapter	BitBlaster Support
FLEX 10K	All packages	*Note (1)*	✓
FLEX 8000	All packages	*Note (1)*	✓
EPC1, EPC1V *Note (2)*	DIP J-Lead	PLMJ1213 PLMJ1213	–
EPC1064	DIP J-lead TQFP	PLMJ1213 PLMJ1213 PLMT1064	–
EPC1213	DIP J-lead	PLMJ1213 PLMJ1213	–
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280	✓
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240	✓
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240	✓
EPM9560	CQFP (208-pin) RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304	✓
EPM7032 EPM7032V EPM7032S	J-lead PQFP TQFP	PLMJ7000-44 PLMQ7000-44 PLMT7000-44	✓ *(3)*
EPM7064 EPM7064S	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100	✓ *(3)*
EPM7096 EPM7096S	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100	✓ *(3)*
EPM7128E EPM7128S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160	✓ *(3)*
EPM7160E EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160	✓ *(3)*

Table 2. Programming Adapters (Part 2 of 2)

Device	Package	Adapter	BitBlaster Support
EPM7192E EPM7192S	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160	✓ *(3)*
EPM7256E EPM7256S	PGA (192-pin) PQFP (160-pin) RQFP (208-pin)	PLMG7256-192 PLMQ7192/7256-160 PLMR7256-208	✓ *(3)*
EPX880	J-lead (84-pin) PQFP (132-pin)	*Note (4)*	✓
EPX8160	PQFP (208-pin)	PLMQ8160-208	✓
EPM5032	DIP J-lead SOIC	PLMD5032A PLMJ5032A PLMS5032A	–
EPM5064	J-lead	PLMJ5064A	–
EPM5128	J-lead PGA	PLMJ5128A PLMG5128A	–
EPM5130	J-lead PGA PQFP	PLMJ5130A PLMG5130A PLMQ5130A	–
EPM5192	J-lead PGA	PLMJ5192A PLMG5192A	–
EP6xx	DIP J-lead SOIC	PLED610 PLEJ610 PLES610	–
EP9xx	DIP J-lead	PLED910 PLEJ910	–
EP18xx	J-lead PGA	PLMJ1810 PLEG1810	–

Notes:

(1) Configuration of FLEX 10K and FLEX 8000 devices is supported by Configuration EPROMs (EPC1064, EPC1064V, EPC1213, EPC1, and EPC1V), the FLEX Download Cable, and the BitBlaster.
(2) Information on EPC1V devices is preliminary.
(3) The BitBlaster supports the in-system programmability of MAX 7000S devices.
(4) Programming support is currently provided through third-party vendors. Contact Altera Applications at (800) 800-EPLD for additional information.

Ordering Codes: *PLExxxx, PLMxxxx, PLAD3-12*

FLEX Download Cable

The FLEX Download Cable together with the ASAP2 and either the PLMJ1213 or PLMT1064 adapter allows designers to download configuration data directly to FLEX 10K or FLEX 8000 devices.

Ordering Code: *PL-FLDLC*

BitBlaster Serial Download Cable

The BitBlaster serial download cable is a hardware interface to a standard RS-232 port on either a PC or UNIX workstation that provides configuration data to FLEX 10K, FLEX 8000, and FLASHlogic devices and programming data to MAX 9000, MAX 7000S, and FLASHlogic devices.

The 25-pin female port on the BitBlaster connects to an RS-232 port with a standard serial cable. The 10-pin female plug on the BitBlaster connects to a device on a circuit board via a 10-pin male header. The BitBlaster contains status lights that indicate the state of the device configuration or programming. Refer to the *BitBlaster Serial Download Cable Data Sheet* in this data book for more information

Ordering Code: *PL-BITBLASTER*

For information on the FLASHlogic Download Cable (PL-FLDLC), see the *BitBlaster Serial Download Cable Data Sheet* in this data book.

Programming Support

Altera customers can create a device programming environment or add to their existing device programming support with the hardware shown in Table 3.

Table 3. Programming Hardware Requirements

If you have . . .	And you want to program . . .	Then you need . . .
No programming hardware	EP610 EP910 EP1810 (PGA)	PL-ASAP2, PLAD3-12 adapter, appropriate programming adapters
No programming hardware	EP1810 (J-lead) Any MAX 5000 device Any MAX 7000 device Any MAX 9000 device Any Configuration EPROM	PL-ASAP2, appropriate programming adapters
LP6 Logic Programmer card	EP610 EP910 EP1810 (PGA)	PL-MPU, PLAD3-12 adapter, appropriate programming adapters
LP6 Logic Programmer card	EP1810 (J-lead) Any MAX 5000 device Any MAX 7000 device Any MAX 9000 device Any Configuration EPROM	PL-MPU, appropriate programming adapters
LP6 Logic Programmer card, PL-MPU Master Programming Unit	EP610 EP910 EP1810 (PGA)	PLAD3-12 adapter, appropriate programming adapters
LP6 Logic Programmer card, PL-MPU Master Programming Unit	EP1810 (J-lead) Any MAX 5000 device EPX740 EPX780 (J-lead) Any MAX 7000 device Any MAX 9000 device Any Configuration EPROM	Appropriate programming adapters

Notes:

EDA Software Support

June 1996, ver. 6

Introduction

Altera emphasizes the importance of supporting industry-standard design tools, and has established the Altera Commitment to Cooperative Engineering Solutions (ACCESS) program. Through this program, Altera and its EDA partners work together to develop either direct support for Altera devices or seamless integration with the Altera MAX+PLUS II development software.

For more information on software support provided by Altera, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

This document summarizes each ACCESS partner's design entry, compilation/synthesis, and simulation/verification products that support Altera devices directly or provide an interface to MAX+PLUS II. As shown in Table 1, Altera supplies design interface kits for several EDA tools. Altera recommends contacting EDA software manufacturers directly for details on product features, specific device support, and product availability.

This document also describes the typical design flow for Altera's interfaces to the Cadence, Mentor Graphics, Synopsys, and Viewlogic design environments. For detailed information on these four interfaces, refer to the following documents:

- *Cadence & MAX+PLUS II Software Interface Guide*
- *Mentor Graphics & MAX+PLUS II Software Interface Guide*
- *Synopsys & MAX+PLUS II Software Interface Guide*
- *Viewlogic Powerview & MAX+PLUS II Software Interface Guide*
- *Viewlogic Workview Office & MAX+PLUS II Software Interface Guide*

Table 1. Standard EDA Support for Altera Devices (Part 1 of 4)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
Accel Technologies, Inc. TEL: (619) 554-1000 FAX: (619) 554-1019	P-CAD Master Accel Schematic	✓ ✓	✓	✓ ✓
ACEO Technology TEL: (510) 656-2189 FAX: (510) 770-9937	Asyn Gatran Softwire		✓ ✓ ✓	
Acugen Software, Inc. TEL: (603) 881-8821 FAX: (603) 881-8906	AADELAY AAMAX ATGEN Test Vectors			✓ ✓ ✓ ✓
Aldec TEL: (702) 456-1222 FAX: (702) 456-1310	Active HDL Active-CAD Susie	✓ ✓	 ✓	 ✓
Cadence Design Systems, Inc. TEL: (408) 943-1234 FAX: (408) 943-0402	Composer *(1)* Concept *(1)* FPGA Designer *(1)* PIC Designer *(1)* Synergy *(1)* RapidSIM *(1)* Verilog-XL *(1)* Leapfrog VHDL *(1)* Veritime	✓ ✓ ✓ ✓	 ✓ ✓ ✓	 ✓ ✓ ✓ ✓
Chronologic Simulation TEL: (415) 965-3312 FAX: (415) 965-2705	VCS			✓
COMPASS Design Automation TEL: (408) 433-4880 FAX: (408) 434-7820	ASIC Synthesizer FPGA Optimizer		✓ ✓	
Data I/O Corp. TEL: (800) 247-5700 FAX: (206) 882-1043	ABEL Synario	✓ ✓	✓ ✓	✓ ✓
Exemplar Logic, Inc. TEL: (510) 337-3700 FAX: (510) 337-3799	Galileo Logic Explorer CORE	✓ ✓	✓ ✓	✓ ✓
Flynn Systems Corp. TEL: (603) 891-1111 FAX: (603) 891-1074	FS-High Density FS-PALibrary FS-ATG			✓ ✓ ✓

Table 1. Standard EDA Support for Altera Devices (Part 2 of 4)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
Front Line TEL: (408) 456-0222 FAX: (408) 456-0265	Pure Speed			✓
Harmonix TEL: (617) 935-8335 FAX: (617) 935-8530	Parthenon		✓	
IK Technology Co., Ltd. (Japan) TEL: (81) 3-3464-5551 FAX: (81) 3-3464-5689	Galahad	✓	✓	✓
IKOS Systems TEL: (408) 255-4567 FAX: (408) 366-8699	Voyager			✓
i-Logix TEL: (508) 682-2100 FAX: (508) 682-5995	Express V-HDL	✓		✓
ISDATA GmbH (Germany) TEL: (49) 721/75 10 87 FAX: (49) 721/75 26 34	LOG/iC Hint	✓ ✓	✓	
Logic Modeling Corp. TEL: (503) 690-6900 FAX: (503) 690-6906	SmartModel PLD-Debug			✓ ✓
Logical Devices, Inc. TEL: (800) 331-7766 FAX: (305) 428-1811	CUPL	✓	✓	✓
Mentor Graphics Corp. TEL: (503) 685-7000 FAX: (503) 685-7704	FPGA Station *(1)* Design Architect *(1)* AutoLogic II *(1)* Autologic Optimizer QuickSim II *(1)* QuickHDL *(1)* QuickPath *(1)*	✓ ✓ ✓ ✓	✓ ✓ ✓	✓ ✓ ✓ ✓
MINC Inc. TEL: (719) 590-1155 FAX: (719) 590-7330	PLDesigner-XL	✓	✓	✓
Model Technology TEL: (503) 641-1340 FAX: (503) 526-5410	V-System/VHDL V-System/VLOG			✓ ✓

Table 1. Standard EDA Support for Altera Devices (Part 3 of 4)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
OrCAD Systems Corp. TEL: (503) 671-9500 FAX: (503) 671-9501	PLD MOD SDT VST	✓ ✓ 	✓ 	✓ ✓ ✓
Quad Design TEL: (805) 988-8250 FAX: (805) 988-8259	Motive			✓
Simucad TEL: (510) 487-9700 FAX: (510) 487-9721	Silos III			✓
Sophia Systems TEL: (408) 943-9300 FAX: (408) 943-9303	Vanguard	✓		
Summit Design TEL: (503) 643-9281 FAX: (503) 646-4954	Visual-HDL	✓		
Synopsys TEL: (415) 962-5000 FAX: (415) 965-8637	HDL Compiler *(1)* Design Analyzer *(1)* Design Compiler *(1)* FPGA Compiler *(1)* DesignWare *(1)* VSS DesignTime *(1)*		✓ ✓ ✓ ✓ ✓ 	 ✓ ✓
Synplicity Inc. TEL: (415) 961-4962 FAX: (415) 961-4974	Synplify		✓	
Vantage Analysis Systems TEL: (510) 659-0901 FAX: (510) 659-0129	Optium			✓
Veda (formerly GenRad) TEL: (800) 600-VEDA FAX: (408) 970-0174	Vulcan System HILO			✓ ✓
VeriBest Corp. (formerly Intergraph) TEL: (800) 837-4237 FAX: (303) 581-9973	VeriBest Design Capture VeriBest Graphic HDL VeriBest HDL VeriBest FPGA/CPLD VeriBest Verilog VeriBest VHDL	✓ ✓ 	 ✓ ✓ 	 ✓ ✓

Table 1. Standard EDA Support for Altera Devices (Part 4 of 4)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
Viewlogic Systems, Inc. TEL: (508) 480-0881 FAX: (508) 480-0882	WorkView Office	✓		✓
	Powerview	✓		✓
	ViewDraw *(1)*	✓		
	ViewPLD	✓		
	ViewSynthesis *(1)*		✓	
	ViewSim *(1)*			✓
	Speedwave *(1)*			✓
	ViewTrace *(1)*			✓
	Quad Motive *(1)*			✓
	VCS			✓
Vista Technologies TEL: (708) 706-9300 FAX: (708) 706-9317	DesignVision	✓		
	Vista Model Creator	✓		
	VHDL Developer Plus	✓		

Note:
(1) Design interface kits are available from Altera.

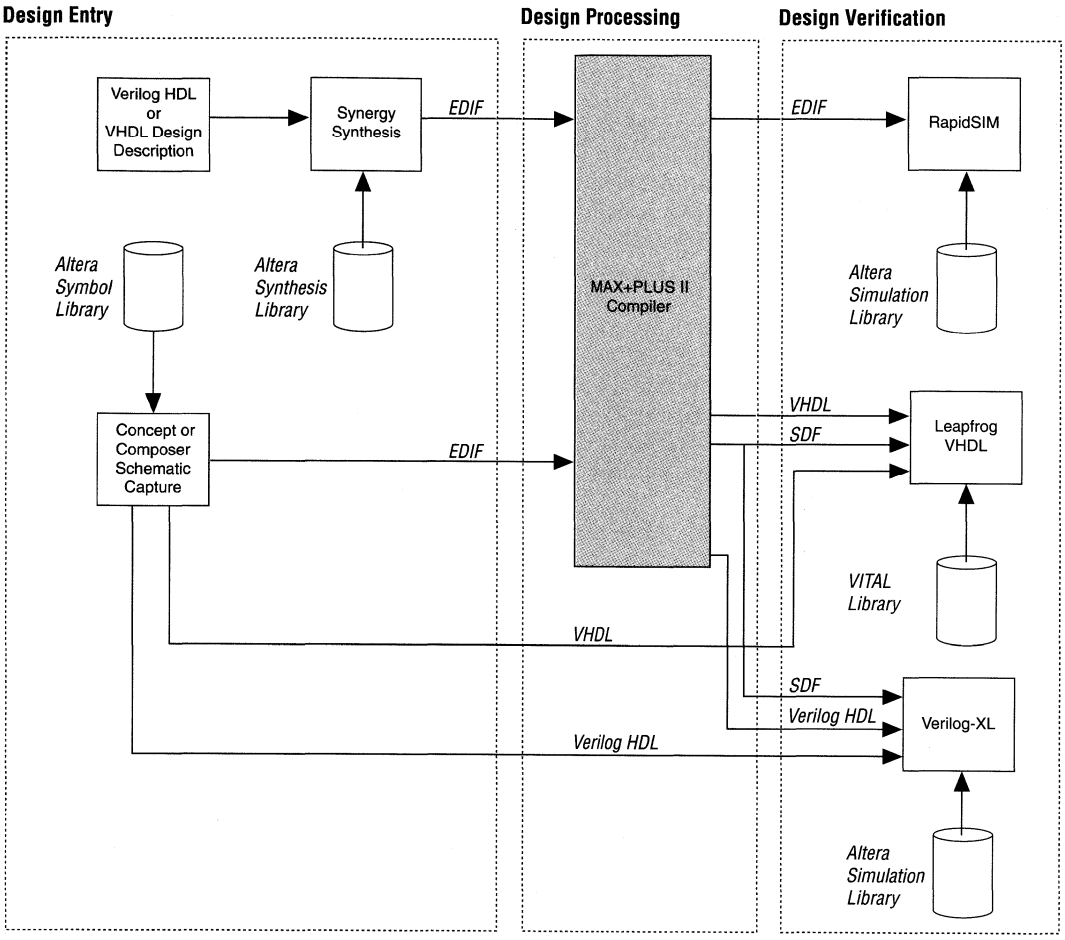
Altera/Cadence Interface

The MAX+PLUS II development software fully supports the Cadence Logic Workbench and Design Framework II design environments. By combining Cadence design entry, synthesis, and verification tools with MAX+PLUS II, designs can be implemented in any Altera programmable logic device (PLD).

The Altera/Cadence interface supports a top-down or mixed-level design methodology. Designs can be entered as a mixture of schematics, VHDL, and Verilog HDL. Schematics are entered with Cadence Concept or Composer schematic capture tools using basic gates, macrofunctions, library of parameterized modules (LPM) symbols (Concept only), and TTL symbols from the symbol libraries supplied by Altera and Cadence. Device resource assignments entered in the schematic are interpreted by MAX+PLUS II. Assignments can also be entered in MAX+PLUS II for all designs using Assign menu commands and the MAX+PLUS II Floorplan Editor. VHDL and Verilog HDL descriptions are synthesized and optimized by the Cadence Synergy synthesis tool and mapped to Altera devices with a technology library supplied by Altera. The design is saved in EDIF format and is then processed by the MAX+PLUS II Compiler, which provides architecture-specific logic synthesis, optimization, and device fitting.

To ensure that a post-routed design is correct and meets customer performance requirements, the MAX+PLUS II Compiler generates timing-annotated Verilog HDL and VHDL netlist files for verification with Cadence Verilog-XL and Leapfrog VHDL simulators. MAX+PLUS II also generates standard EDIF netlist files that contain timing information for simulation with the Cadence RapidSIM simulator. See Figure 1 for a typical design flow.

Figure 1. Design Flow between Altera & Cadence



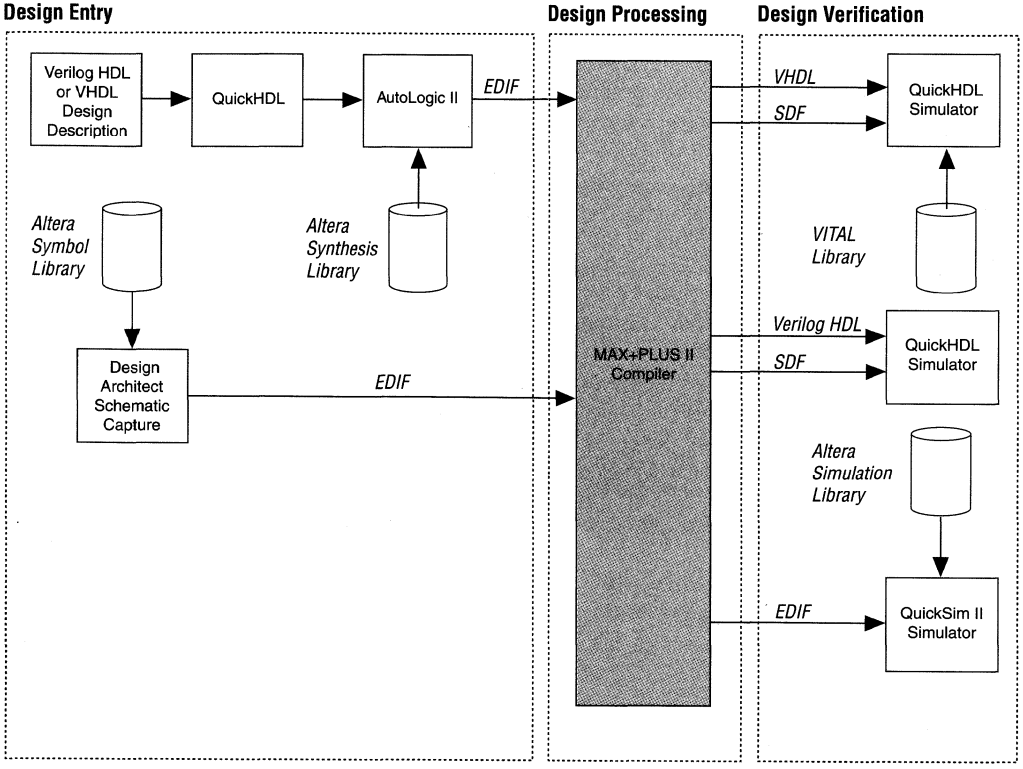
Altera/Mentor Graphics Interface

The MAX+PLUS II software is fully integrated into the Mentor Graphics Falcon Framework. By combining Mentor Graphics design entry, synthesis, and verification tools with MAX+PLUS II, designs can be implemented in any of the Altera PLDs.

The Altera/Mentor Graphics design flow supports a top-down or mixed-level design methodology. Designs can be entered as a mixture of schematics and VHDL. Schematics are entered in the Mentor Graphics Design Architect using familiar basic gates, macrofunctions, LPM, and TTL symbols from a symbol library provided by Altera. Device and resource assignments entered in the schematic are interpreted by MAX+PLUS II. Assignments can also be entered in MAX+PLUS II for all designs using Assign menu commands and the MAX+PLUS II Floorplan Editor. VHDL or Verilog HDL design descriptions are synthesized and optimized by the Mentor Graphics AutoLogic tool and mapped with an Altera synthesis library to Altera devices. The design is saved in EDIF format and is then processed by the MAX+PLUS II Compiler, which provides architecture-specific logic synthesis, optimization, and device fitting.

To ensure that a post-routed design is correct and meets customer performance requirements, the MAX+PLUS II Compiler generates timing-annotated VHDL and Verilog HDL netlist files for verification with the Mentor Graphics QuickHDL simulator. MAX+PLUS II also generates timing-annotated industry-standard EDIF netlist files that, combined with the Altera-provided simulation library, support the Mentor Graphics QuickSim II simulator. See Figure 2 for a typical design flow.

Figure 2. Design Flow between Altera & Mentor Graphics



Altera/ Synopsys Interface

SYNOPSYS®

The MAX+PLUS II software fully supports the Synopsys design environment. The Altera/Synopsys interface brings high-level design methodology to high-density programmable logic. This interface contains Altera synthesis and simulation libraries, which describe logic functions that can be used to implement designs in Altera PLDs. With these libraries, the Synopsys Design Compiler or FPGA Compiler can synthesize VHDL or Verilog HDL design descriptions to target any of the Altera PLDs.

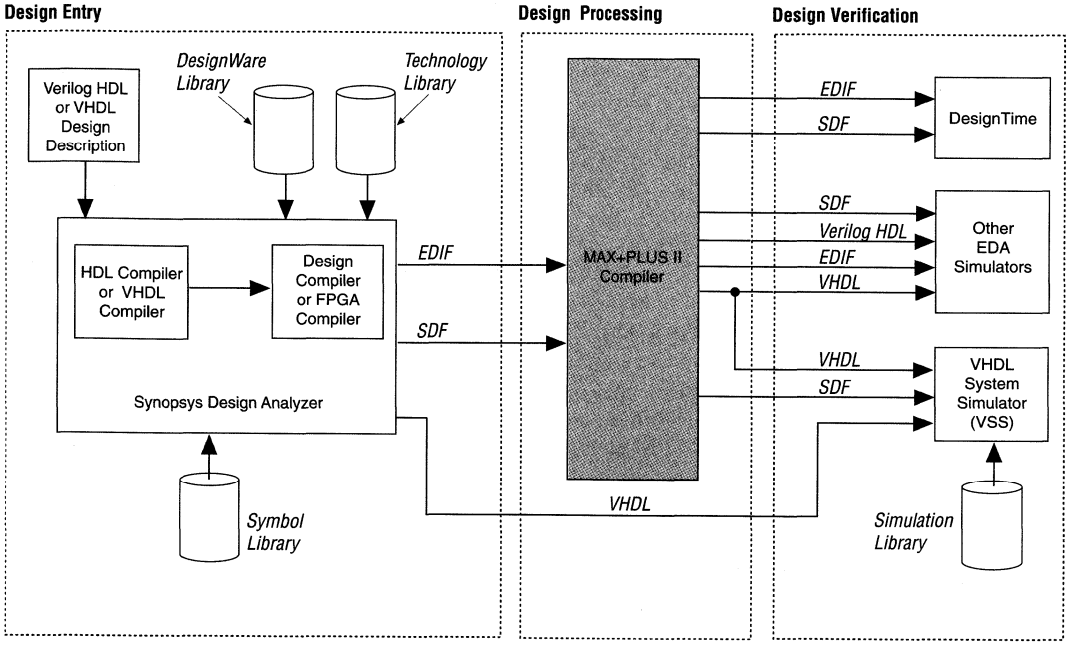
Designs are synthesized to meet user-specified area and timing goals. Design timing constraints entered in the Design Compiler or FPGA Compiler are automatically interpreted by the MAX+PLUS II Compiler, providing integration between design concept and implementation. Assignments can also be entered in MAX+PLUS II for all designs using Assign menu commands and the MAX+PLUS II Floorplan Editor. In addition, a Design Ware library is supplied for the Altera FLEX 10K and FLEX 8000 family of devices, offering area optimization and higher performance. The design is saved in EDIF format and is then processed by the MAX+PLUS II Compiler, which provides architecture-specific logic synthesis, optimization, and device fitting.

To ensure that a post-routed design is correct and meets customer performance requirements, the MAX+PLUS II Compiler generates either:

- Timing-annotated VHDL netlist files for verification with the Synopsys VHDL System Simulator (VSS)
- Timing-annotated Verilog or EDIF netlist files for verification with industry-standard simulators

MAX+PLUS II also generates post-routed EDIF netlist files for timing analysis with DesignTime. See Figure 3 for a typical design flow.

Figure 3. Design Flow between Altera & Synopsys



Altera/ Viewlogic Interface

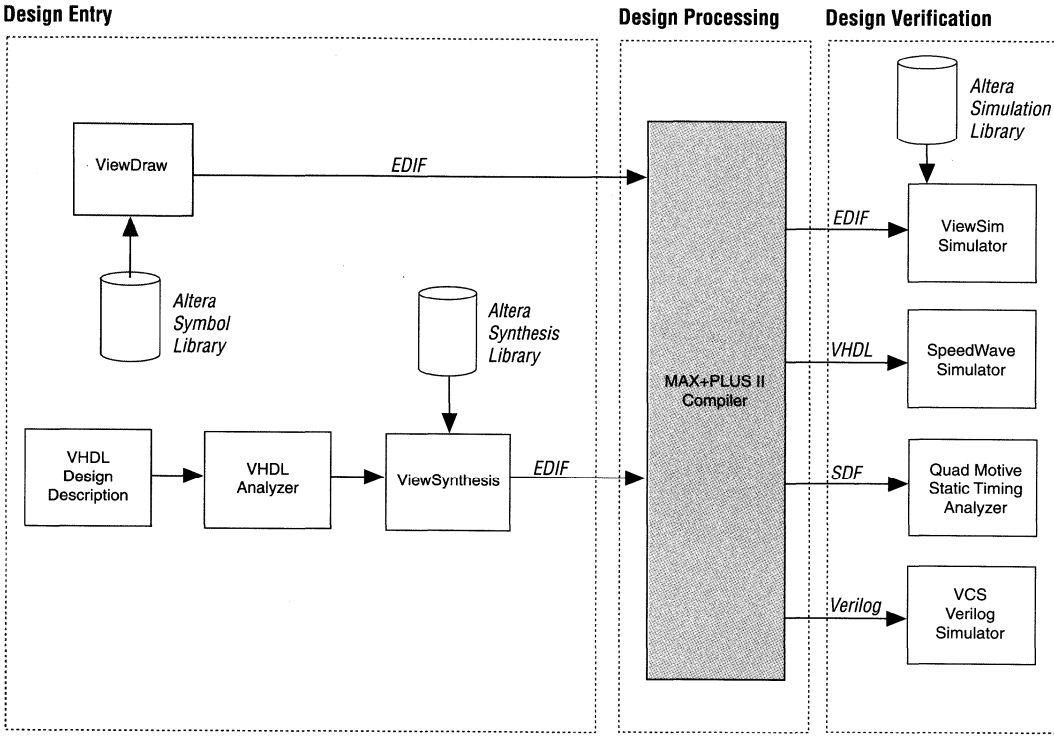
VIEWlogic

The MAX+PLUS II software is fully integrated into Viewlogic Powerview, and Workview Office product families, supporting both workstation and PC platforms. By combining Viewlogic design entry, synthesis, and verification tools with MAX+PLUS II, designs can be implemented in any of the Altera PLDs.

The Altera/Viewlogic design flow supports a top-down or mixed-level design methodology. Designs can be entered as a mixture of schematics, VHDL, and ABEL. Schematics are entered in Viewlogic ViewDraw using LPM symbols, gates, macrofunctions, and TTL functions from both Viewlogic- and Altera-supplied symbol libraries. Device resource assignments entered in the schematic are interpreted by MAX+PLUS II. Assignments can also be entered in MAX+PLUS II for all designs using Assign menu commands and the MAX+PLUS II Floorplan Editor. VHDL descriptions are synthesized by Viewlogic ViewSynthesis and mapped with an Altera-supplied technology library to Altera devices. The design is saved in EDIF format and is then processed by the MAX+PLUS II Compiler, which provides architecture-specific logic synthesis, optimization, and device fitting.

To ensure that a post-routed design is correct and meets customer performance requirements, the MAX+PLUS II Compiler generates timing-annotated EDIF netlist files for verification with the ViewSim simulator and for timing analysis with the Quad Motive Static Timing Analyzer. See Figure 4 for a typical design flow.

Figure 4. Design Flow between Altera & Viewlogic



Notes:

Programming Hardware Manufacturers

June 1996, ver. 3

Introduction

Table 1 lists the manufacturers that offer programming hardware support for Altera devices. Altera recommends contacting manufacturers directly for up-to-date details on product features, specific device support, and product availability.

Table 1. Programming Hardware Manufacturers (Part 1 of 3)

Manufacturer	Address	Telephone	Fax
Advin Systems, Inc.	1050 E. Duane Avenue, Suite L Sunnyvale, CA 94086	(408) 243-7000	(408) 736-2503
American Advantech	750 East Arques Avenue Sunnyvale, CA 94086	(408) 245-6678	(408) 245-8268
Ando Electric Co. Ltd.	19-7 Kamata, 4-Chome Ota-ku, Tokyo 144 Japan	(81) 33 733 1161	(81) 33 739 7310
Aval Data Corp.	Shinyuri 21, Bldg 6F, 2-2, 1-Chome, Manpukuji Asao-Ku, Kawasaki-City, Kanagawa 215 Japan	(81) 44 952 1311	(81) 44 952 1331
B & C Microsystems, Inc.	750 N. Pastoria Avenue Sunnyvale, CA 94086	(408) 730-5511	(408) 730-5521
BP Microsystems	1000 N. Post Oak Road, Suite 225 Houston, TX 77055-7237	(713) 688-4600	(713) 688-0920
Bytek Corp.	543 NW 77th Street Boca Raton, FL 33487-1323	(407) 994-3520	(407) 994-3615
Celectronic GmbH	Nordichstraße, 63-65 D-13406 Berlin 1 Germany	(49) 3041 3607 5	(49) 3041 3607 8
Cornelius Consult	Am Siepen 17 D-4630 Bochum 1 Germany	(49) 2343 6120 6	(49) 2343 5669 2
Data I/O Corp.	P.O. Box 97046 Redmond, WA 98073-9746	(206) 881-6444	(206) 882-1043
EE Tools	544 Weddell Drive, Suite 6 Sunnyvale, CA 94089	(408) 734-8184	(408) 734-8185

Table 1. Programming Hardware Manufacturers (Part 2 of 3)

Manufacturer	Address	Telephone	Fax
Elan Digital Systems Limited, U.K.	Elan House, Little Park Farm Road Segensworth West Fareham, Hants PO15 5SJ United Kingdom	(44) 1489 579799	(44) 1489 577516
ertec GmbH	St. Johann 10 D-91058 Erlangen Germany	(49) 9131 7557 0	(49) 9131 7557 10
HAMIS Haase, Menrad & Co. GmbH	Büssinghof/Böcklerstraße 219 D-3300 Braunschweig Germany	(49) 531 79231	(49) 531 74020
ICE Technical, Ltd.	Station Buildings, Penistone South Yorks S30 GHG United Kingdom	(44) 1226 767404	(44) 1226 370434
Instronic Peripherals & Systems	No. 471, 1st Floor, E.S.I. Road, II Block, Rajajinagar Bangalore 560 010 India	(91) 80 3304636	(91) 80 3304636
Leap Electronic Co., Ltd.	6F-4, No. 4, Lane 609, Sec. 5, Chung Hsin Road, San Chung City, Taipei Hsein Taiwan	(886) 2 999 1860	(886) 2 999 0015
Link Computer Graphics, Inc.	369 Passaic Avenue, Suite 100 Fairfield, NJ 07004	(201) 808-8990	(201) 808-8786
Logical Devices, Inc.	130 Capitol Drive Golden, CO 80401	(305) 279-6868 (800) 331-7766	(305) 279-6869
MicroPross	33 rue Gantois Lille 59000 France	(33) 20 15 11 33	(33) 20 15 11 66
Minato Electronics	3628 Madison Avenue, #5 North Highlands, CA 95660	(916) 348-6066	(916) 348-0926
Needham's Electronics, Inc.	4630 Beloit Drive, Suite 20 Sacramento, CA 95838	(916) 924-8037	(916) 924-8065
Oliver Advanced Engineering	1146 North Central, #380 Glendale, CA 91202	(818) 240-0080	(818) 240-6131
Owen Electronic GmbH	Fritz-Wunderlich-Straße 51 D-6798 Kusel Germany	(49) 6381 4202 0	(49) 6381 4202 85
Prologic Systems	557-0 Burbank Street Broomfield, CO 80020	(303) 460-0103	(303) 469-5565

Table 1. Programming Hardware Manufacturers (Part 3 of 3)

Manufacturer	Address	Telephone	Fax
SMS Holding GmbH	IM Grund 15 D-88239 Wangen Germany	(49) 7522 9728 0	(49) 7522 9728 50
Stag Programmers, LTD	Silver Court, Watchmead Welwyn Garden City, Herts AL71LT United Kingdom	(44) 1707 332148	(44) 1707 371503
Sunrise Electronic, Inc.	675 Brea Canyon Road, #6 Walnut, CA 91789	(909) 595-7774	(909) 594-7009
Sunshine Electronics Co., Ltd.	Rm. 304, 3F, No. 2, Lane 137 Sec. 5 Ming Shen E. Road Taipei Taiwan	(886) 2 763 3732	(886) 2 765 4065
System General	1603A South Main Street Milpitas, CA 95036	(408) 263-6667	(408) 262-9220
Tribal Microsystems/ HiLo Systems	44388 South Grimmer Blvd Fremont, CA 94538	(510) 623-8859	(510) 623-9925
Xeltek	3563 Ryder Street Santa Clara, CA 95051	(408) 524-1932	(408) 245-7084

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Configuration Elements & Reliability

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Data Sheet

Introduction

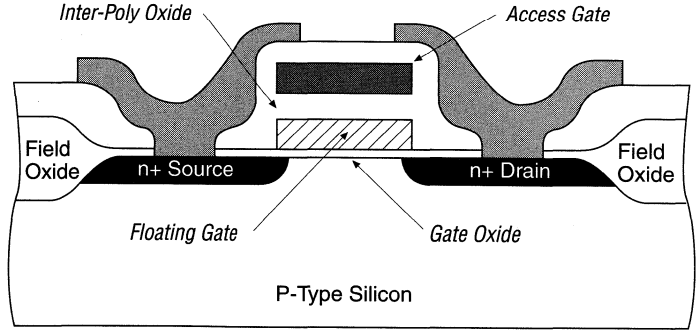
Altera's broad range of programmable logic devices (PLDs) incorporates four types of configuration elements: EPROM, EEPROM, FLASH, and SRAM. To ensure the highest level of device performance and reliability, Altera maintains a comprehensive testing program that carefully monitors the factors affecting the basic programming elements of each device. Altera maintains rigorous quality standards both before a device is put into production and throughout the manufacturing process.

EPROM Configuration Element

The EPROM transistor is a modified NMOS transistor in which the threshold voltage is easily switched between a low voltage (near V_{SS}) and a high voltage (greater than V_{CC}). The different threshold voltages represent the EPROM cell in the on and off states.

The EPROM transistor has a floating polysilicon gate between the access gate and the substrate, as shown in Figure 1. The floating gate is electrically isolated from the substrate by a thin gate oxide that is approximately 200 Å thick, and from the access gate by a thicker dielectric inter-poly oxide that typically consists of oxides and/or nitrides.

Figure 1. EPROM Cell Construction



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EPROM transistors are programmed to a high-threshold voltage with hot electron injection. When a high programming voltage (V_{PP}) is applied to the access gate of an EPROM cell, and a slightly lower voltage (V_D) is applied to its drain, electrons flow from the source to the drain. As these electrons pick up kinetic energy, their path is altered by an electric field located between the access gate and substrate. This electric field is generated by the potential difference between V_{PP} on the access gate and V_D on the drain. Electrons that achieve a kinetic energy of 3.2 eV accelerate vertically toward the floating gate, pass through the gate oxide, and are trapped on the floating-gate electrode. These electrons create a net negative voltage on the floating gate that opposes the electrical field created by the positive voltage on the access gate. The result is a substantial increase in the threshold voltage required to change the EPROM cell from a non-conducting to a conducting state. See Figure 2.

Figure 2. EPROM Cell Programming

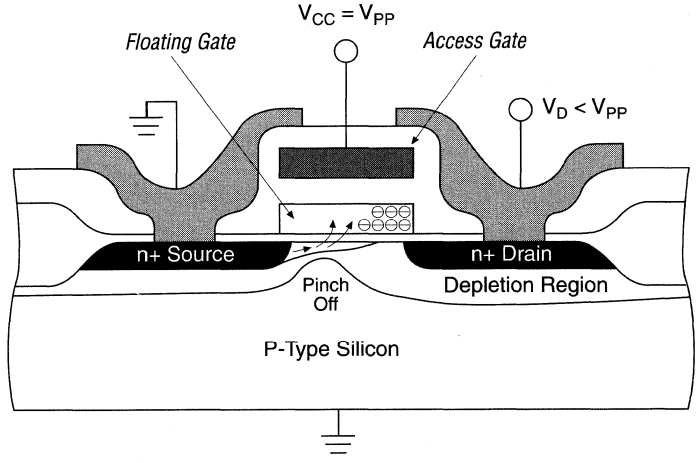
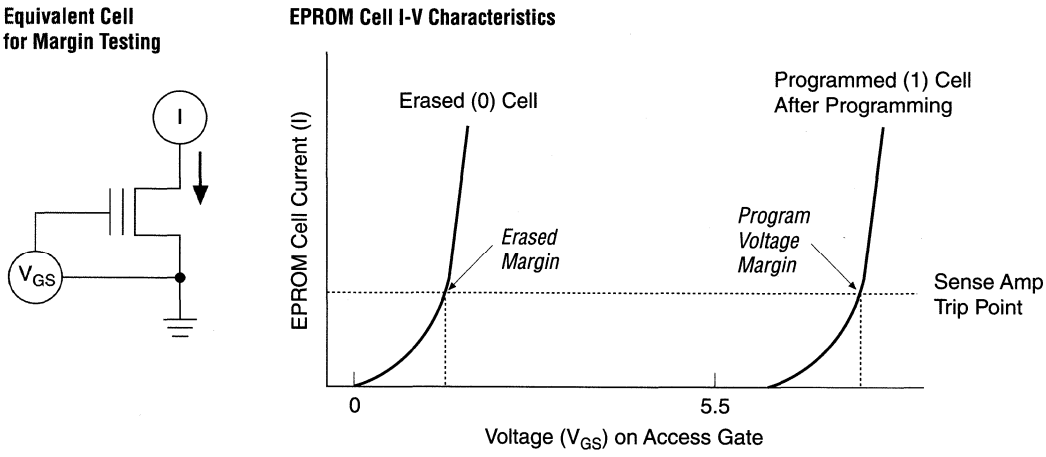


Figure 3 shows the current-voltage (I-V) relationships for programmed (high-threshold voltage) and erased (low-threshold voltage) EPROM cells. The programmed EPROM cell behaves as a transistor that is turned off, because source-drain current does not flow for access-gate voltages ranging from 0 to V_{CC}. In contrast, an erased cell produces source-drain current when its access gate is brought to approximately 1 V, like a transistor that is turned on.

Programmed EPROM cells in the off state are erased by exposing the device to ultraviolet (UV) radiation with wavelengths of 2,540 Å. The excess electrons on the floating gate absorb radiant UV energy, experience a rise in energy level above the 3.2-eV barrier, overcome the oxide-silicon potential barrier, and finally migrate into the substrate where they are neutralized.

Figure 3. Current vs. Voltage Relationships of Erased & Programmed EPROM Cells



EEPROM Configuration Element

The EEPROM transistor, like the EPROM transistor, is an MOS transistor that is either on or off, depending on the threshold voltage. Unlike EPROM devices, however, EEPROM devices can be erased electrically. The EEPROM cell consists of a single, floating polysilicon gate structure that is used to change the threshold voltage of the transistor. See Figure 4. The threshold voltage is changed when a tunneling mechanism traps an excess of electrons on the floating gate. Fowler-Nordheim tunneling occurs when the floating gate is raised to a high voltage (12 V to 13 V) via capacitive coupling to the n+ implant region. Once the electrons have been trapped on the floating gate, they present a negative shielding voltage and increase the threshold voltage of the transistor, making it impossible to turn the transistor on under normal operating voltages. This process allows the floating gate to act as an on/off switch for the read transistor.

The EEPROM cell is erased with the same tunneling mechanism as the EPROM cell. Because the electrons are removed from the floating gate, the gate has a net positive charge that allows the EEPROM transistor to be turned on or off, depending on the voltage on the control gate.

For a complete operational description of the EEPROM cell, see the *Altera Reliability Report No. 25* available from Altera Literature Services or from an Altera sales representative.

Figure 4. EEPROM Cell Construction

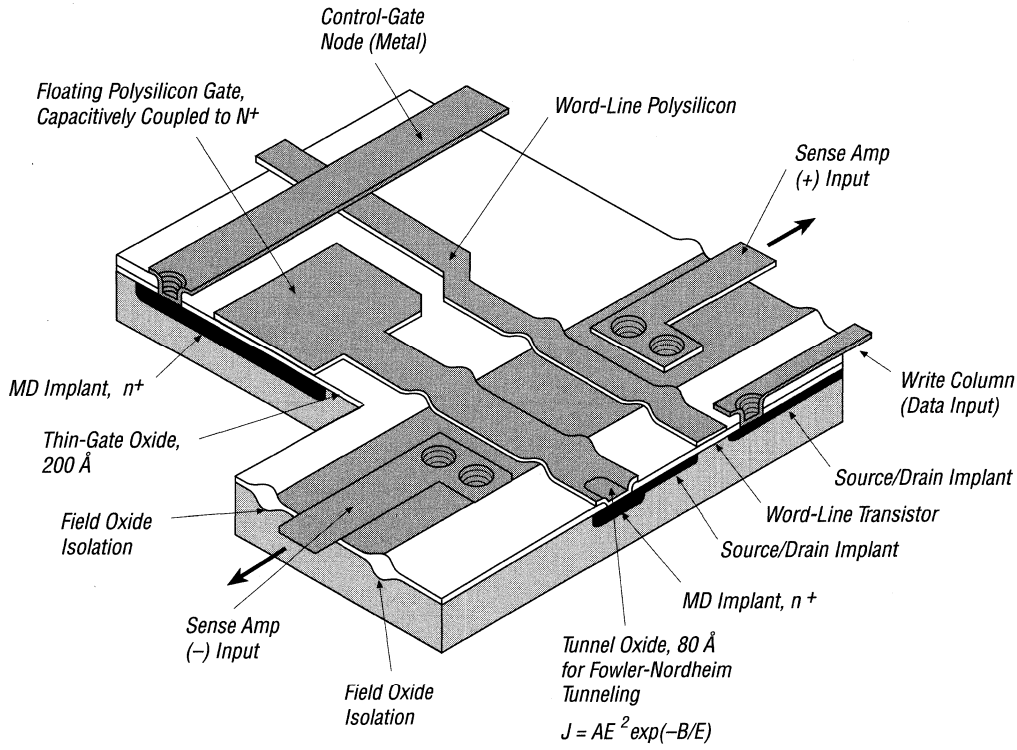
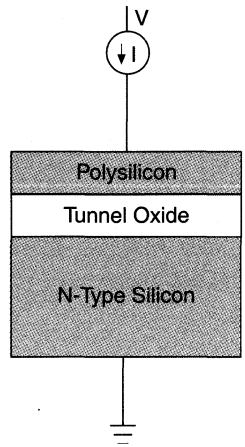


Figure 5 shows a 2-electrode structure in which one electrode is formed by polysilicon and another is formed by a heavily doped N-type silicon diffusion. These electrodes are separated by a tunnel oxide that is approximately 80 Å thick. When typical operating voltages of 5 V or less are applied across the tunnel oxide, it acts as a dielectric and does not conduct electricity. When 12 V to 14 V are applied, however, electrons tunnel through the oxide. This process is characterized by an extremely small tunneling current (less than 10^{-20} A) at typical operating voltages of 5 V or less. At the higher voltages used to erase or program the cell (i.e., charge or discharge the floating gate), the exponential rise in current produces approximately 1 µA of current flow through the tunnel oxide. Depending on the voltage's polarity, this current is sufficient to charge or discharge the cell within a few milliseconds.

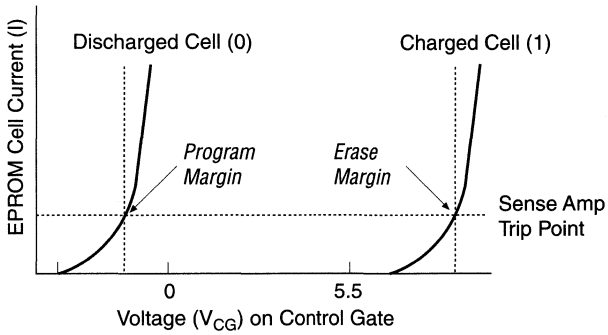
Figure 5. EEPROM Floating-Gate Electrode, Tunnel Oxide & Heavily Doped Diffusion Electrode



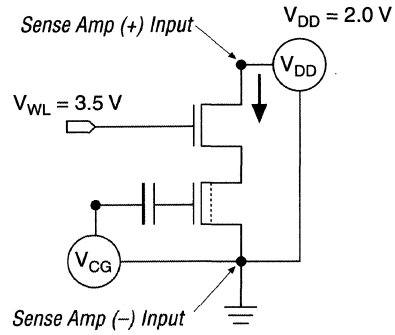
The I-V relationships for programmed and erased EEPROM cells are similar to those of EPROM cells (see Figure 6). Unlike the EPROM cell, however, the threshold voltage of a discharged EEPROM cell is negative (less than 0 V) because electrons are removed from the floating gate. Electron removal gives the floating gate a net positive charge.

Figure 6. Current vs. Voltage Relationships of Erased & Programmed EEPROM Cells

EEPROM Cell I-V Characteristics



Equivalent Circuit for Margin Testing



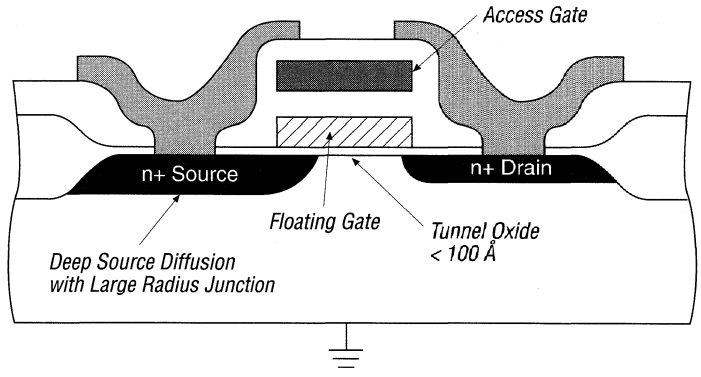
FLASH Configuration Element

The FLASH transistor, used in Altera's FLASHlogic devices, is a hybrid configuration element that combines design, manufacturing, and operational characteristics of EPROM and EEPROM configuration elements.

As shown in Figure 7, the FLASH transistor has two layers of polysilicon in a stacked gate structure that resembles the EPROM transistor. However, the transistors have different gate-oxide thicknesses and source/drain regions: the FLASH cell gate oxide is less than 100 Å thick, while the EPROM gate oxide is approximately 200 Å thick.

The source and drain diffusions of a FLASH cell are asymmetric; the source has a higher diffusion coefficient than the drain. The source-to-gate overlap is greater than the drain-to-gate overlap, causing a graded diffusion with a higher junction breakdown voltage. In contrast, the EPROM transistor has symmetric source and drain diffusions.

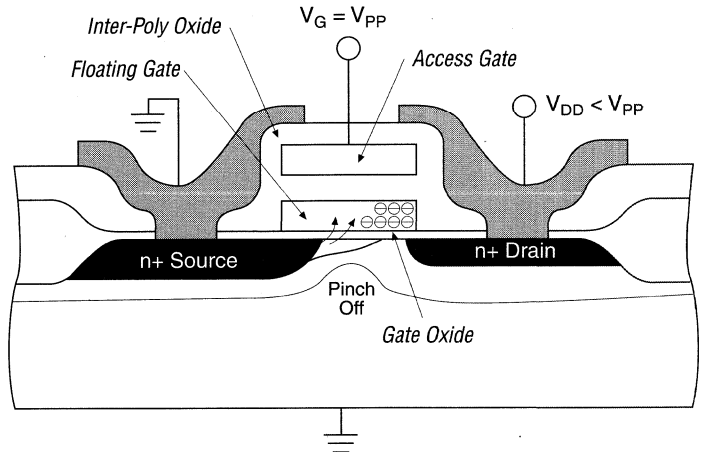
Figure 7. FLASH Configuration Element Construction



A tungsten film overlays the access gate, effectively reducing the resistivity of the second polysilicon layer and improving the performance of the device. The tungsten film does not alter FLASH cell operation.

FLASH transistors, like EPROM transistors, are programmed using hot electron injection. See Figure 8. When a high programming voltage (V_{PP}) of approximately 12 V is applied to the upper access gate, it capacitively couples the access gate to the floating gate, inverting the P-type channel below the gate and turning on the cell. When a lower voltage (V_{DD}) of 5 to 8 V is applied to the drain, it causes a large source-to-drain current, resulting in electron acceleration from the source to the drain.

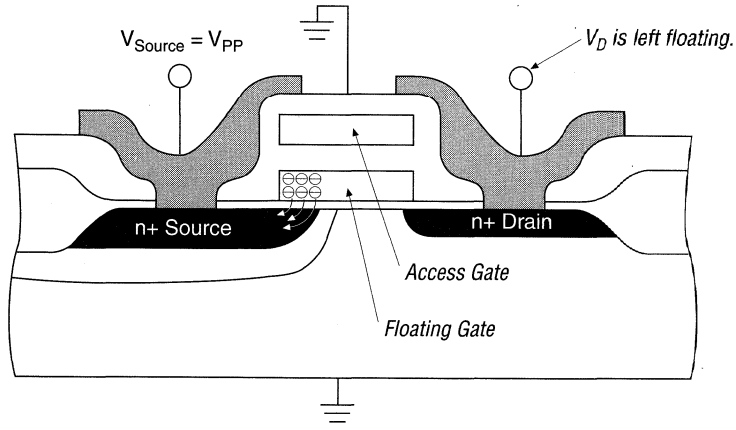
Figure 8. FLASH Configuration Element Programming Using Hot Electron Injection



An electric field, generated by the coupled access and floating gates, diverts the flow of electrons towards the gate oxide. Diverted electrons with energy greater than 3.2 eV jump through the gate oxide and are trapped on the polysilicon floating gate. When the programming voltages are removed, the electrons trapped on the floating gate raise the threshold voltage above 5.5 V, turning the cell off.

To erase the FLASH transistor, the excess electrons are removed from the floating polysilicon gate with Fowler-Nordheim tunneling, the same method used to erase EEPROM cells. The access gate is grounded, effectively grounding the floating gate, and a high programming voltage (V_{PP}) is applied to the source junction. As shown in Figure 9, this process applies a high field across the tunnel oxide between the floating gate and the graded source junction. The field, approximately 12×106 V/cm, produces a tunnel current of electrons between the floating gate and the source that discharges the cell.

Figure 9. FLASH Configuration Element Discharging Operation Using Fowler-Nordheim Tunneling

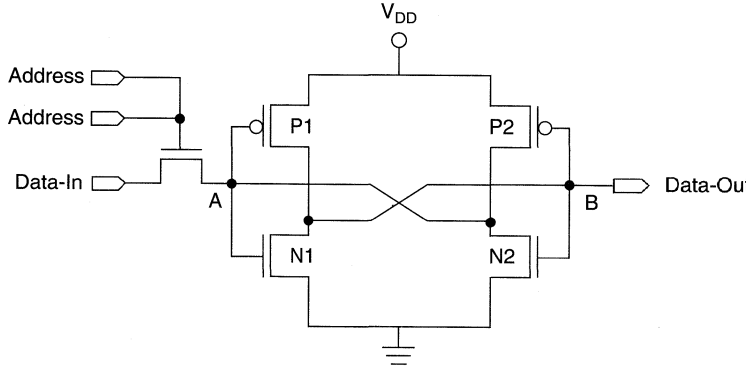


SRAM Configuration Element

The basic programming element of Altera's FLEX 10K and FLEX 8000 programmable logic devices are SRAM configuration elements. Figure 10 shows the standard CMOS five-transistor cell that comprises the configuration element.

The FLEX 10K and FLEX 8000 device manufacturing process is a subset of the EEPROM fabrication process. Therefore, all development and reliability enhancements used to manufacture EEPROM devices also apply to SRAM-based devices.

Figure 10. SRAM Configuration Element



Failure Mechanisms & Reliability Screens

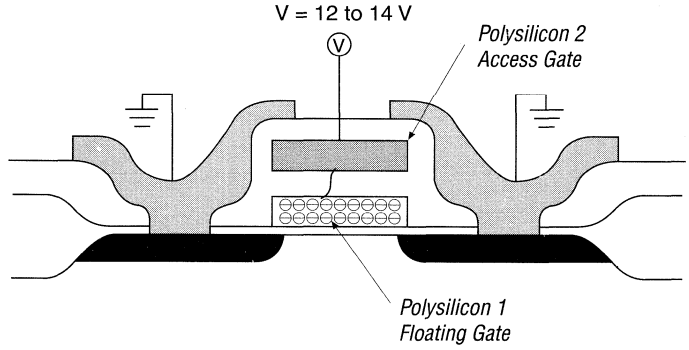
EPROM, EEPROM, and FLASH cells function through a change in threshold voltage. Reliable EPROM, EEPROM, and FLASH cells hold excess electrons placed on the floating gate, thus maintaining their charge and a high threshold voltage (transistor off) over the expected life of the device. Discharged cells maintain a low threshold voltage (transistor on), preventing electrons from moving onto the floating gate over the life of the device.

Voltage Margin Testing

Voltage margin testing is used to measure the threshold voltage of EPROM, EEPROM, or FLASH cells. This testing is essential for monitoring the ability of a device to be programmed or erased, and the long-term stability of a device after programming or erasure. Altera devices incorporate special test-mode circuitry that allows measurement of the threshold voltage (i.e., voltage margin) of each EPROM, EEPROM, or FLASH cell on a device. This circuitry is used to determine the programmability of all devices and to implement screens that detect charge loss from programmed devices. During the screening process, any degradation of the threshold voltage is measured for each cell as a function of time, temperature, and voltage. Voltage margin testing does not apply to SRAM cells because they are configured at system power-up by a Configuration EPROM or an external host.

Altera's voltage margin testing is performed during wafer-sort operations. At Wafer Sort 1, devices are tested for combinatorial and registered logic functionality and for cell programming to ensure that all EPROM, EEPROM, or FLASH cells are fully programmable. Each cell undergoes voltage-margin testing to ensure that its threshold voltage exceeds 5.5 V, the maximum V_{CC} value encountered during normal operation. Next, each cell's access gate is raised to 12 V to pull electrons off the floating gate through any defects in the inter-poly oxide between the floating and access gates. See Figure 11.

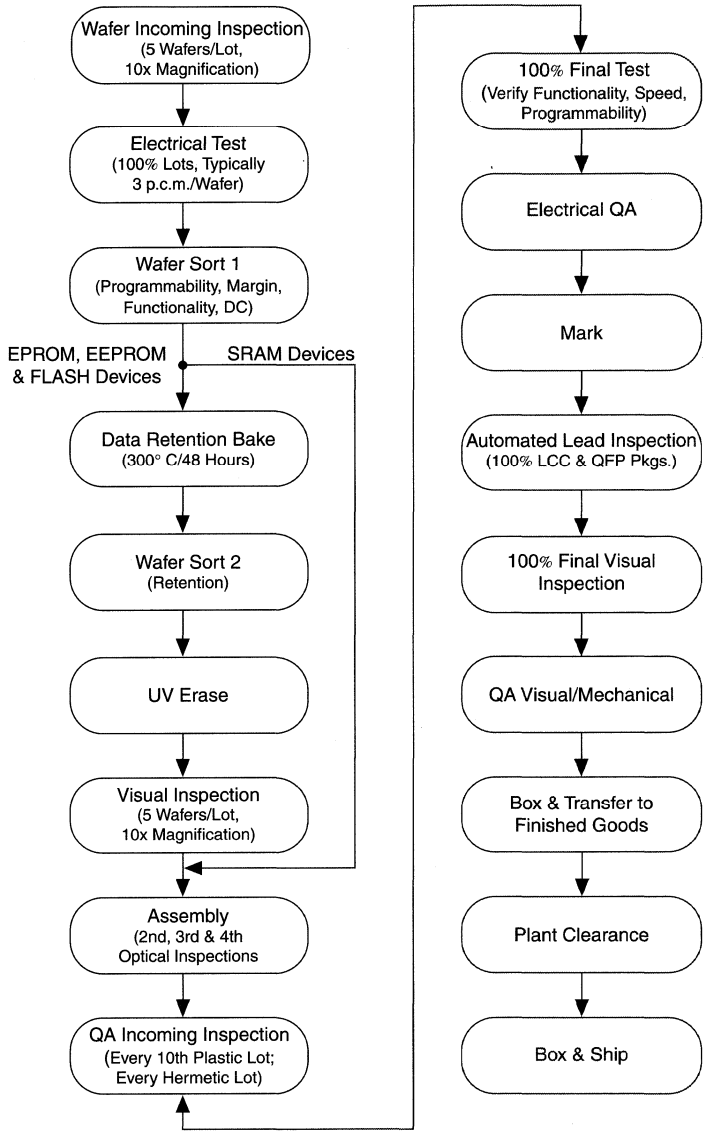
Figure 11. DC Erase Stress for EPROM, EEPROM & FLASH Configuration Elements



As shown in Figures 1, 4, and 7, the floating gates in all cells are completely surrounded by oxide. Any defect in the oxide, or contamination by mobile ionic charges such as Na^+ can cause electrons to migrate off the gate. This "cell stress," or DC erase stress, lowers the threshold voltage of cells with a defective oxide. A cell's base threshold voltage is determined by a voltage margin test performed immediately after programming and before the DC erase stress. After the DC erase stress is applied, each cell's voltage margin is tested again. If any cell shows a significant reduction in threshold voltage, the device is rejected from the manufacturing flow.

Thermally activated charge-loss mechanisms are also reliability hazards. To detect material defects, every device is baked at a high temperature with all cells in the charged state after Wafer Sort 1. Depending on the device, this bake is performed at 300° C for 12 hours or 245° C for 96 hours. After the bake, the threshold voltage for each cell is remeasured during Wafer Sort 2 and compared to its pre-bake value. Devices with cells that exhibit a reduced threshold voltage are rejected from the manufacturing flow. Additional voltage margin testing is performed on packaged devices after assembly. Figure 12 shows a typical wafer-sort process.

Figure 12. Wafer-Sort, Assembly & Final Test Flow for Altera Devices



Reliability Screening

Reliability testing is an integral part of the standard production test flow for all Altera devices. During the various wafer-sort operations, devices are screened for reliability. Voltage- and temperature-accelerated stresses are applied to activate potential charge-loss failure mechanisms within the device. To ensure the effectiveness of Altera's testing program, test results are routinely verified.

After the IC package assembly operation, during which each die is removed from the wafers and placed into packages, each device is tested and the results are compared against data sheet specifications. The test is performed at elevated temperatures to ensure that specifications are met for the maximum operating temperature: 70° C for commercial and 85° C for industrial devices.

Altera Reliability Program

Altera's integrated circuits must meet rigorous reliability standards. Altera uses a two-phase approach to ensure a consistently high level of reliability from its manufacturing processes and devices:

- New product/production process qualification
- Reliability monitoring

New Product/Production Process Qualification

Altera performs rigorous reliability tests on new devices and subjects new or substantially modified processes to a rigorous series of reliability tests before production. Tests are performed to Altera and industry standards. This qualification procedure ensures that all manufacturing processes and products meet Altera's reliability requirements.

Reliability Monitoring

Once a device or process is qualified for production, Altera routinely conducts reliability tests throughout the manufacturing life cycle. Reliability tests are conducted under the careful supervision of trained reliability engineers and technicians, and are performed to Altera, commercial, and industry standards.

Altera's Reliability Engineering Lab uses the latest equipment for reliability testing, allowing Altera engineers and technicians to perform accurate reliability qualifications and monitoring on a timely basis. This equipment provides engineers and technicians with the control and precision required to perform rigorous semiconductor stress tests.

Results from Altera's reliability monitoring program are published several times each year in the *Altera Reliability Report*. This report summarizes the test results for all Altera devices over a 15-month period. It includes detailed descriptions of the reliability tests, their implementation, and useful information about semiconductor reliability. For a copy of the *Altera Reliability Report No. 25*, contact Altera Literature Services at (408) 894-7144.

QFP Carrier & Development Socket

June 1996, ver. 10 Data Sheet

Features

- Quad flat pack (QFP) carriers protect fragile leads on QFP devices during shipping and device handling.
- QFP development sockets allow on-board electrical and mechanical prototype testing with QFP packages.
- Carriers and development sockets are available for 100-, 160-, 208-, 240-, and 304-pin devices.
- Development socket footprints are compatible with QFP footprints, providing a smooth transition from prototype to production.
- Together, carriers and sockets help prevent electrostatic damage to the devices while providing excellent AC circuit performance.

General Description

Altera QFP carriers and development sockets protect the fragile leads on QFP devices during shipping and throughout the development cycle. Each socket is designed with a lead footprint that is compatible with the device, so it can be used during both mechanical and electrical prototyping. QFP carriers and development sockets are currently available for 100-, 160-, 208-, 240-, and 304-pin QFP packages. Figure 1 shows the carrier and development socket for the 100-pin QFP device (the 160- and 208-pin QFP carriers and development sockets are similar).

Figure 1. 100-Pin QFP Carrier & Development Socket

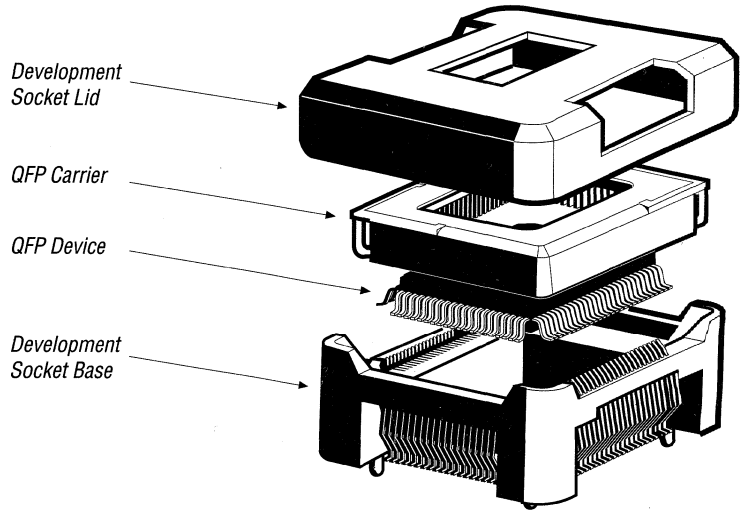


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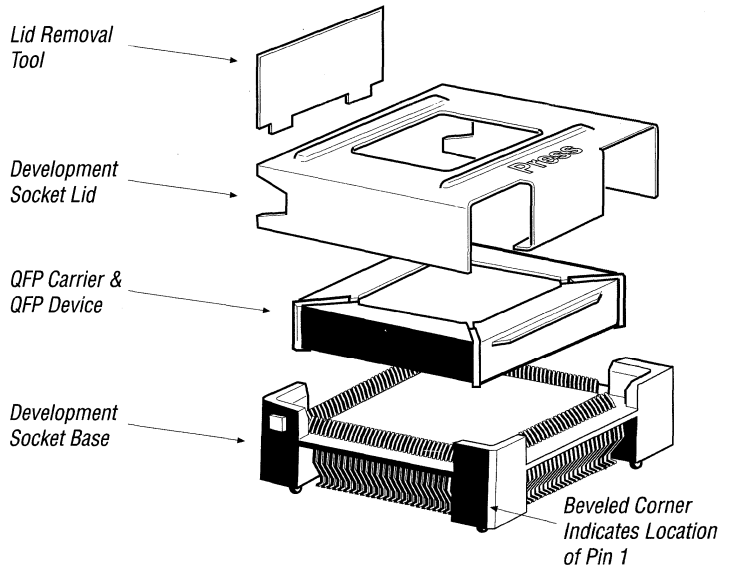
Figure 2 shows the carrier and development socket for the 240-pin QFP device (the 304-pin QFP carrier and development socket are similar).

Figure 2. 240-Pin QFP Carrier & Development Socket



QFP Carrier

The carrier is a static-dissipative, molded plastic shell that holds the QFP device in a secure frame to prevent mechanical damage to the device leads. The device is held in the carrier by recessed plastic clips (two clips on the 100-pin carrier and four clips on the 160-, 208-, 240-, and 304-pin carriers). Figure 3 shows the dimensions of the QFP carriers.

All MAX 9000, MAX 7000, and MAX 5000 QFP devices with 100 to 304 pins can be ordered in carriers, which eliminates the need to handle the delicate device leads. The devices and carriers are packaged in antistatic rails.

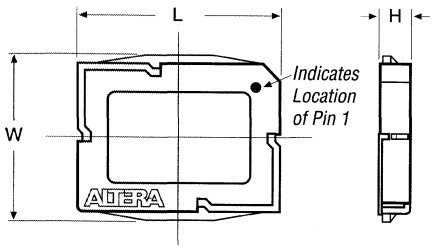
Devices can be programmed and erased while in the carrier. EPROM-based QFP devices are erased with a UV lamp; EEPROM-based QFP devices are erased electrically in a programming adapter.

☞ QFP devices without protective carriers should be handled with a vacuum wand in an electrostatically protected workplace to reduce the possibility of mechanical or electrical device damage.

Figure 3. QFP Carrier Dimensions

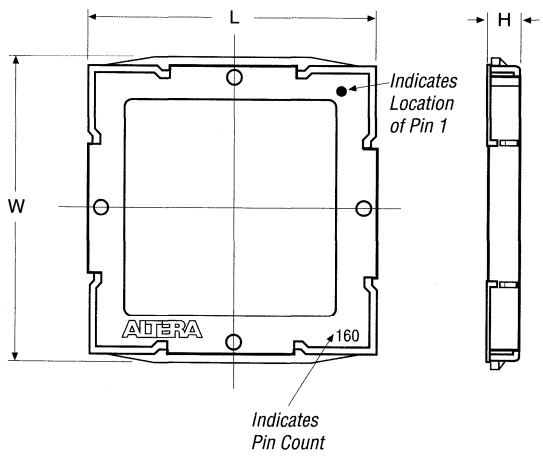
Dimensions are shown in millimeters. The carrier is rated from –65° C to 155° C, and is qualified to handle commercial and industrial operating temperatures. Illustrations are not drawn to scale.

100-Pin QFP Carrier

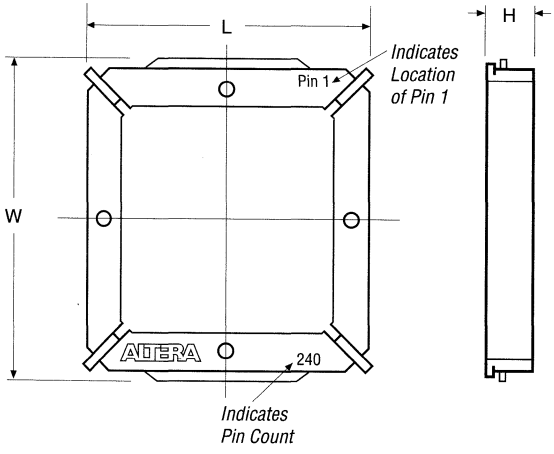


Pin Count	L	W	H
100	25.2	21.2	4.2
160	33.2	35.2	5.1
208	33.2	35.2	5.1
240	37.0	40.0	6.4
304	45.0	48.0	6.4

160- & 208-Pin QFP Carrier



240- & 304-Pin QFP Carrier



QFP Development Socket

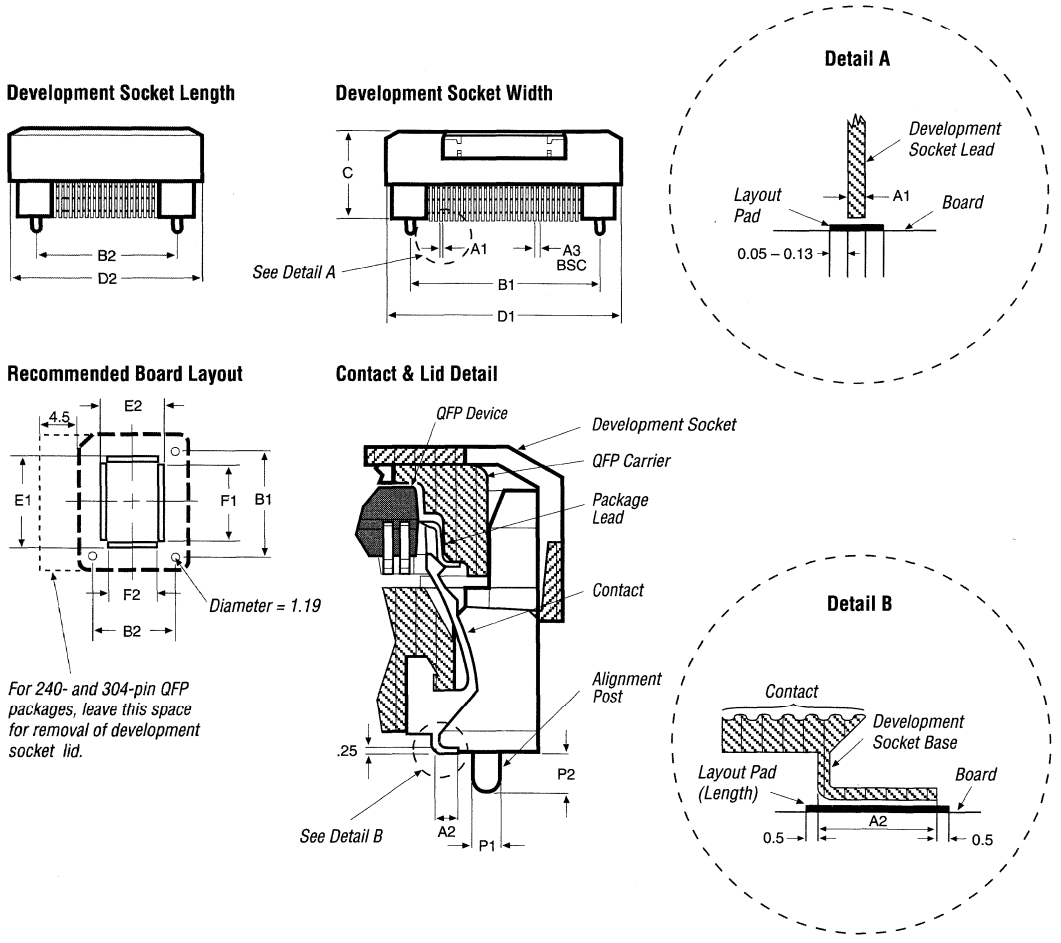
The QFP development socket footprint is compatible with the lead footprint of the QFP device. It ensures the device's electrical connection to the printed circuit board (PCB) and provides excellent AC circuit performance: low noise, low capacitance, and low inductance. Although the QFP development socket is designed to minimize noise, interconnect capacitance, and inductance, these effects can be further reduced by mounting the device directly on the PCB for production.

Altera recommends using the QFP development socket for prototyping only. Altera does not recommend using them for production builds.

Figure 4 shows the dimensions of the QFP development socket. Details A and B show the PCB pad layout length and width recommended for use with the development socket. These industry-standard pad layout dimensions are for the "gull-wing" lead that is typically found on QFP packages. The layout pad extends from 0.05 mm to 0.13 mm beyond each side of the lead width (A1), and 0.5 mm beyond each side of the lead length (A2), as shown in Details A and B, respectively. A layout pad of these dimensions is also suitable for use with QFP devices that do not use carriers. To ensure correct board layout, pad sizes must be compatible with the development socket and the QFP device leads.

Figure 4. QFP Development Socket Dimensions

Dimensions are shown in millimeters. The tolerance of all layout pad dimensions is ±0.025 mm. The continuous duty rating for the development socket is –65° C to 155° C. The carrier and development socket are qualified to handle commercial and industrial operating temperatures.



Pin Count	A1	A2	A3	B1	B2	C	D1	D2	E1	E2	F1	F2	P1	P2
100	0.20	0.93	0.65	25.00	19.00	12.00	31.51	25.54	23.63	17.63	18.85	12.35	1.00	1.50
160	0.20	0.93	0.65	33.80	33.80	12.80	39.80	39.80	32.08	32.08	25.35	25.35	1.00	1.50
208	0.20	0.93	0.50	33.80	33.80	12.80	39.80	39.80	31.68	31.68	25.50	25.50	1.00	1.50
240	0.20	0.93	0.50	34.00	34.00	14.30	44.00	42.90	35.20	35.20	29.50	29.50	1.00	1.50
304	0.20	0.93	0.50	42.00	42.00	14.30	52.00	50.90	43.30	43.30	37.50	37.50	1.00	1.50
Tolerance	±0.12	±0.12	±0.12	±0.12	±0.12	±0.40	±0.20	±0.20	±0.12	±0.12	±0.12	±0.12	±0.12	±0.12

The development socket base is designed to withstand the temperatures required by industry-standard solder reflow technology. The soldering time at the allowed maximum temperature of 220° C should be approximately 10 seconds. The soldering temperature should not increase more than 3° C per second.

To perform reflow operations, Altera recommends using 100% forced convection reflow ovens rather than infrared (IR) reflow ovens. The large thermal mass of the development socket base shields or "shadows" the solder paste from the IR radiation used in IR reflow ovens. Shadowing prevents the paste from heating and flowing properly, which causes inadequate lead contact with the circuit board and unacceptable solder joints. Ovens with 100% forced convection reflow provide the even and efficient heat transfer required to form an acceptable solder joint.

The development socket lid and the QFP carrier should not be subjected to the solder reflow process. They cannot withstand the typical reflow temperatures of 180° C to 220° C, and can be harmed by the cleaners and solvents used in the reflow process. Only the development socket base should be subjected to solder reflow. However, the socket lid and carrier are qualified to handle commercial and industrial operating temperatures.

With the appropriate solder mask, multiple development sockets can be closely spaced on the board. Three alignment posts ensure correct orientation and provide sufficient registration for reflow soldering. When other components must be placed near the development socket, the designer must make sure that component leads do not conflict with the outline of the development socket.

The socket lid holds the QFP carrier in the development socket base and braces the carrier by pressing the QFP device leads against the electrical contacts in the socket base. The contact material in the development socket base is a beryllium copper with a tin/lead plating. These contacts connect the device leads to the PCB, ensuring a positive electrical connection that is not susceptible to mechanical interruption through jarring or impulsive shocks. The carrier design ensures that the pressure of the socket contacts does not significantly affect the coplanarity of the device leads. This carrier/socket combination allows the designer to perform mechanical analysis during the functional prototyping cycle.

Altera also provides a tool to extract the QFP device from the carrier. See "Extracting a Device from the QFP Carrier" on page 621 of this data sheet for complete details.

Using the QFP Carrier & Development Socket

This section gives step-by-step instructions for the following procedures:

- Inserting the QFP carrier and device into the development socket
- Removing the QFP carrier and device from the development socket
- Programming a device in the QFP carrier
- Extracting a device from the QFP carrier

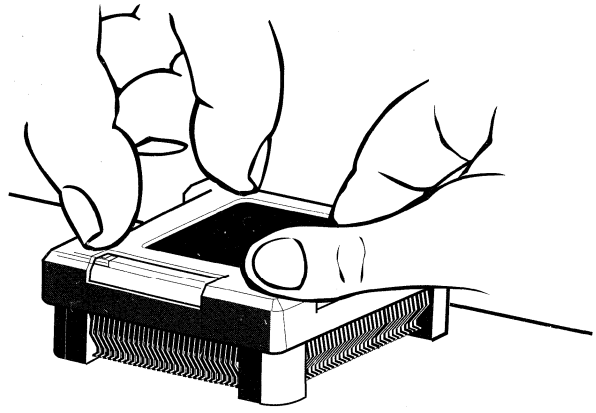
The device should be removed from the QFP carrier only after it has been programmed and is ready to be soldered onto the PCB.

Inserting the QFP Carrier & Device into the Development Socket

To insert a 100-, 160-, or 208- pin QFP carrier and device into the development socket:

1. Align the QFP carrier and device on the development socket by matching the beveled corner of the carrier to the beveled corner of the socket base and aligning the corresponding dots.
2. Place the QFP carrier and device in the development socket base.
3. Place the socket lid over the socket base and press down firmly on all four corners of the lid. Clicking sounds are clearly audible as the socket lid is pressed into place. See Figure 5.
4. Visually confirm that the tabs on all sides of the lid have locked onto the development socket base.

Figure 5. Inserting a 100-, 160-, or 208-Pin QFP Carrier & Device into the Development Socket

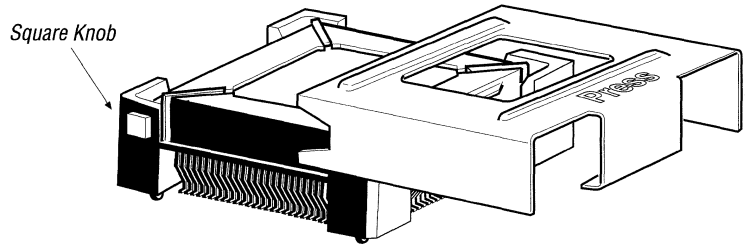


When placing the development socket lid onto or removing it from the socket base, Altera recommends bracing the side of the PCB opposite the development socket to prevent the PCB from flexing. Some insertion force is required to seat a high-pin-count device. If the PCB is not properly braced, repeated flexing of the PCB can cause excessive wear, resulting in cracks in the solder joints and in the PCB traces.

To insert a 240- or 304-pin QFP carrier and device into the development socket:

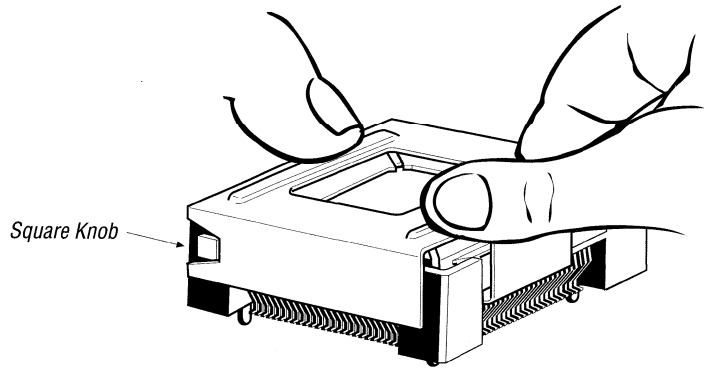
1. Align the QFP carrier and device on the development socket base by matching pin 1 of the device to pin 1 of the socket base.
2. Place the QFP carrier and device in the development socket base.
3. Align the development socket lid as shown in Figure 6.

Figure 6. Aligning a 240- or 304-Pin QFP Development Socket Lid



4. Slide the development socket lid horizontally on top of the development socket base until the lid reaches the square knobs on the sides of the socket base.
5. While pressing down on the part of the development socket lid labeled with the word "Press," slide the development socket lid until the square knobs on the socket base fit firmly in the lid. See Figure 7.

Figure 7. Sliding a 240- or 304-Pin QFP Development Socket Lid into Place



Removing the QFP Carrier & Device from the Development Socket

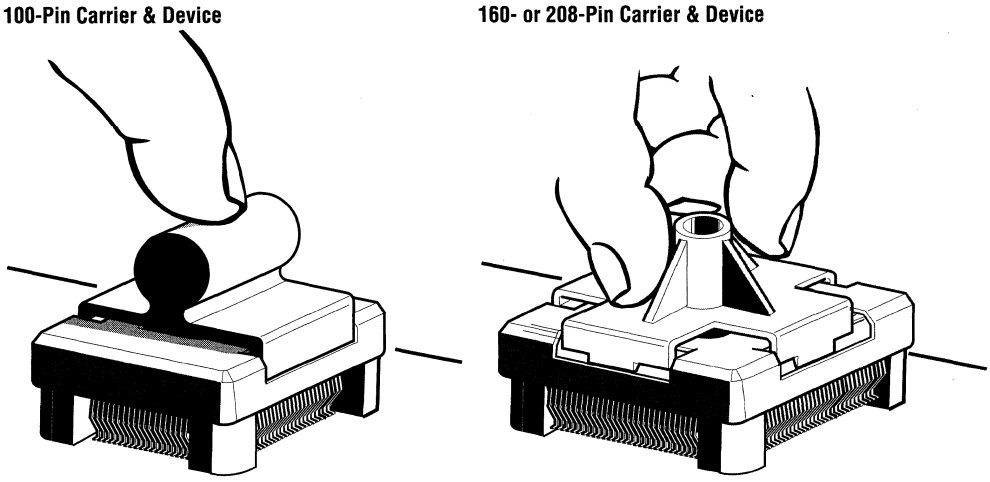
For 100-, 160-, 208-, 240-, and 304-pin packages, Altera does not recommend removing the development socket lid at temperatures below –10° C.

To remove a 100-, 160-, or 208-pin QFP carrier and device from the development socket:

1. Place the removal tool over the QFP socket lid, as shown in Figure 8.
2. Gently press down, making sure that the edges of the tool fit into the slots on the top of the lid. Clicking sounds will be clearly audible. To ensure that all four tabs of the 160- and 208-pin QFP carrier have been unlatched from the development socket base, twist the removal tool back and forth after it is pressed down.
3. While maintaining pressure, lift the lid and removal tool together.
4. Remove the QFP carrier and device.

☞ Altera recommends removing a QFP carrier and device from a development socket no more than 25 times.

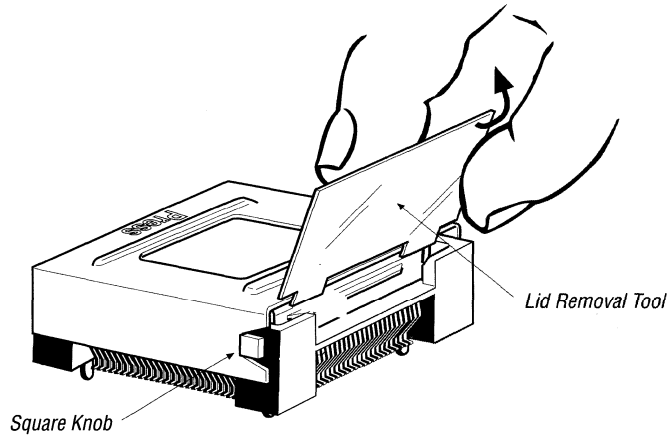
Figure 8. Removing a 100-, 160-, or 208-Pin QFP Carrier & Device from the Development Socket



To remove a 240- or 304-pin QFP carrier and device from the development socket:

1. Place the lid removal tool in the slot between the edge of the development socket lid and the edge of the development socket base. See Figure 9.

Figure 9. Removing a 240- or 304-Pin QFP Carrier & Device from the Development Socket



2. Tilt the top of the lid removal tool toward the center of the development socket until the development socket lid slides away from the square knobs on the sides of the socket base.

3. Remove the lid removal tool, slide the development socket lid back, and remove the lid from the development socket base.

Programming a Device in the QFP Carrier

QFP devices that are shipped in the protective QFP carriers are ready to be programmed with an Altera or third-party programming adapter. With Altera programming software and hardware, test vectors can be directly applied to the device for programming verification and functional testing. Devices in QFP packages can also be programmed with industry-standard programming hardware from other manufacturers.

To program a device in the QFP carrier:

1. Place the QFP carrier with the device into the programming adapter, making sure that the carrier and adapter are aligned correctly.

2. Close the retaining latch by pressing the latch against the socket. A clicking sound is clearly audible as the latch fastens over the socket.

The retaining latch on the clamshell-style programming adapter socket ensures good electrical contact between the device leads and the socket. To ensure proper programming, the retaining latch must be closed after the QFP carrier and device are placed into the programming adapter.

Extracting a Device from the QFP Carrier

Altera offers carrier extraction tools for 100-, 160-, 208-, 240-, and 304-pin devices, and recommends using the extraction tool to extract devices from QFP carriers. Table 1 shows the ordering codes for QFP carrier extraction tools.

Table 1. QFP Carrier Extraction Tools

Product	Ordering Code
100-pin QFP carrier extraction tool	PL-EXT1
160- & 208-pin QFP carrier extraction tool	PL-EXT2
240-pin QFP carrier extraction tool	PL-EXT4
304-pin QFP carrier extraction tool	PL-EXT5

The QFP device fits in the QFP carrier extraction tool only when the device is correctly oriented in the carrier insertion slot. For 100-, 160-, and 208-pin QFP devices, the pin indicator on the corner of the device (as shown in Figure 3) should be aligned with the beveled corner of the extraction tool; a sliding platform slips over the QFP device, securing it in the slot and bending back the yellow retaining clips located on the corners of the QFP carrier.

For 240- and 304-pin QFP devices, the pin indicator on the corner of the device (as shown in Figure 3) should be aligned with the pin indicator on the extraction tool. The extraction tool lid closes over the QFP device, bending back the yellow retaining clips located on all four corners of the QFP carrier. The yellow retaining clips lock in the open position.

The extraction button on the extraction tool ejects the QFP device from the carrier and places the device directly onto a QFP handling tray or onto a catch plate, which is included with the extraction tool. The catch plate included with the extraction tool for 100-pin devices holds four devices; the catch plate included with 160-, 208-, 240-, and 304-pin devices holds two devices.

The ridges on the bottom of the extraction tool help to align the extraction tool with the sides of the handling tray or catch plate. The default size of the extraction tool supports the Peak Plastic Corporation low-profile JEDEC tray listed in Table 2.

Table 2. QFP Handling Tray Part Numbers

Pin Count	Peak Part Number
100	ND-1420-2.7-0811-8
160	ND-2828-3.5-0308-8
208	ND-2828-3.5-0308-8
240	ND-3232-3.3-0308-8
304	ND-4040-3.8-0206-8

A multi-device extraction tool is available for use in production environments. This tool extracts up to six QFP devices at a time into low-profile JEDEC trays. Contact Altera Customer Marketing at (408) 894-7104 for more information.

To extract a 100-, 160-, or 208-pin QFP device from the carrier using the extraction tool:

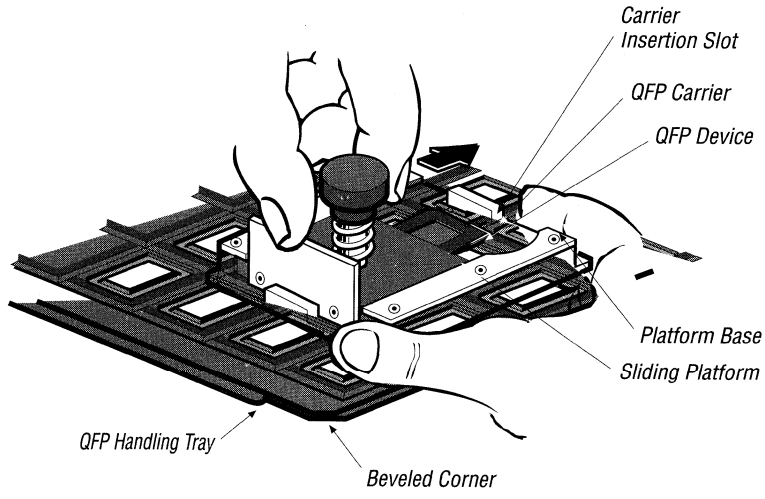
1. Align the ridges on the bottom of the extraction tool with the sides of an empty slot on the QFP handling tray. To ensure proper device orientation, align the beveled corner of the extraction tool with the beveled corner of the QFP handling tray. If a handling tray is not available, place the extraction tool over the catch plate provided.

2. Open the extraction tool by moving the sliding platform until the carrier insertion slot is completely exposed.

3. Place the carrier-protected QFP device into the carrier insertion slot. Align the beveled edge of the carrier with the beveled edge of the carrier insertion slot, and make sure that the carrier is flush with the platform base.

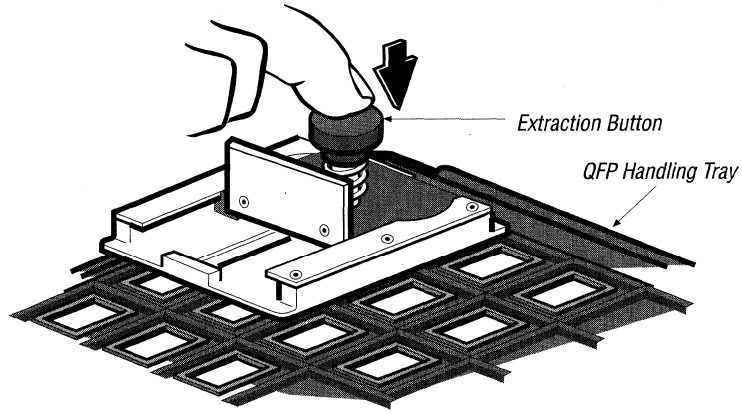
4. Move the sliding platform until it completely covers the QFP device. See Figure 10.

Figure 10. Placing a 100-, 160-, or 208-Pin QFP Carrier & Device in the Extraction Tool



5. With the QFP device completely covered, press down on the extraction button to release the QFP device from the carrier. Place it in the QFP handling tray or on the catch plate. See Figure 11. If a handling tray or a catch plate is not available, use a vacuum wand or other handling tool to move the QFP devices.

Figure 11. Pressing the Extraction Button to Remove a 100-, 160-, or 208-Pin QFP Device from the QFP Carrier



To extract a 240- or 304-pin QFP device from the carrier using the extraction tool:

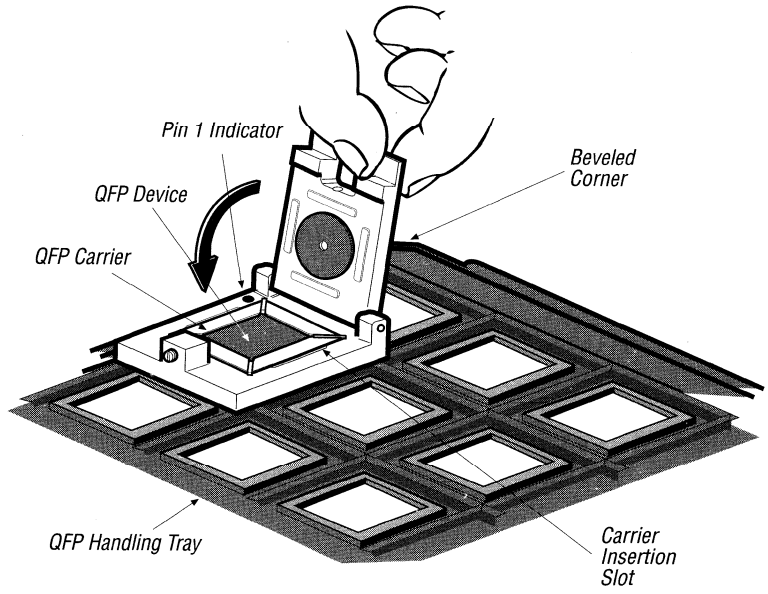
1. Place the extraction tool over the QFP handling tray by lining up the ridges on the bottom of the extraction tool with the sides of an empty slot. To ensure proper device orientation, align the pin indicator on the extraction tool with the beveled corner of the QFP handling tray. If a handling tray is not available, place the extraction tool over the catch plate provided.

2. Open the extraction tool by lifting the lid upwards and back until the carrier insertion slot is completely exposed.

3. Place the carrier-protected QFP device into the carrier insertion slot. Align the pin indicator on the corner of the carrier with the pin indicator on the corner of the extraction tool.

4. Lower the extraction tool lid down until it is completely closed over the QFP device. See Figure 12.

Figure 12. Placing a 240- or 304-Pin QFP Carrier & Device in the Extraction Tool



5. With the QFP device completely covered, press down on the extraction button to release the QFP device from the carrier and place it in the QFP handling tray or on the catch plate. If a handling tray or a catch plate is not available, use a vacuum wand or other handling tool to move the QFP devices.

Notes:

Altera Device Package Information

June 1996, ver. 6 Data Sheet

Introduction

This data sheet provides the following package information for all Altera devices:

- Lead materials
- Thermal resistance
- Package weights
- Package outlines

In this data sheet, packages are listed in ascending pin count order.

Lead Materials

Table 1 shows the available package types, lead materials, and lead finishes for all Altera device packages.

Table 1. Altera Device Lead Materials

Package Type	Package Code	Lead Material	Lead Finish *Note (1)*
Ceramic dual in-line	D	Alloy 42	Solder dip
Plastic dual in-line	P	Copper	Solder plate
Ceramic J-lead chip carrier	J	Alloy 42	Solder dip
Plastic J-lead chip carrier	L	Copper	Solder plate
Ceramic pin-grid array	G	Alloy 42	Gold over nickel plate
Plastic small-outline integrated circuit	S	Copper	Solder plate
Ceramic quad flat pack	W	Alloy 42	Tin plate: 100-pin commercial Solder dip: 208-pin
Plastic quad flat pack	Q	Copper	Solder plate
Plastic thin quad flat pack	T	Copper	Solder plate
Power quad flat pack	R	Copper	Solder plate
Plastic ball-grid array	B	Tin-lead alloy (63/37)	–

Note:
(1) Solder dip: 60/40 typical. Solder plate: 85/15 typical.

Thermal Resistance

Tables 2 through 8 provide θ_{JA} (junction-to-ambient thermal resistance) and θ_{JC} (junction-to-case thermal resistance) values for Altera FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices.

Table 2. Thermal Resistance of FLEX 10K Devices *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPF10K10	84	PLCC	11	35	23	18	14
	144	TQFP	9	42	35	32	30
	208	PQFP	7	35	24	18	14
EPF10K20	208	RQFP	2	18	12	9	7
	240	RQFP	2	20	13	10	8
EPF10K30	208	RQFP	2	18	12	9	7
	240	RQFP	2	20	13	10	8
	356	BGA	*Note (2)*	*Note (2)*	*Note (2)*	*Note (2)*	*Note (2)*
EPF10K40	208	RQFP	2	18	12	9	7
	240	RQFP	2	20	13	20	8
EPF10K50	240	RQFP	2	20	13	10	8
	356	BGA	*Note (2)*	*Note (2)*	*Note (2)*	*Note (2)*	*Note (2)*
	403	PGA	**3**	**12**	**10**	**9**	**8**
	403	PGA, *Note (3)*	**3**	**10**	**8**	**7**	**6**
EPF10K70	240	RQFP	2	20	13	10	8
	503	PGA	**1**	**8**	**7**	**6**	**4**
EPF10K100	503	PGA	**1**	**8**	**7**	**6**	**4**
	503	PGA, *Note (3)*	**1**	**6**	**5**	**4**	**3**
	503	PGA, *Note (4)*	**1**	**2**	n/a	n/a	n/a

Notes:
(1) Bold type designates measured values.
(2) For more information, contact Altera Applications at (800) 800-EPLD.
(3) Measured with pin-fin heat sink.
(4) Measured with motor-driven fan heat sink.

Table 3. Thermal Resistance of FLEX 8000 Devices *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPF8282A	84	PLCC	**11**	**35**	**23**	**18**	**14**
EPF8282AV	100	TQFP	**10**	**44**	**38**	**34**	**31**
EPF8452A	84	PLCC	**11**	**35**	**23**	**18**	**14**
	100	TQFP	**10**	**44**	**38**	**34**	**31**
	160	PQFP	**7**	**35**	**26**	**20**	**16**
	160	PGA	**6**	**20**	**13**	**10**	**8**
EPF8636A	84	PLCC	**11**	**35**	**23**	**18**	**14**
	160	PQFP	**6**	**20**	**13**	**10**	**8**
	192	PGA	**6**	**16**	**11**	**8**	**6**
	208	PQFP	7	35	24	18	14
	208	RQFP	**2**	**18**	**12**	**9**	**7**
EPF8820A	144	TQFP	9	42	35	32	30
	160	PQFP	**6**	**20**	**13**	**10**	**8**
	192	PGA	**6**	**16**	**11**	**8**	**6**
	208	PQFP	7	35	24	18	14
	208	RQFP	**2**	**18**	**12**	**9**	**7**
	225	BGA	**6**	**28**	**19**	**14**	**11**
EPF81188A	208	PQFP	7	35	24	18	14
	232	PGA	**2**	**14**	**10**	**7**	**5**
	240	RQFP	**2**	**20**	**13**	**10**	**8**
EPF81500A	240	RQFP	**2**	**20**	**13**	**10**	**8**
	280	PGA	**2**	**14**	**10**	**7**	**5**
	304	RQFP	**1**	**20**	**13**	**10**	**8**

Note:
(1) Bold type designates measured values.

Table 4. Thermal Resistance of MAX 9000 Devices *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPM9320	84	PLCC	**11**	**35**	**23**	**18**	**14**
	208	RQFP	**2**	**18**	**12**	**9**	**7**
	280	PGA	**2**	**14**	**10**	**7**	**5**
EPM9400	84	PLCC	**11**	**35**	**23**	**18**	**14**
	208	RQFP	**2**	**18**	**12**	**9**	**7**
	240	RQFP	**2**	**20**	**13**	**10**	**8**
EPM9480	208	RQFP	**2**	**18**	**12**	**9**	**7**
	240	RQFP	**2**	**20**	**13**	**10**	**8**
EPM9560	208	RQFP	2	18	12	9	7
	240	RQFP	**2**	**20**	**13**	**10**	**8**
	280	PGA	**2**	**14**	**10**	**7**	**5**
	304	RQFP	**1**	**20**	**13**	**10**	**8**

Note:
(1) Bold type designates measured values.

Table 5. Thermal Resistance of MAX 7000 Devices *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPM7032	44	PLCC	**9**	**52**	45	41	36
EPM7032S		PQFP	**18**	**63**	55	48	43
		TQFP	**19**	**64**	56	50	45
EPM7032V	44	PLCC	**9**	**52**	45	41	36
		TQFP	**19**	**64**	56	50	45
EPM7064	44	PLCC	**11**	**35**	**23**	**18**	**14**
EPM7064S		TQFP	**10**	**44**	**38**	**34**	**31**
	68	PLCC	**12**	**44**	33	25	20
	84	PLCC	**11**	**35**	**23**	**18**	**14**
	100	PQFP	**11**	**50**	43	38	34
EPM7096	68	PLCC	**12**	**44**	33	25	20
EPM7096S	84	PLCC	**11**	**35**	**23**	**18**	**14**
	100	PQFP	**11**	**50**	43	38	34
EPM7128E	84	PLCC	**11**	**35**	**23**	**18**	**14**
EPM7128S	100	TQFP	10	44	38	34	31
		PQFP	**11**	**50**	43	38	34
	160	PQFP	**7**	**35**	**26**	**20**	**16**
EPM7160E	84	PLCC	**11**	**35**	**23**	**18**	**14**
EPM7160S	100	PQFP	**11**	**50**	43	38	34
	160	PQFP	**7**	**35**	**26**	**20**	**16**
EPM7192E	160	PGA	**6**	**20**	**13**	**10**	**8**
EPM7192S		PQFP	**7**	**35**	**26**	**20**	**16**
EPM7256E	160	PQFP	**7**	**35**	**26**	**20**	**16**
EPM7256S	192	PGA	**6**	**16**	**11**	**8**	**6**
	208	RQFP	**2**	**18**	**12**	**9**	**7**

Note:
(1) Bold type designates measured values.

Table 6. Thermal Resistance of FLASHlogic Devices *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air
EPX780	84	PLCC	**11**	**35**
	132	QFP	**11**	**40**
EPX880	84	PLCC	**11**	**35**
	132	PQFP	**11**	**40**
EPX8160	208	PQFP	**7**	**35**

Note:
(1) Bold type designates measured values.

Table 7. Thermal Resistance of MAX 5000 Devices *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W)
EPM5032	28	CerDIP	**12**	**44**
		PDIP	**19**	**48**
		JLCC	**9**	**69**
		PLCC	**10**	**59**
		SOIC	**18**	**68**
EPM5064	44	JLCC	**15**	**62**
		PLCC	**9**	**52**
EPM5128	68	JLCC	**11**	**39**
		PLCC	**12**	**44**
		PGA	**2**	**32**
EPM5130	84	JLCC	**4**	**30**
		PLCC	**11**	**35**
	100	CQFP	**11**	**50**
		PQFP	**10**	**50**
		PGA	**4**	**26**
EPM5192	84	JLCC	**4**	**30**
		PLCC	**11**	**35**
		PGA	**2**	**27**

Note:
(1) Bold type designates measured values.

Table 8. Thermal Resistance of Classic Devices *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W)
EP610	24	CerDIP	**10**	**60**
		PDIP	**18**	**55**
		SOIC	**17**	**77**
	28	PLCC	**13**	**74**
EP610I	24	CerDIP	**18**	**60**
		PDIP	**22**	**67**
	28	PLCC	**16**	**64**
EP910	40	CerDIP	**12**	**40**
		PDIP	**23**	**49**
	44	PLCC	**10**	**58**
EP910I	40	CerDIP	**17**	**44**
		PDIP	**29**	**51**
	44	PLCC	**16**	**55**
EP1810	68	JLCC	**12**	**47**
		PLCC	**13**	**44**
		PGA	**6**	**38**

Note:
(1) Bold type designates measured values.

Package Weights

Table 9 shows the package weights of Altera devices.

Table 9. Package Weights of Altera Devices (Part 1 of 2)

Pins	Package	Weight (in grams)
8	PDIP	0.5
8	CerDIP	1.4
20	CerDIP	3.2
20	SOIC	*Note (1)*
24	CerDIP	4.1
24	PDIP	1.7
24	SOIC	*Note (1)*
28	SOIC	*Note (1)*
28	PLCC	1.1
28	JLCC	*Note (1)*
28	PDIP	2.0
28	CerDIP	4.5
32	TQFP	*Note (1)*

Table 9. Package Weights of Altera Devices (Part 2 of 2)

Pins	Package	Weight (in grams)
40	PDIP	6.0
40	CerDIP	13.2
44	PLCC	2.3
44	JLCC	2.8
44	PQFP	*Note (1)*
44	TQFP	0.3
68	PGA	10.4
68	JLCC	7.1
68	PLCC	4.6
84	PLCC	6.8
84	JLCC	10.9
84	PGA	10.6
100	PQFP	1.6
100	CQFP	2.1
100	PGA	14.2
100	TQFP	0.5
132	PQFP	4.4
144	TQFP	*Note (1)*
160	PQFP	5.4
160	PGA	19.9
192	PGA	24.1
208	PQFP	*Note (1)*
208	RQFP	10.8
208	CQFP	8.5
225	BGA	*Note (1)*
232	PGA	25.5
240	RQFP	15.1
240	PQFP	*Note (1)*
280	PGA	29.5
304	RQFP	26.3
403	PGA	29.5
503	PGA	59.0

Note:
(1) For more information, contact Altera Applications at (800) 800-EPLD.

Package Outlines

Package outlines are listed in ascending pin count order. Altera package outlines meet the requirements of *JEDEC Publication No. 95*. Table 10 lists the JEDEC package outlines that are used with Altera devices.

Table 10. JEDEC Package Outline Cross Reference (Part 1 of 2) *Note (1)*

Pins	Package	JEDEC Outline
8	CerDIP	MO-058
8	PDIP	MO-095
20	CerDIP	MO-058
20	SOIC	MS-013
24	CerDIP	MO-058
24	PDIP	MO-095
24	SOIC	MO-013
28	SOIC	MO-013
28	PLCC	MO-018
28	JLCC	MO-087
28	PDIP	MO-095
28	CerDIP	MO-058
32	TQFP	MO-136
40	PDIP	MO-095
40	CerDIP	MO-058
44	PLCC	MO-018
44	JLCC	MO-087
44	PQFP	MO-108
44	TQFP	MO-136
68	PGA	MO-067
68	JLCC	MO-087
68	PLCC	MO-018
84	JLCC	MO-087
84	PLCC	MO-018
84	PGA	MO-067
100	PQFP	MO-108
100	TQFP	MO-136
100	CQFP	*Note (1)*
100	PGA	MO-067
132	PQFP	MO-069
144	TQFP	MO-136
160	PQFP	MO-108
160	PGA	MO-067

Table 10. JEDEC Package Outline Cross Reference (Part 2 of 2) Note (1)		
Pins	**Package**	**JEDEC Outline**
192	PGA	MO-067
208	PQFP	MO-143
208	RQFP	MO-143
208	CQFP	*Note (1)*
225	BGA	MO-151
232	PGA	MO-067
240	RQFP	MO-143
240	PQFP	MO-143
280	PGA	MO-067
304	RQFP	MO-143
403	PGA	–
503	PGA	–

Note:
(1) For more information, contact Altera Applications at (800) 800-EPLD.

Table 11 summarizes the maximum lead coplanarity for Altera J-lead and QFP packages.

Table 11. Maximum Lead Coplanarity for J-Lead & QFP Packages	
Package	**Maximum Lead Coplanarity**
Ceramic J-lead packages (JLCC)	0.006 inches (0.15 mm)
Plastic J-lead packages (PLCC)	0.004 inches (0.10 mm)
Ceramic QFP packages (CQFP)	0.004 inches (0.10 mm)
Plastic QFP packages (PQFP) with lead pitch of 0.65 mm or greater	0.004 inches (0.10 mm)
Plastic QFP packages (PQFP) with lead pitch of 0.5 mm	0.003 inches (0.08 mm)
Ball-grid array (BGA) packages	0.006 inches (0.15 mm)

For information on device package ordering codes, see *Ordering Information* in this data book.

Package outline dimensions are shown in the following formats:

min. inches (min. millimeters)
max. inches (max. millimeters)

or:

nominal inches ± tolerance
(nominal millimeters ± tolerance)

or:

inches
(millimeters) BSC, Min., Max., Ref., Typ., R, Dia., Sq.

Table 12 shows the units used to describe package outline dimensions.

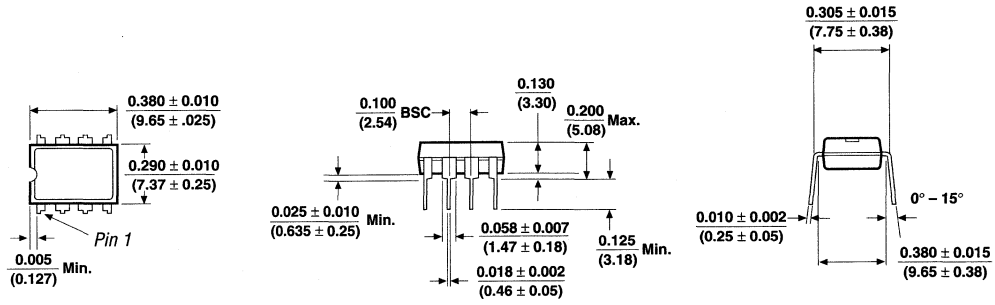
Table 12. Package Outline Units

Unit	Description
BSC	Basic. Represents theoretical exact dimension or dimension target.
Min.	Minimum dimension specified.
Max.	Maximum dimension specified.
Ref.	Reference. Represents dimension for reference use only. This value is not a device specification.
Typ.	Typical. Provided as a general value. This value is not a device specification.
R	Radius. Represents curve dimension.
Dia.	Diameter. Represents curve dimension.
Sq.	Square. Indicates a square feature for a package with equal length and width dimensions.

The following figures show the package outlines for all Altera devices.

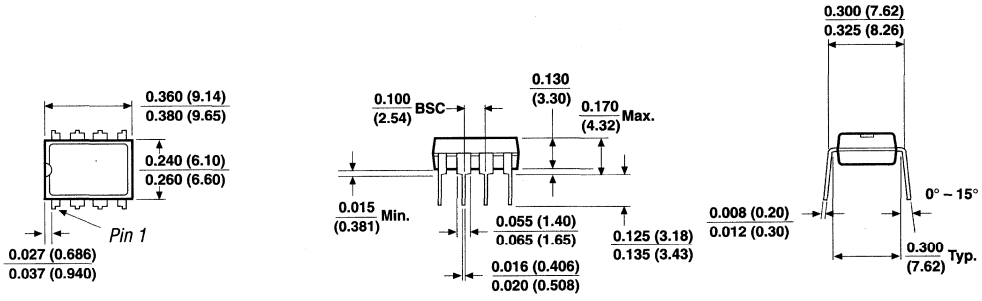
8-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



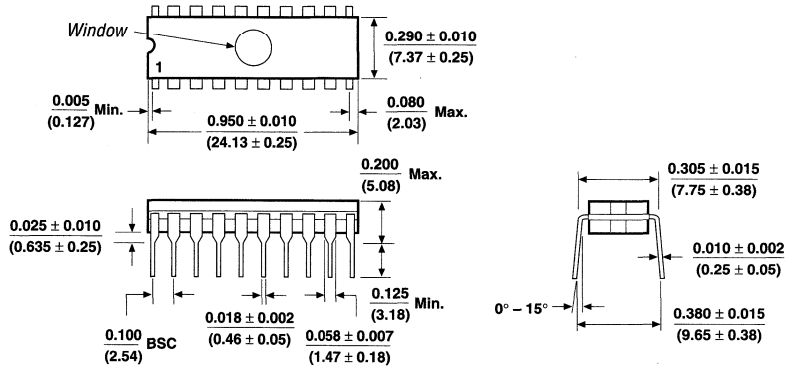
8-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



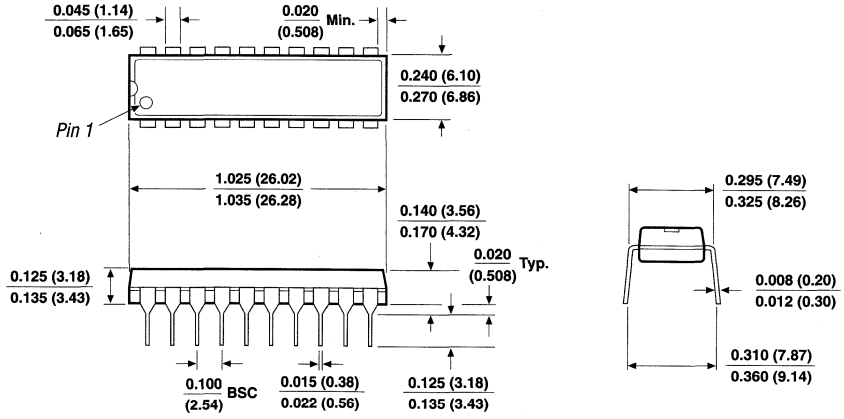
20-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



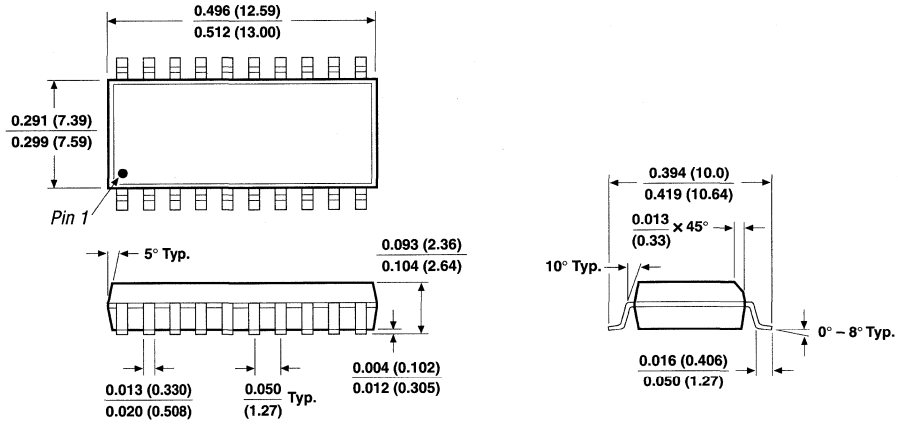
20-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



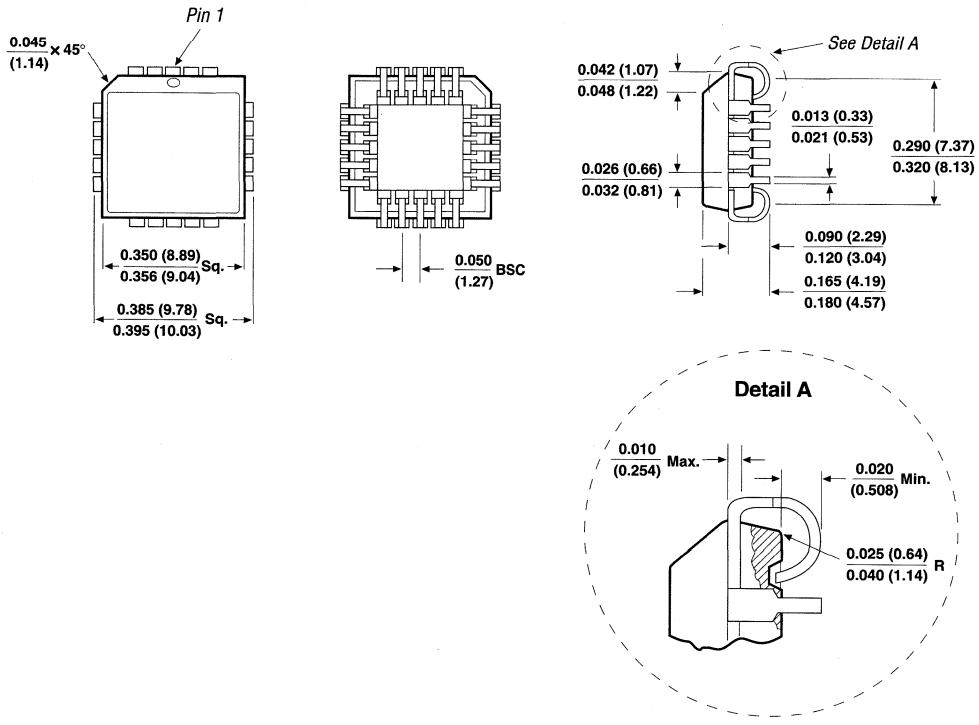
20-Pin Plastic Small-Outline Integrated Circuit (SOIC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



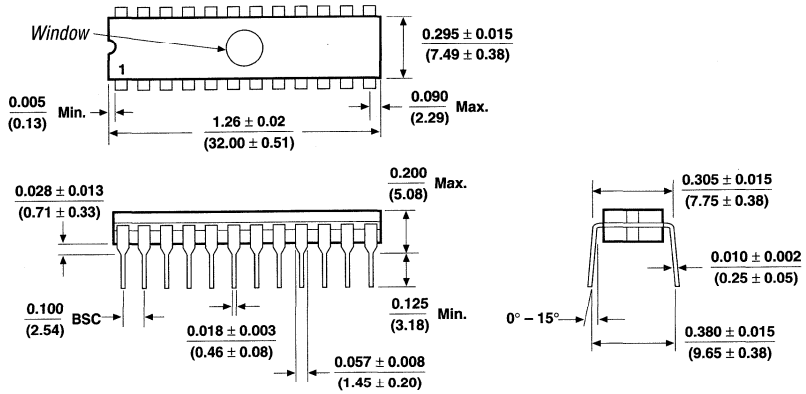
20-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



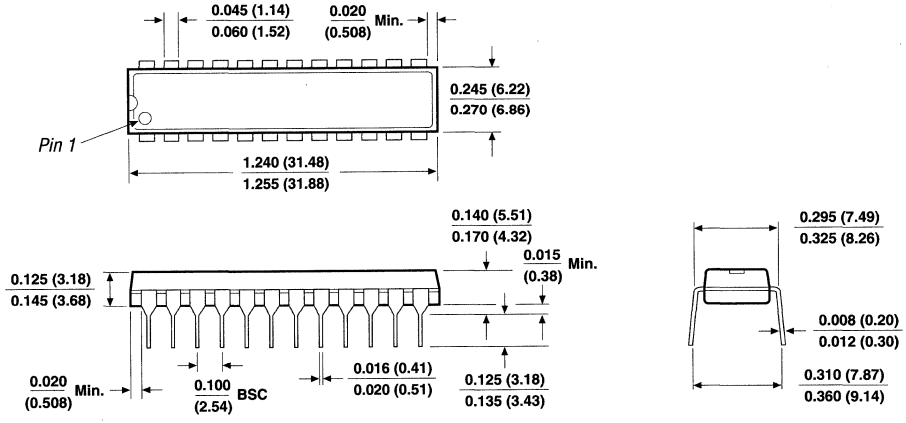
24-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



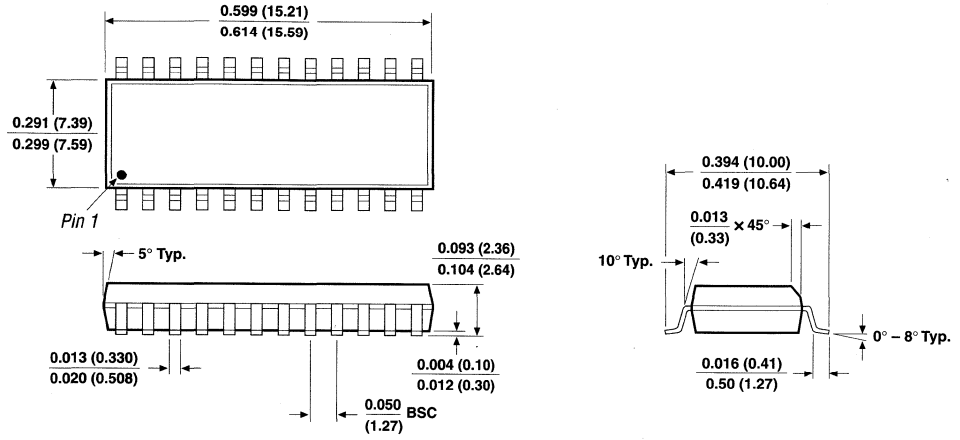
24-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



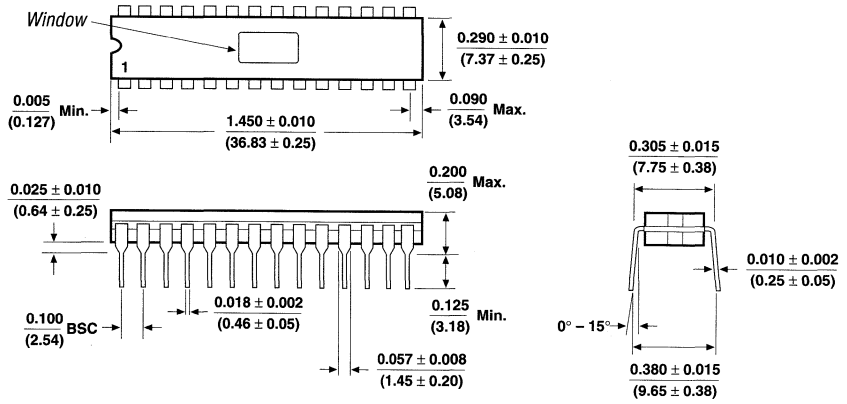
24-Pin Plastic Small-Outline Integrated Circuit (SOIC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



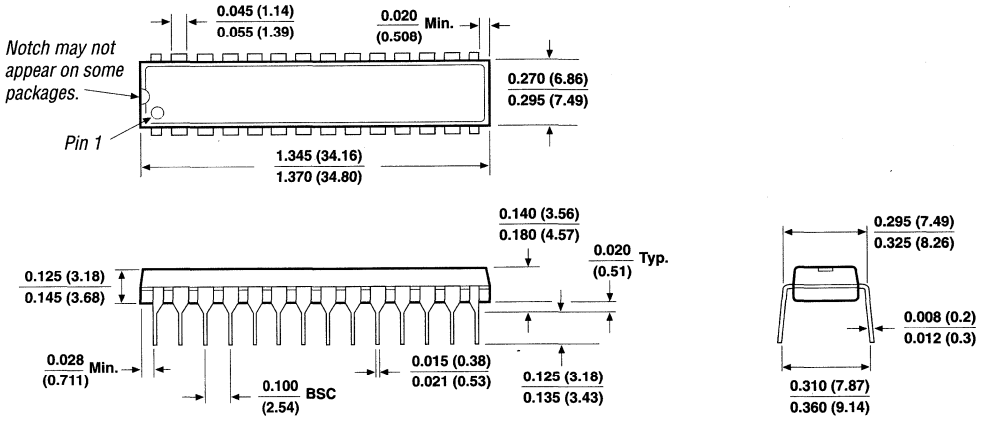
28-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



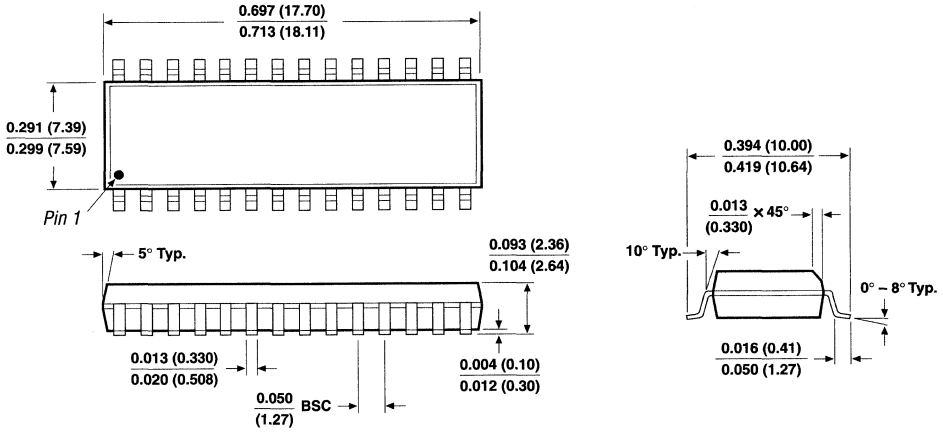
28-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



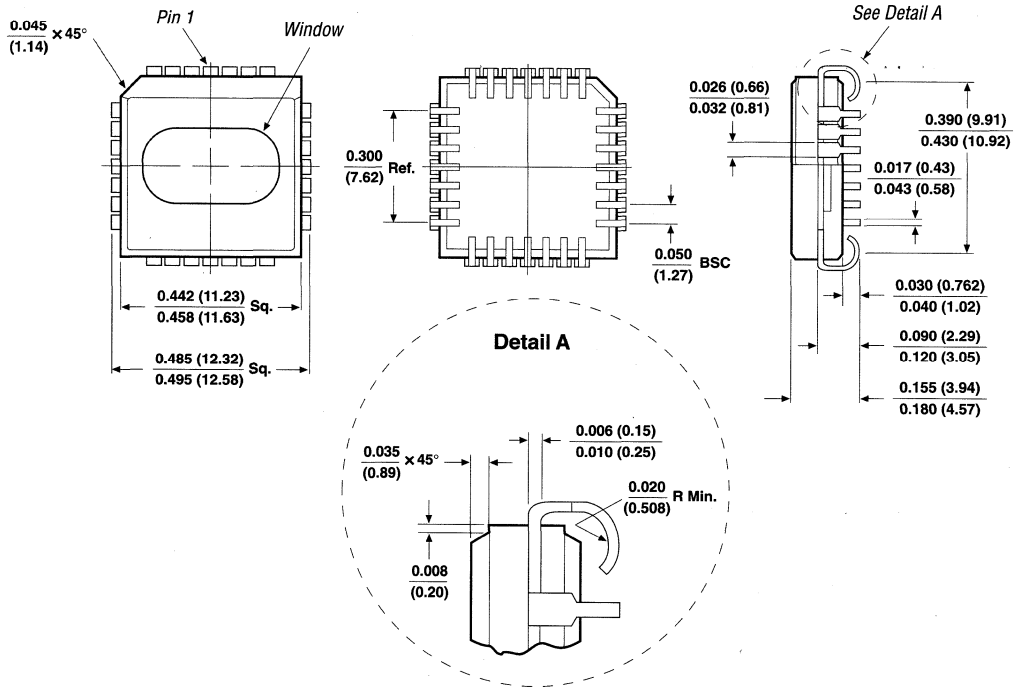
28-Pin Plastic Small-Outline Integrated Circuit (SOIC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



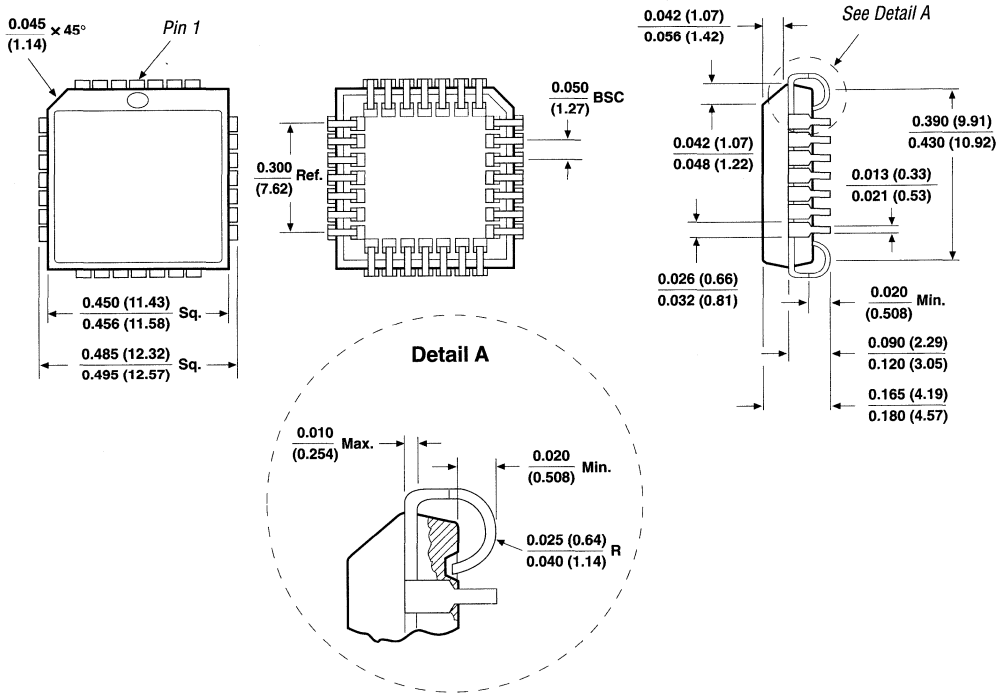
28-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



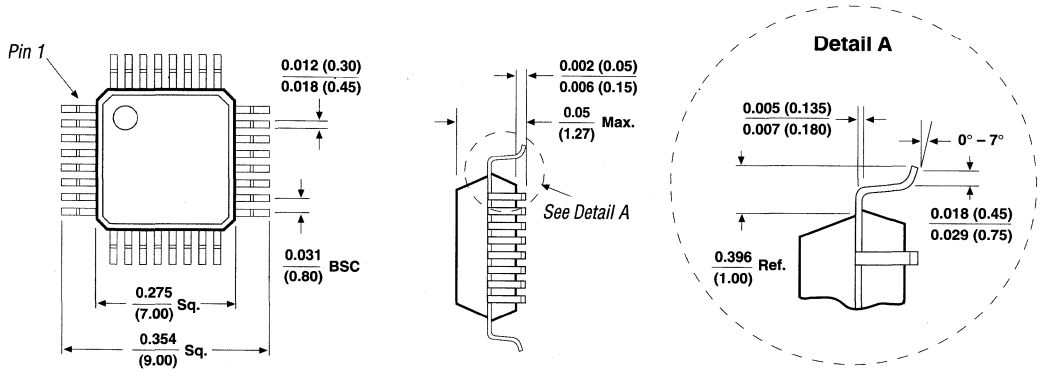
28-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



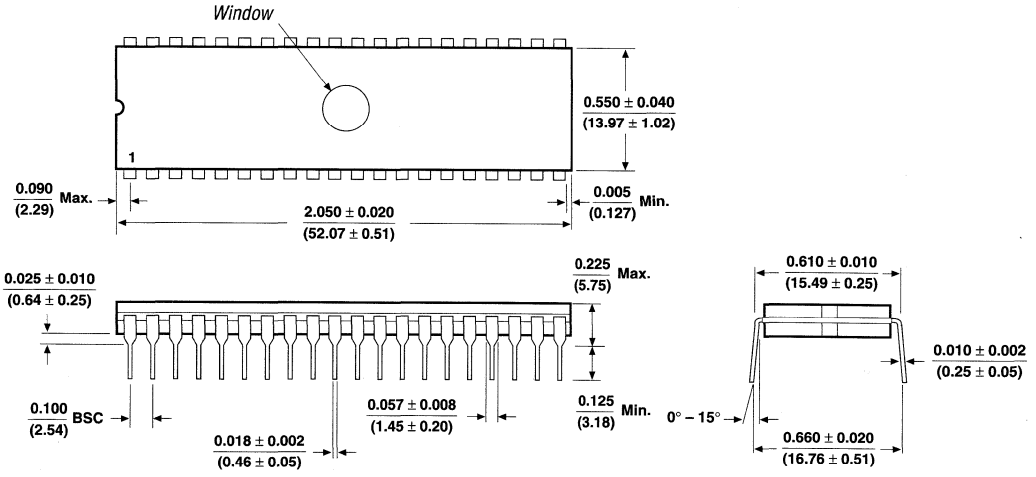
32-Pin Plastic Thin Quad Flat Pack (TQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



40-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



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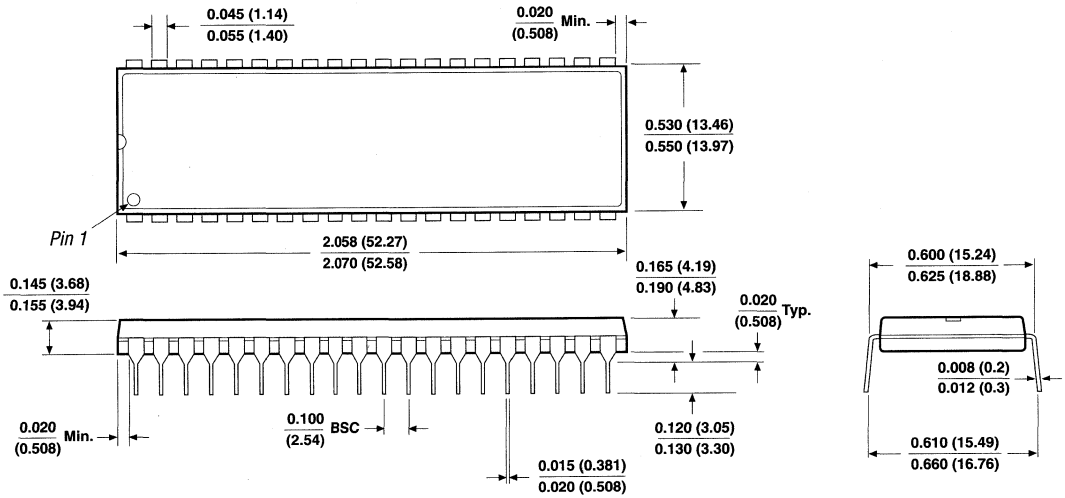
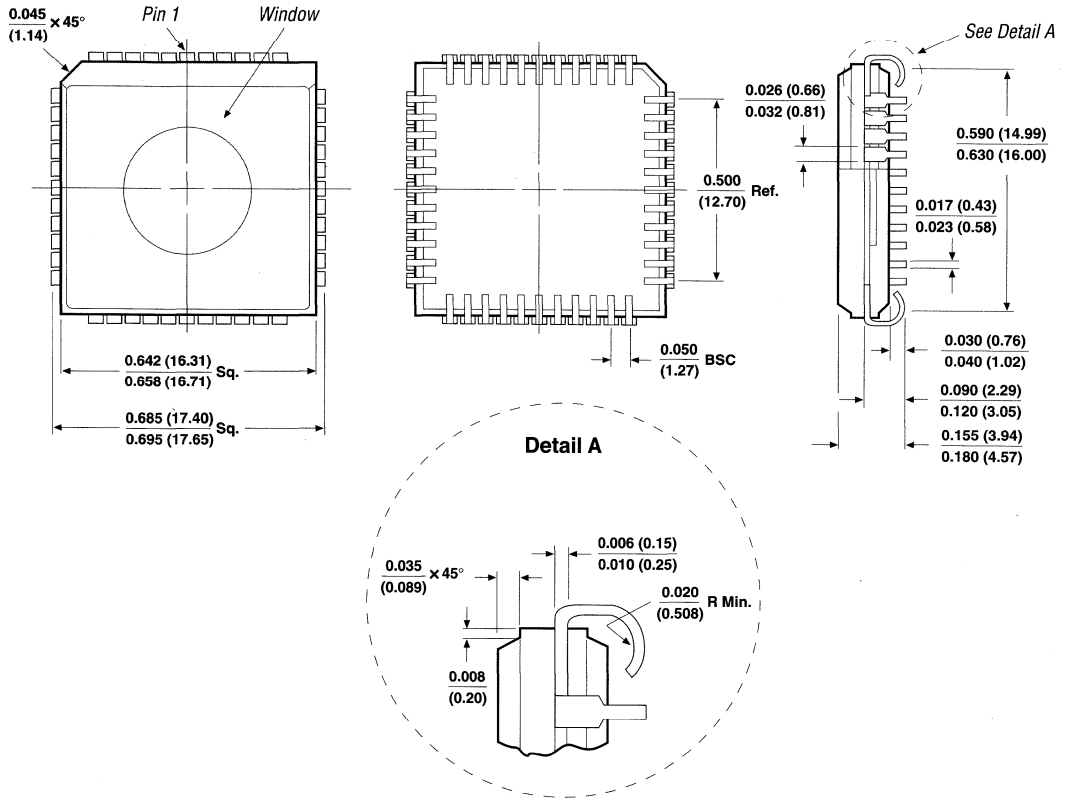
40-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



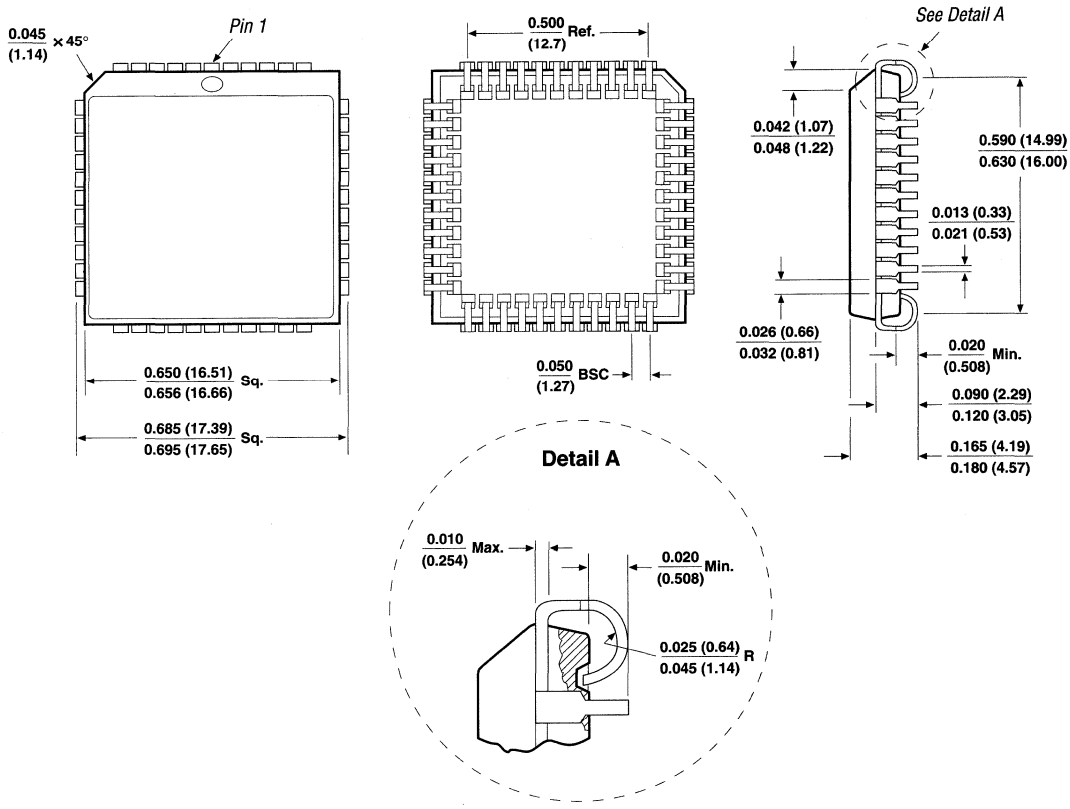
44-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



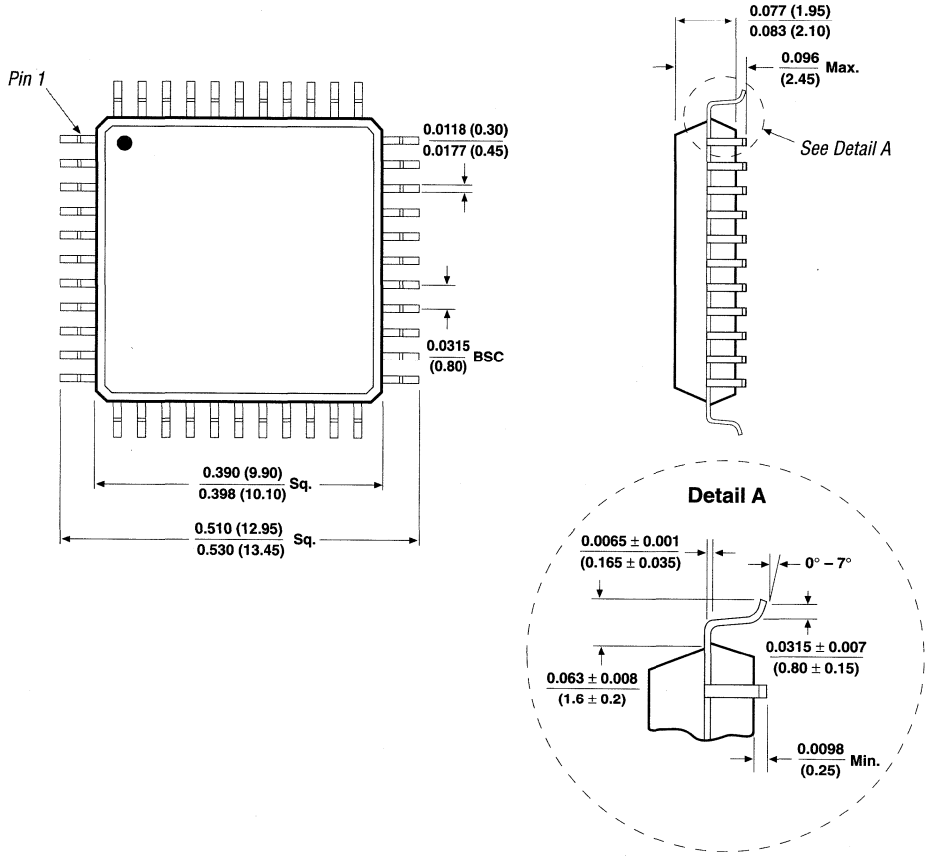
44-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



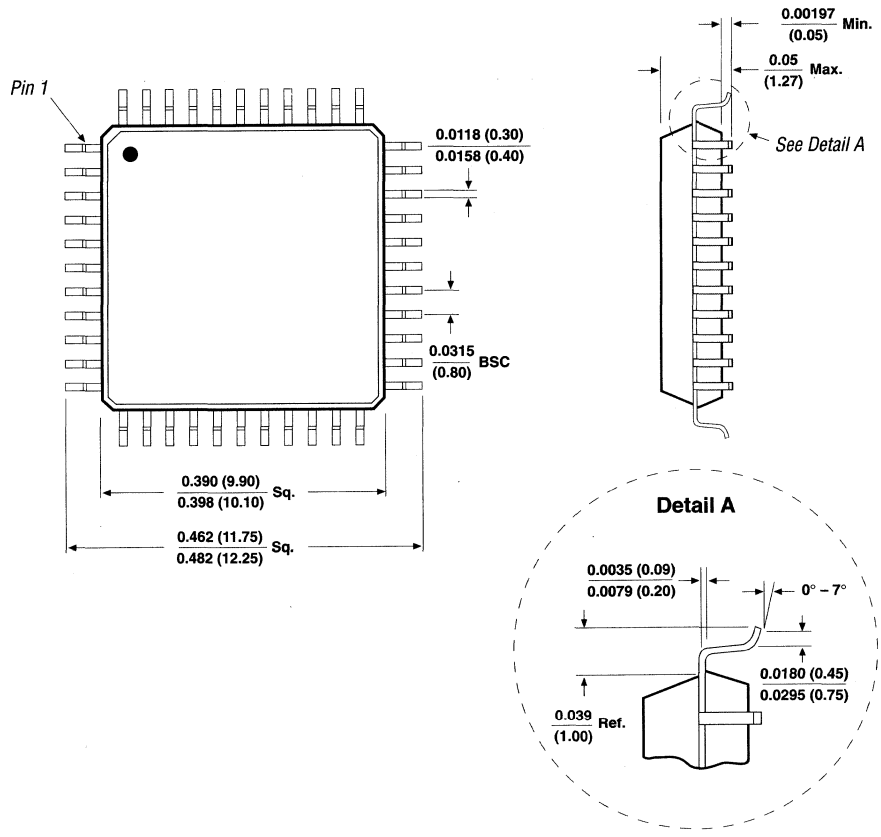
44-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



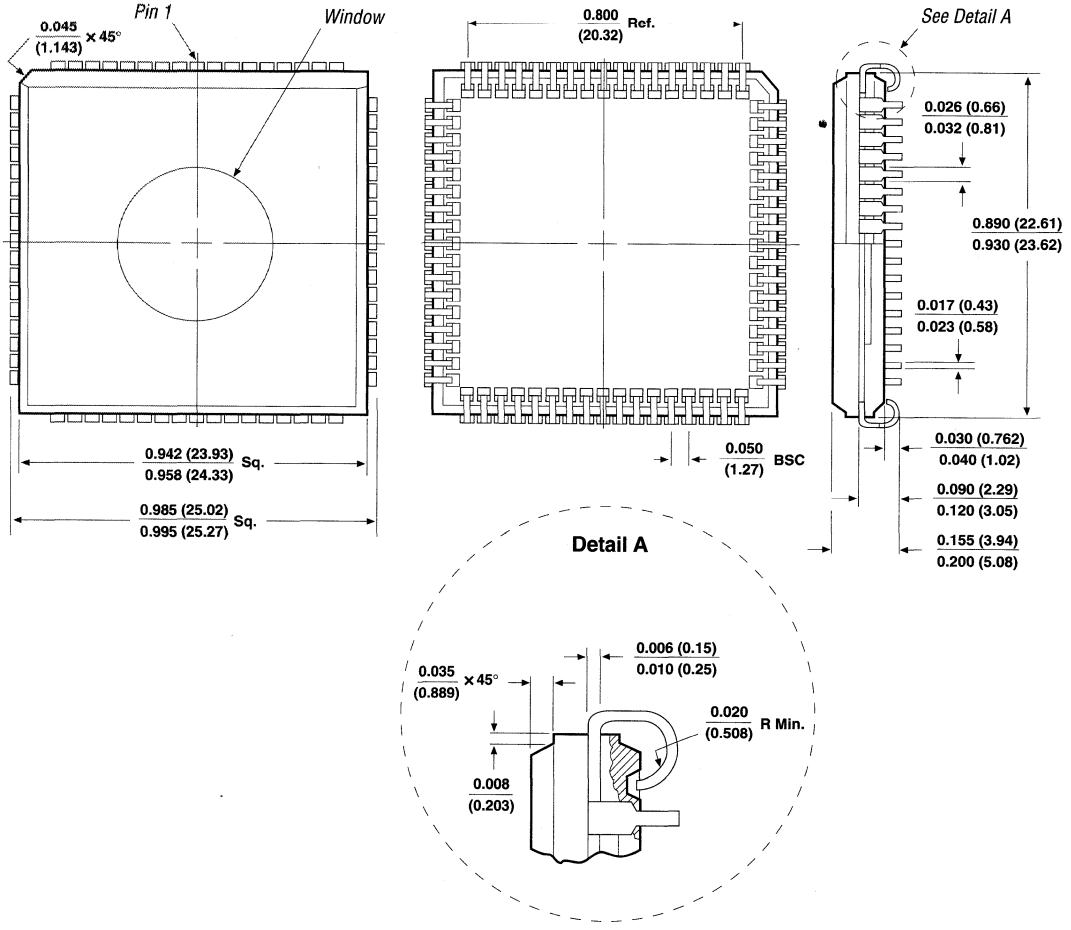
44-Pin Plastic Thin Quad Flat Pack (TQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



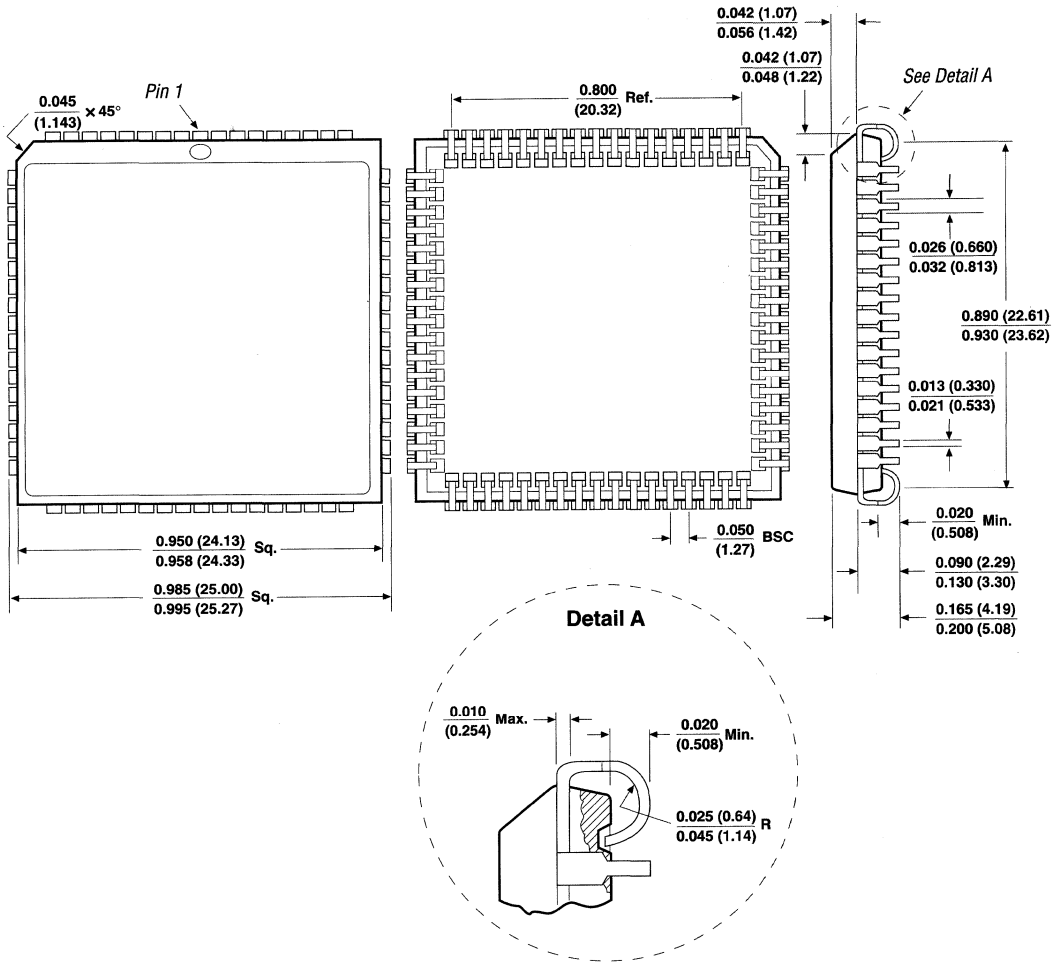
68-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



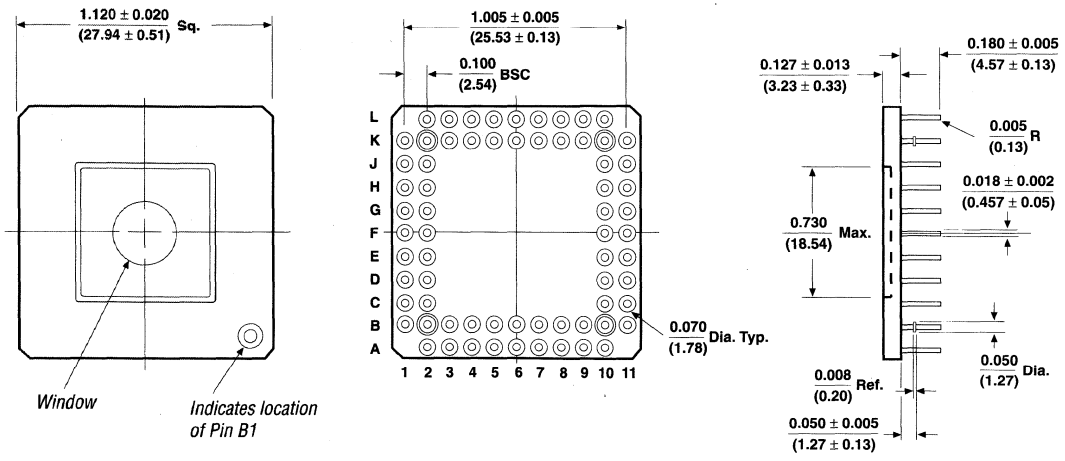
68-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



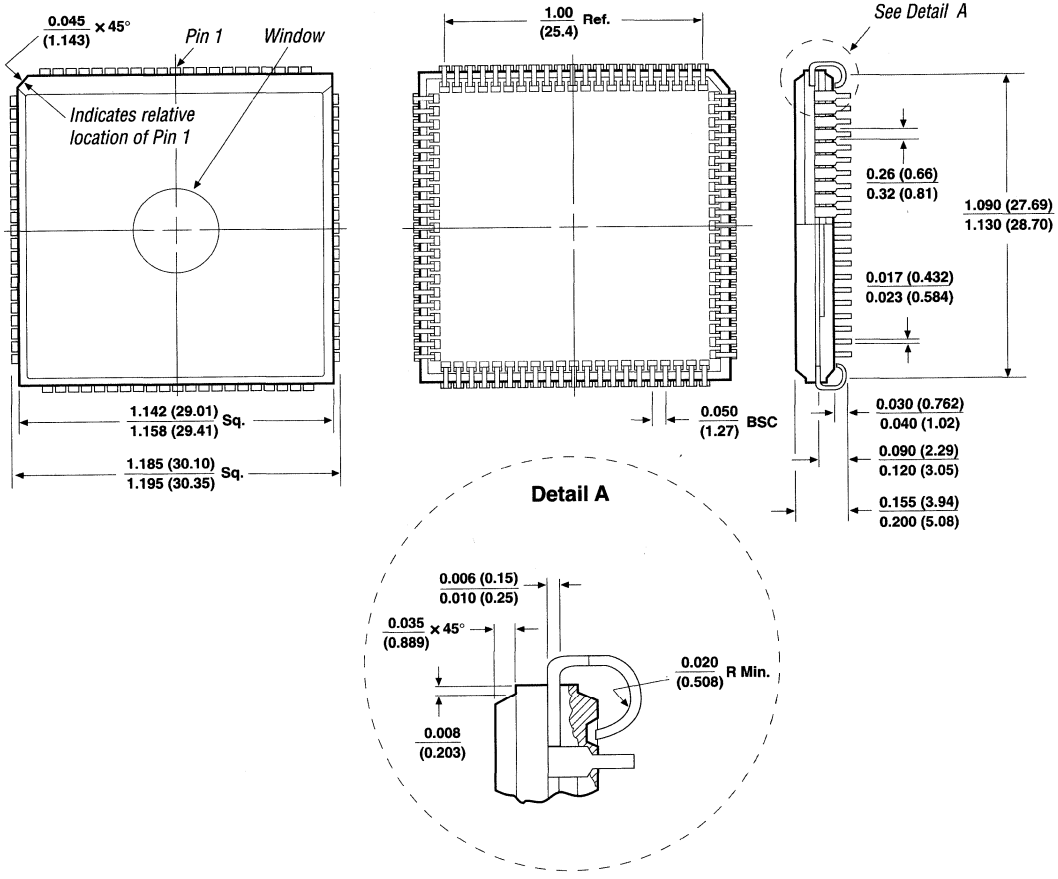
68-Pin Small Outline Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



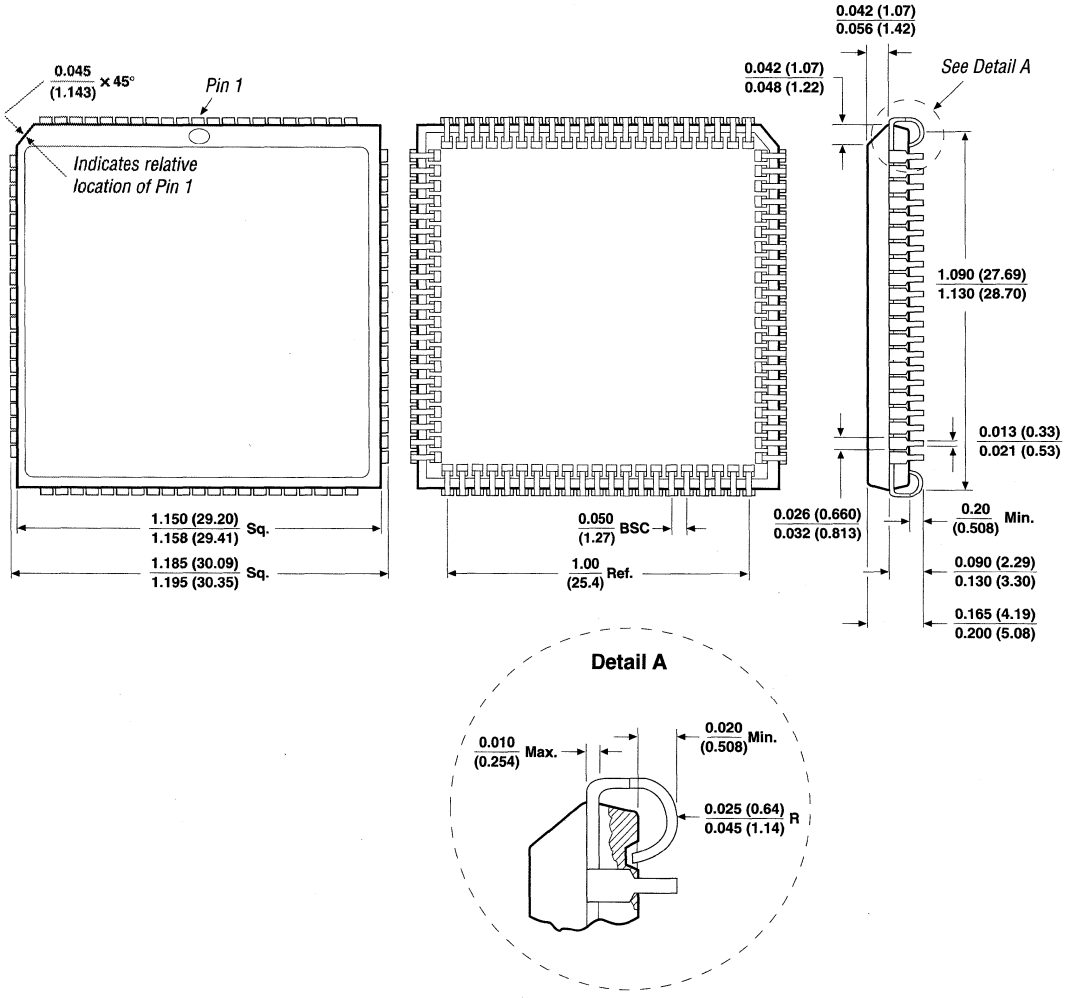
84-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



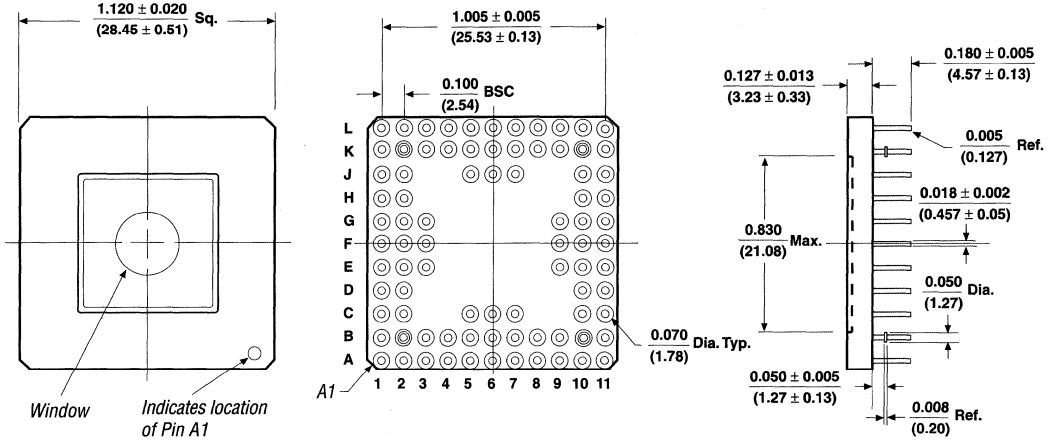
84-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



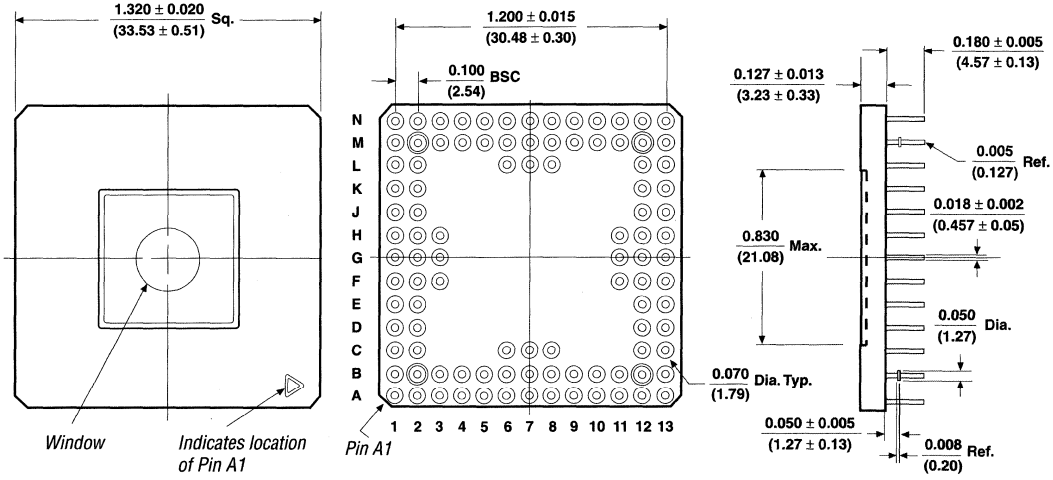
84-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



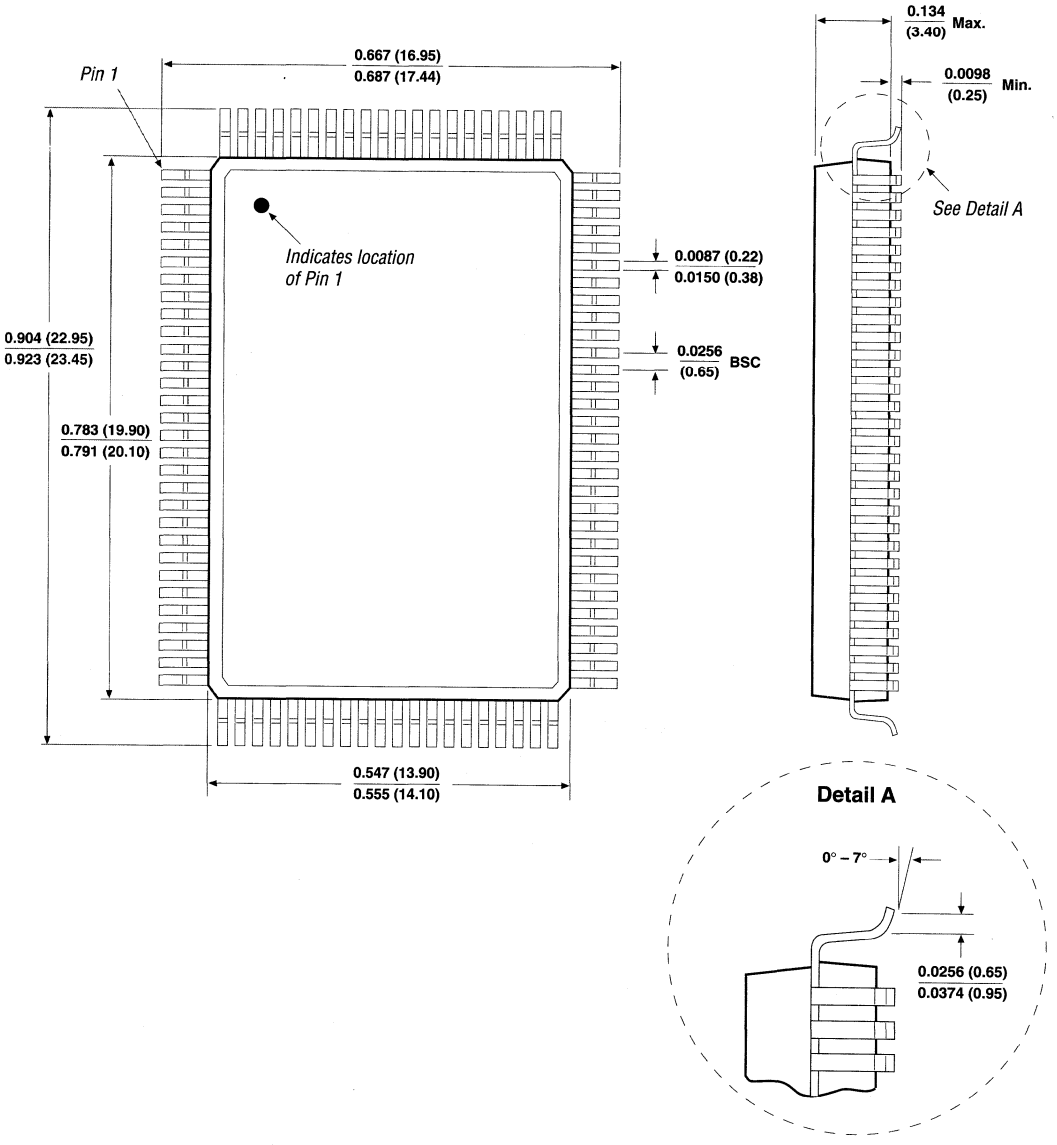
100-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



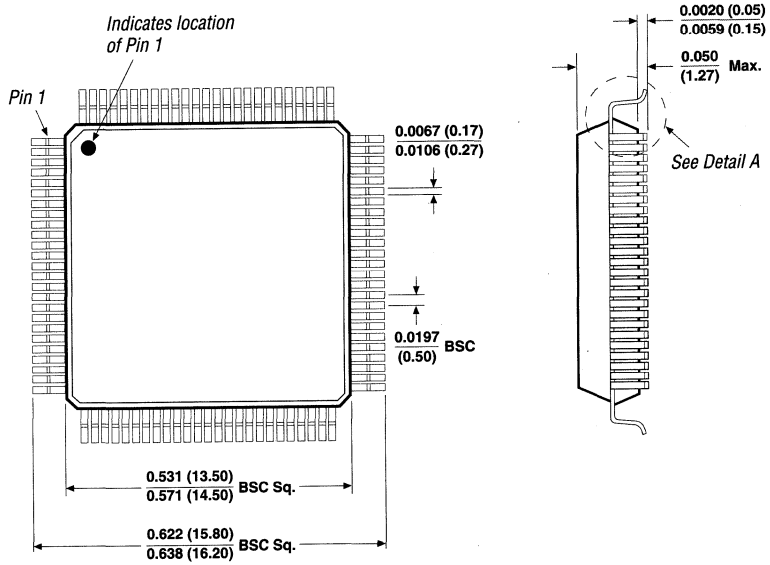
100-Pin Plastic Quad Flat Pack (PQFP)

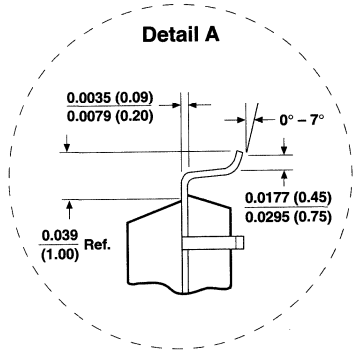
Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



100-Pin Plastic Thin Quad Flat Pack (TQFP)

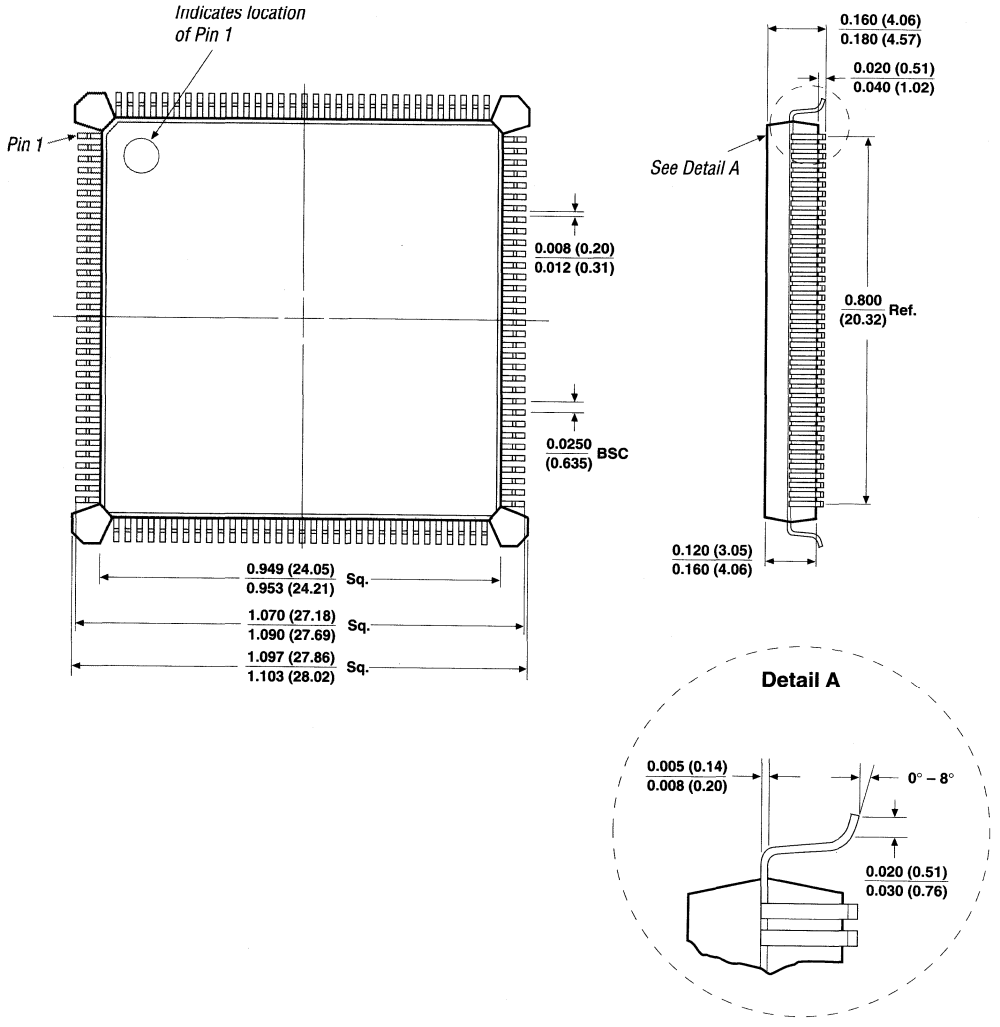
Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.





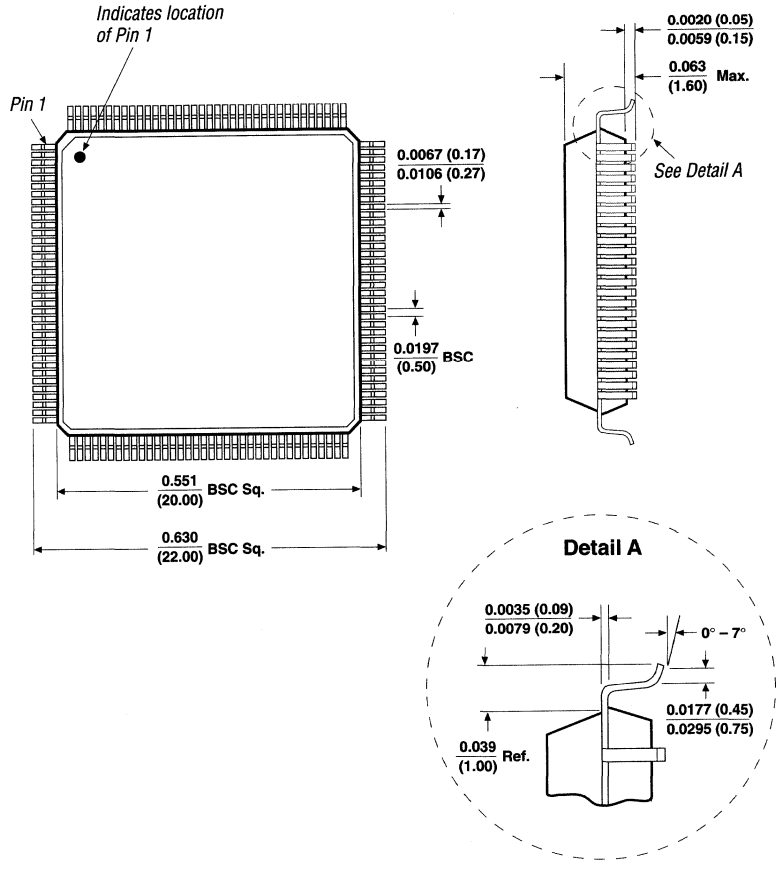
132-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



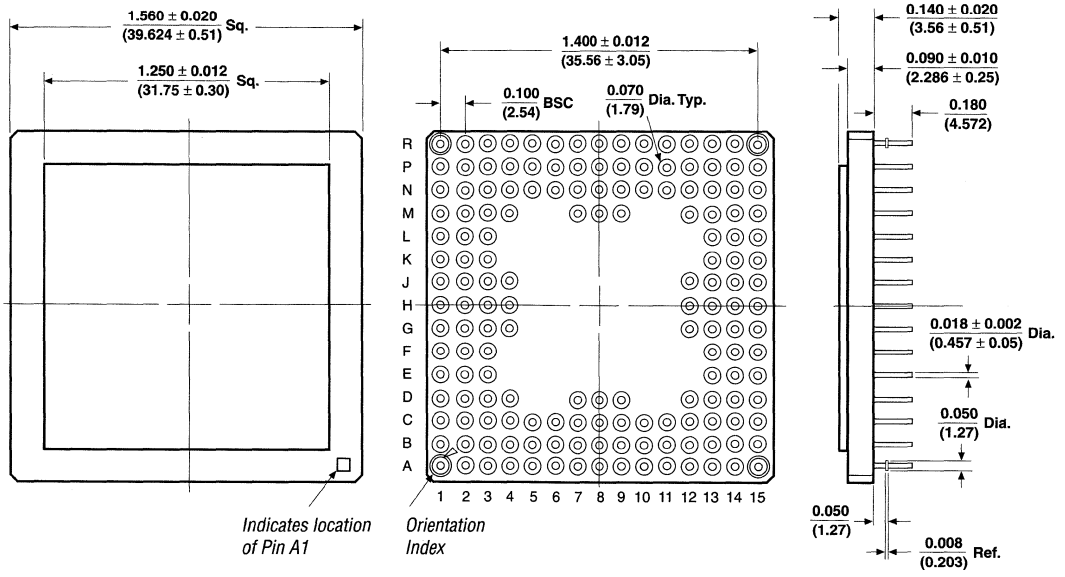
144-Pin Plastic Thin Quad Flat Pack (TQFP)

This information is preliminary. Controlling measurement is in millimeters, shown in parenthesis. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



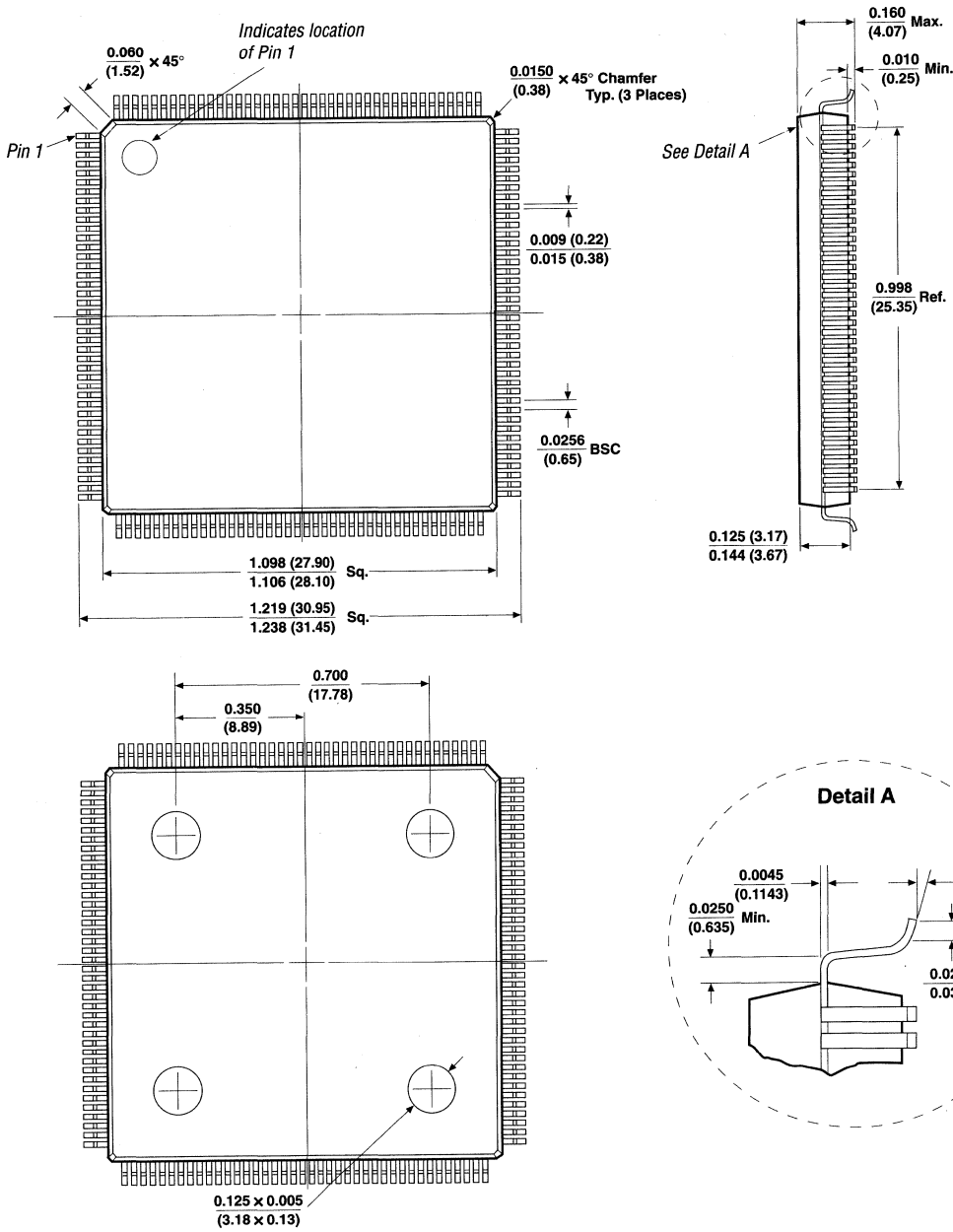
160-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



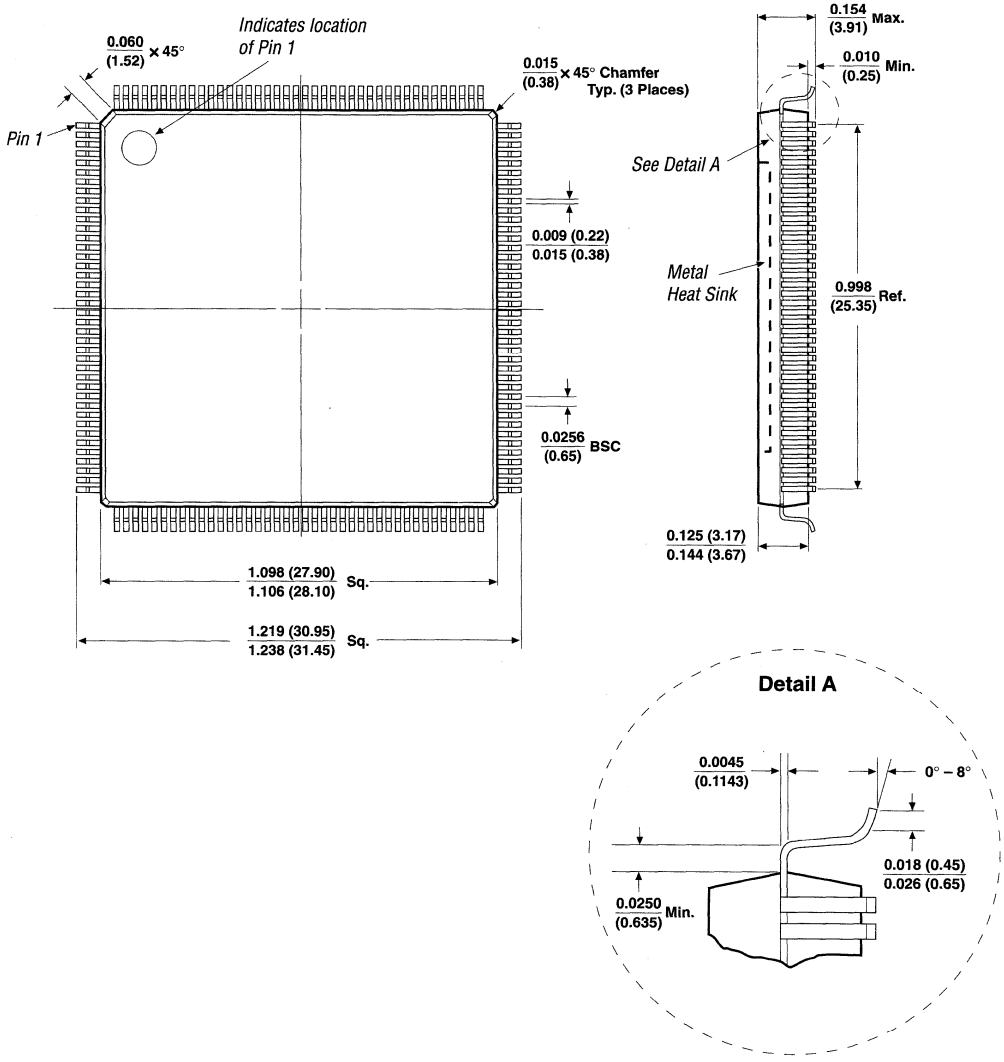
160-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



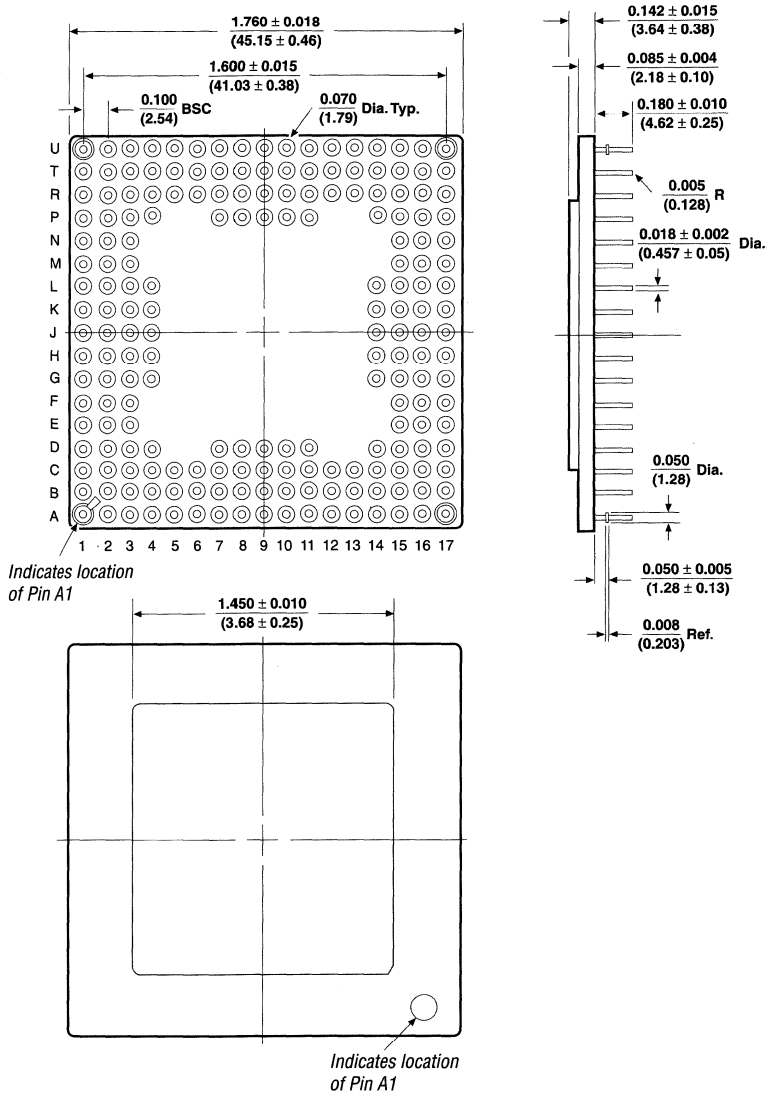
160-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



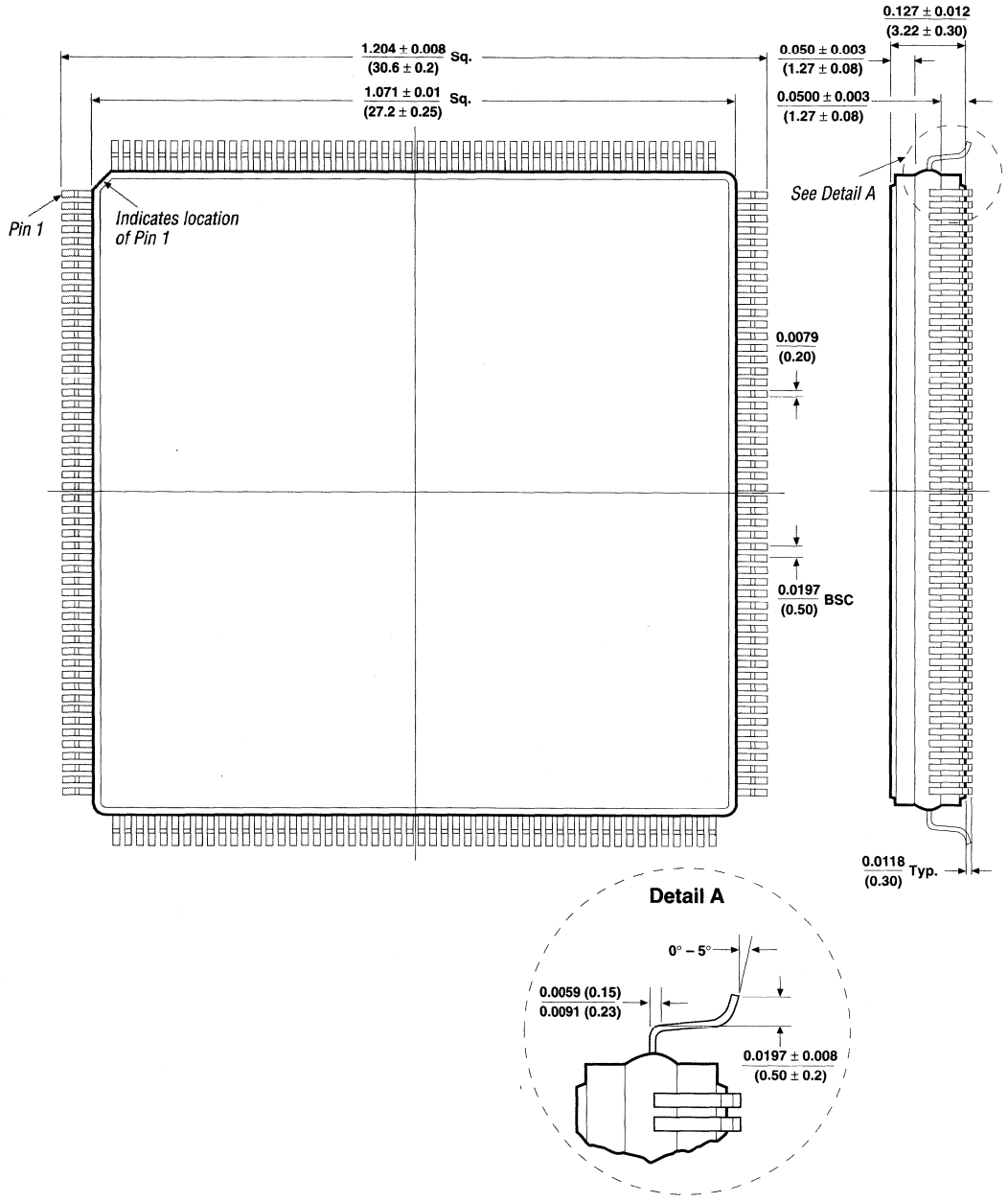
192-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



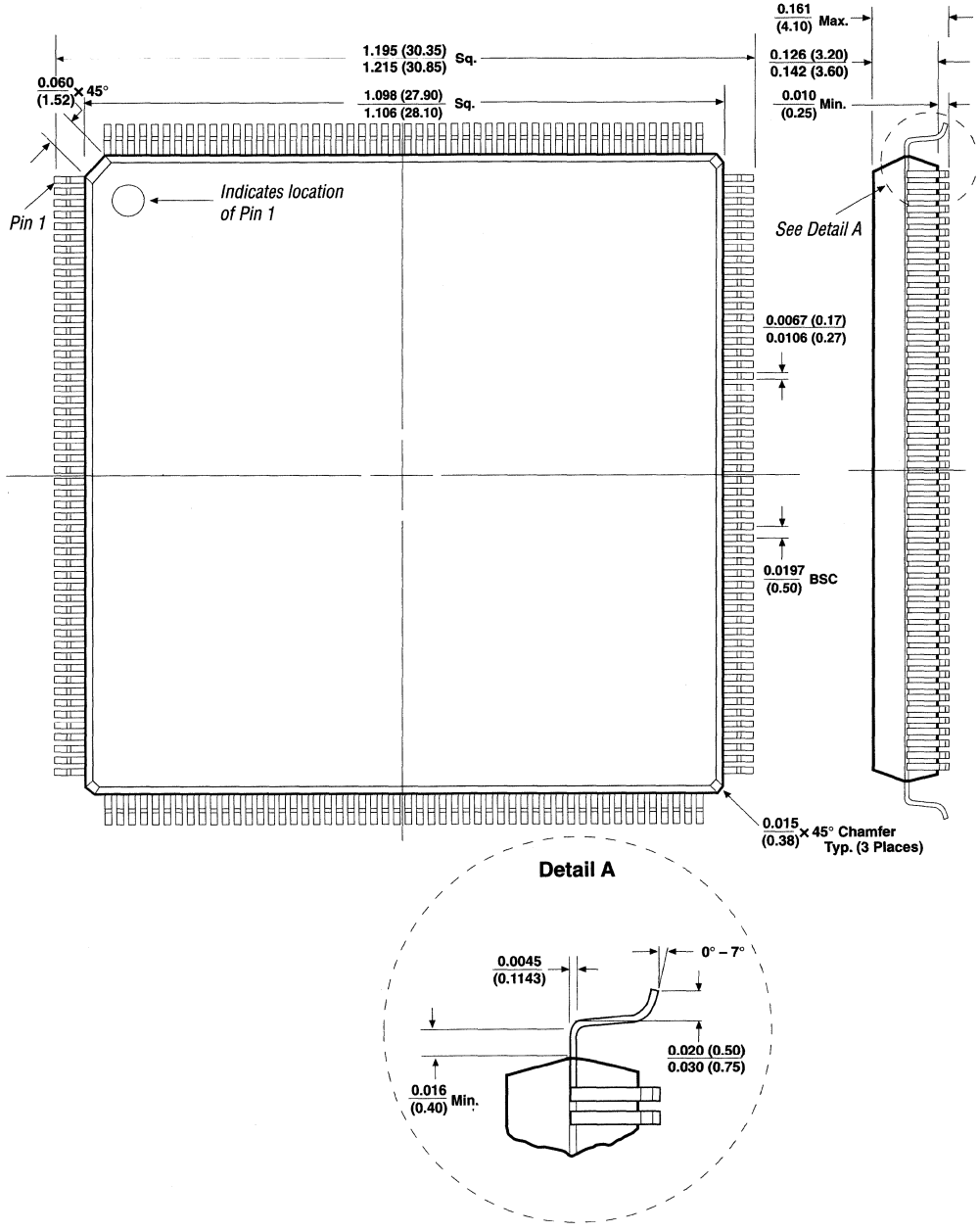
208-Pin Ceramic Quad Flat Pack (CQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



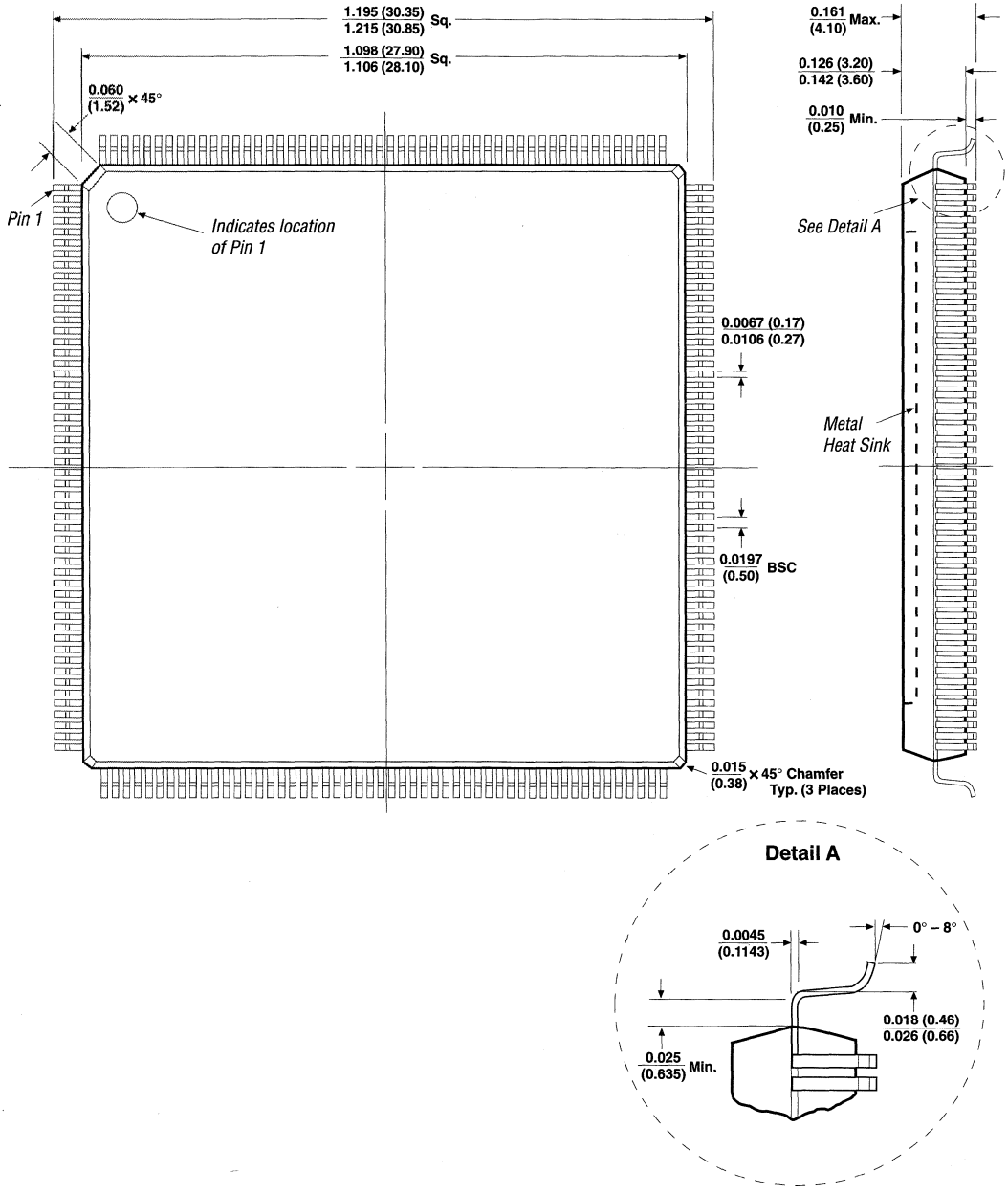
208-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



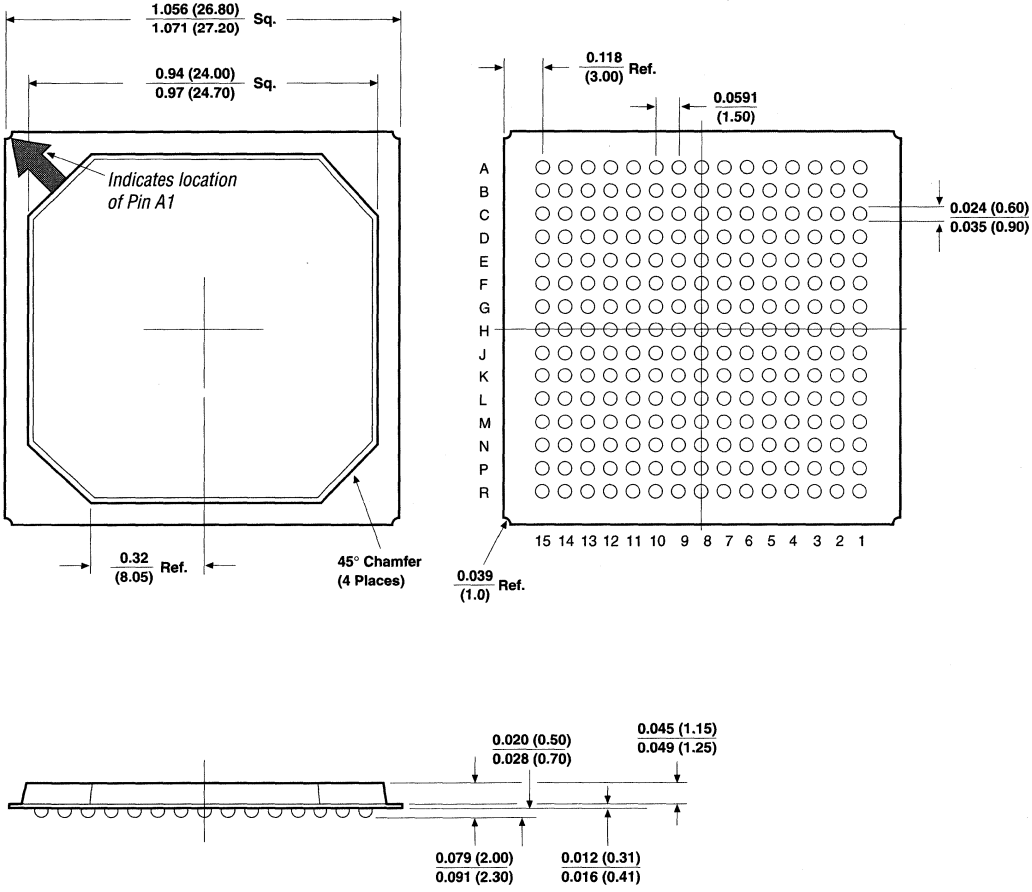
208-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



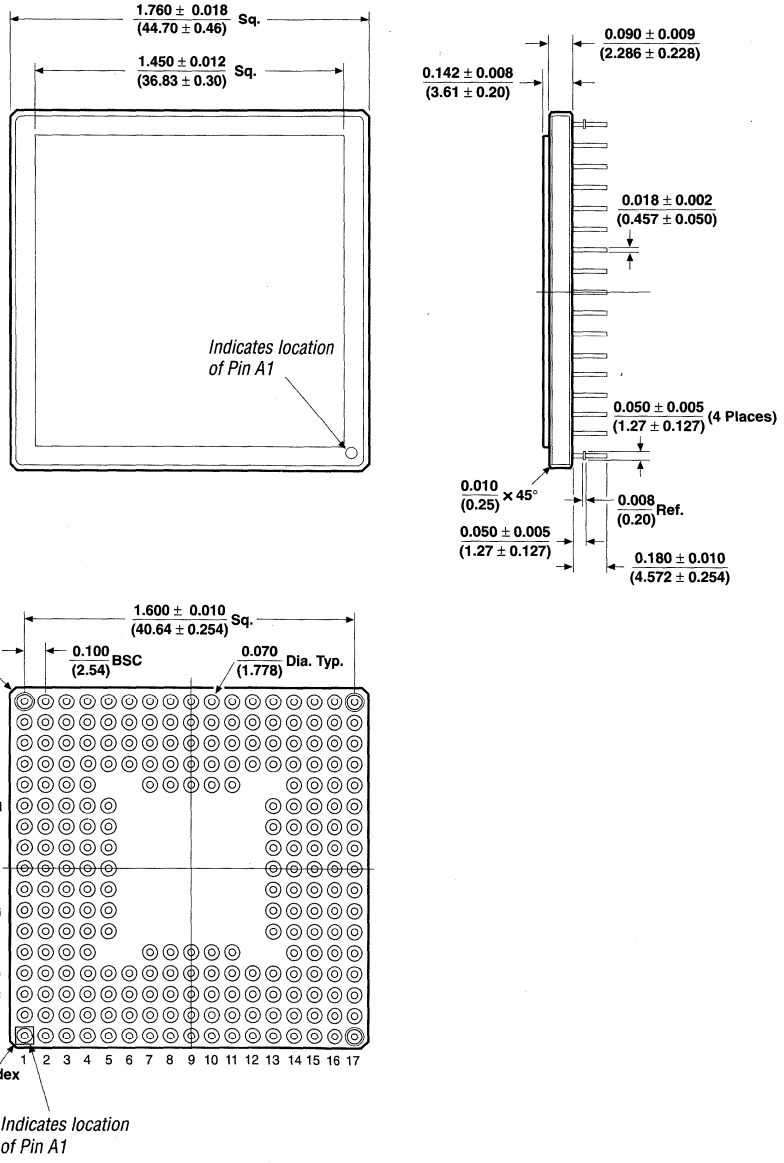
225-Pin Ball-Grid Array (BGA)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



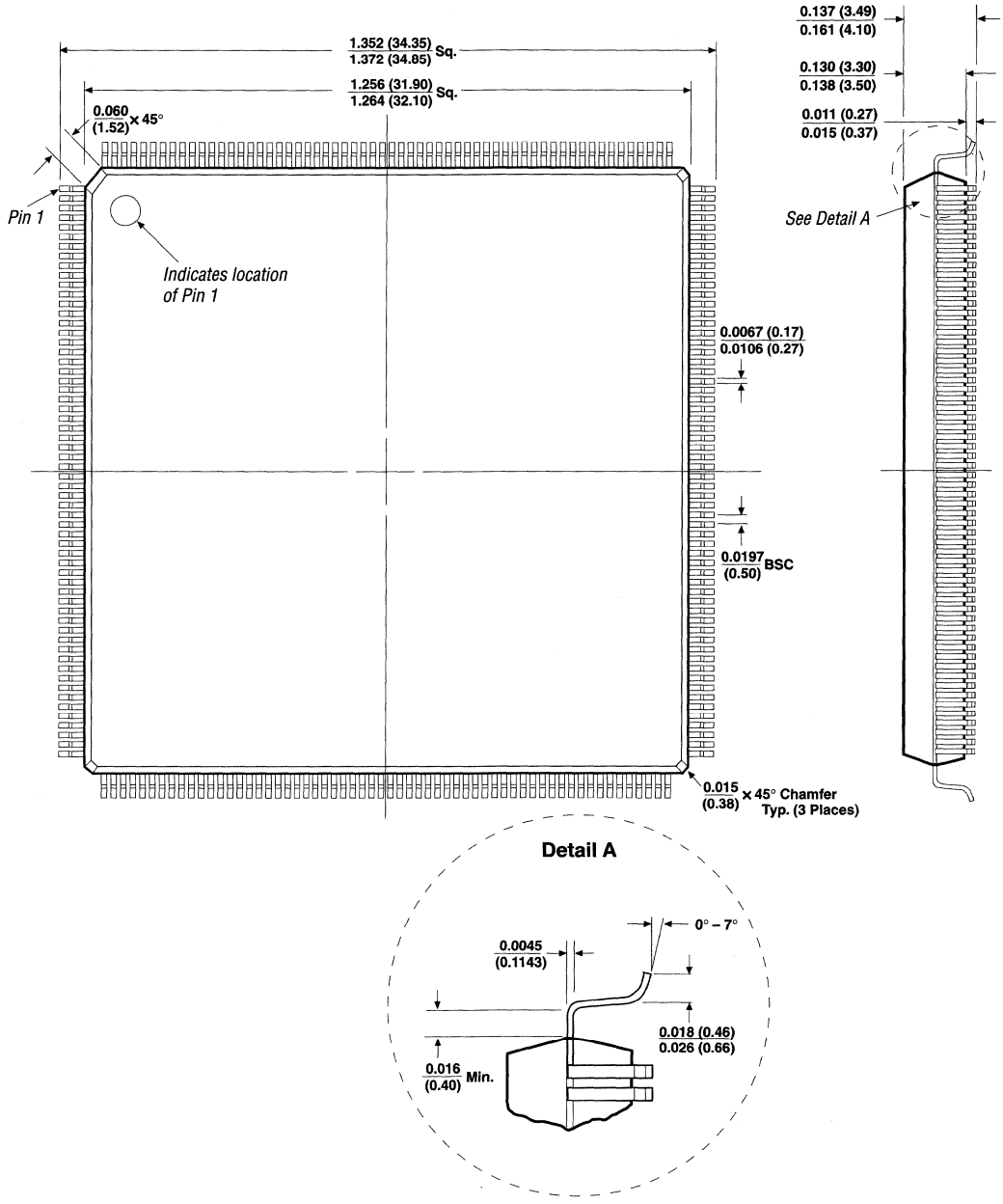
232-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



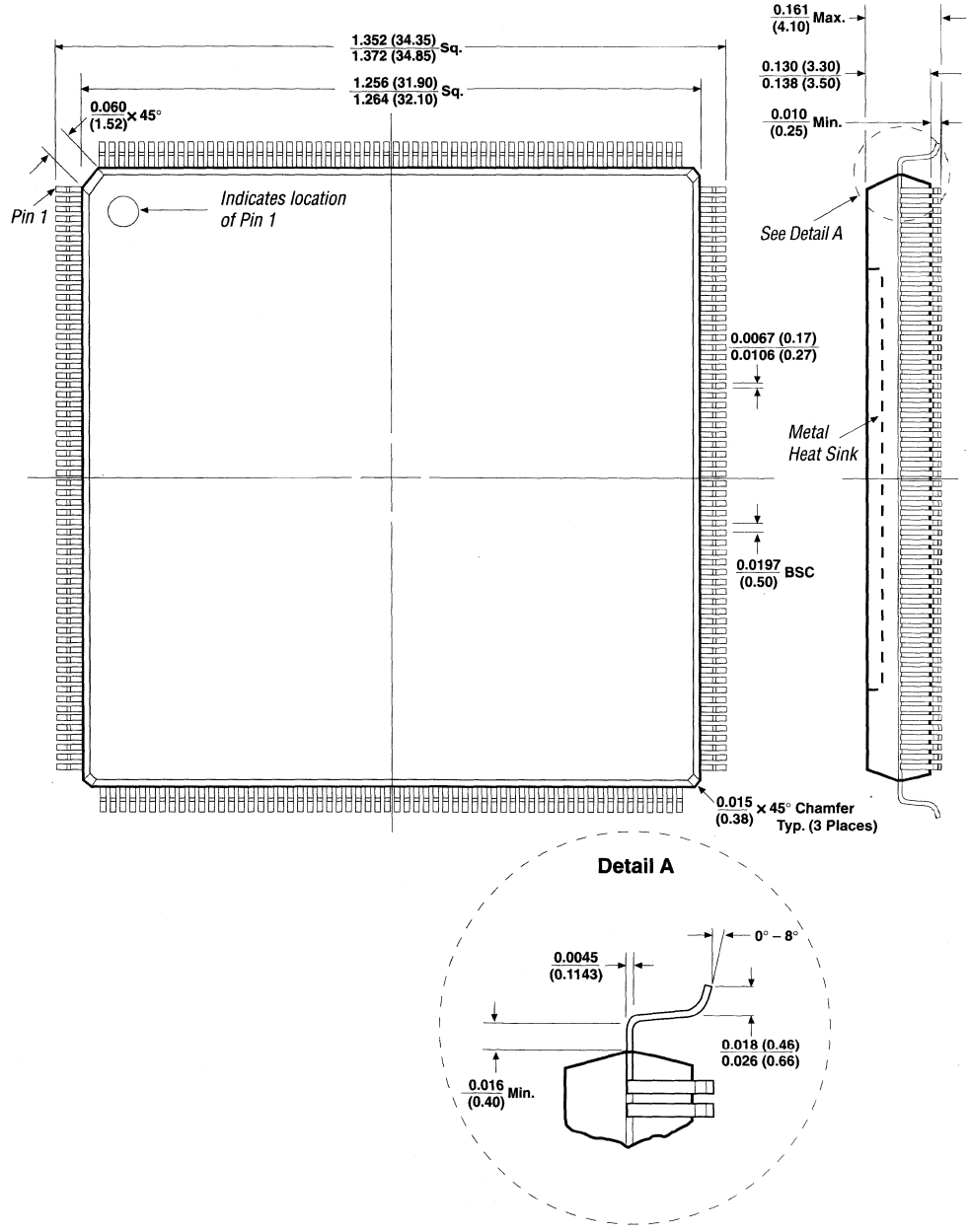
240-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



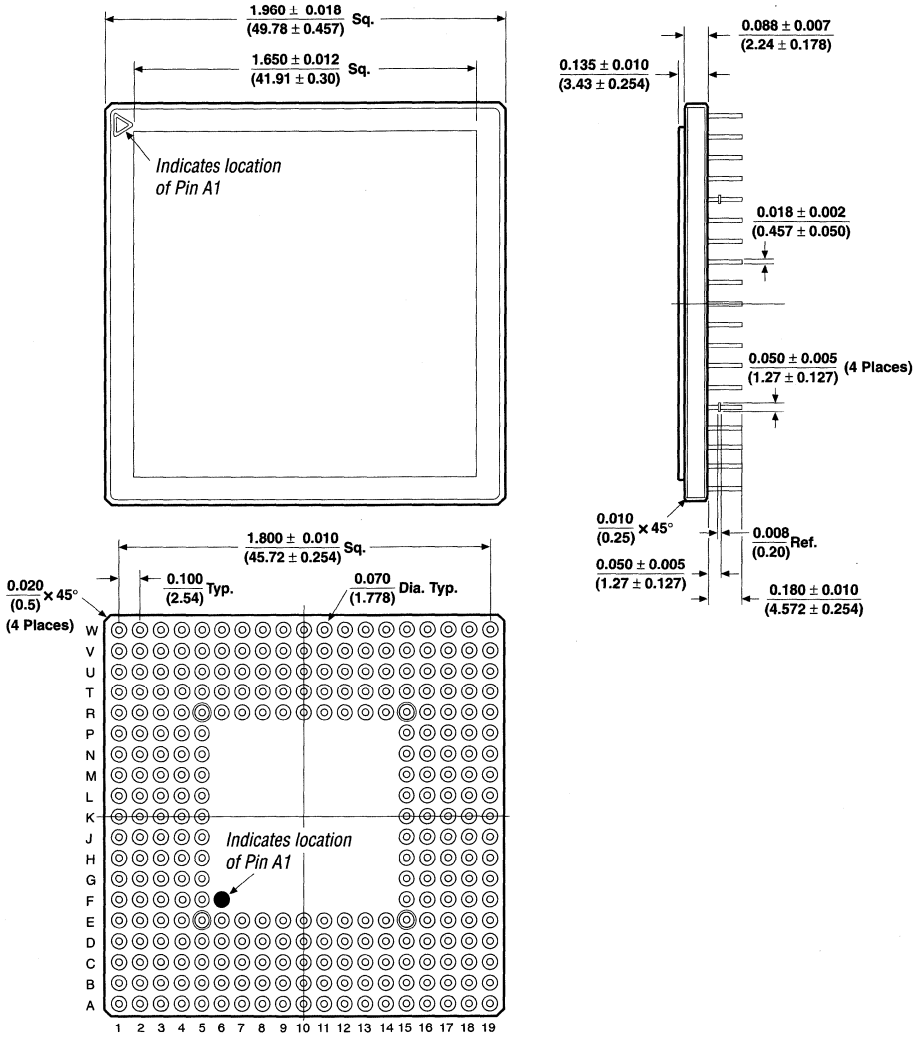
240-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



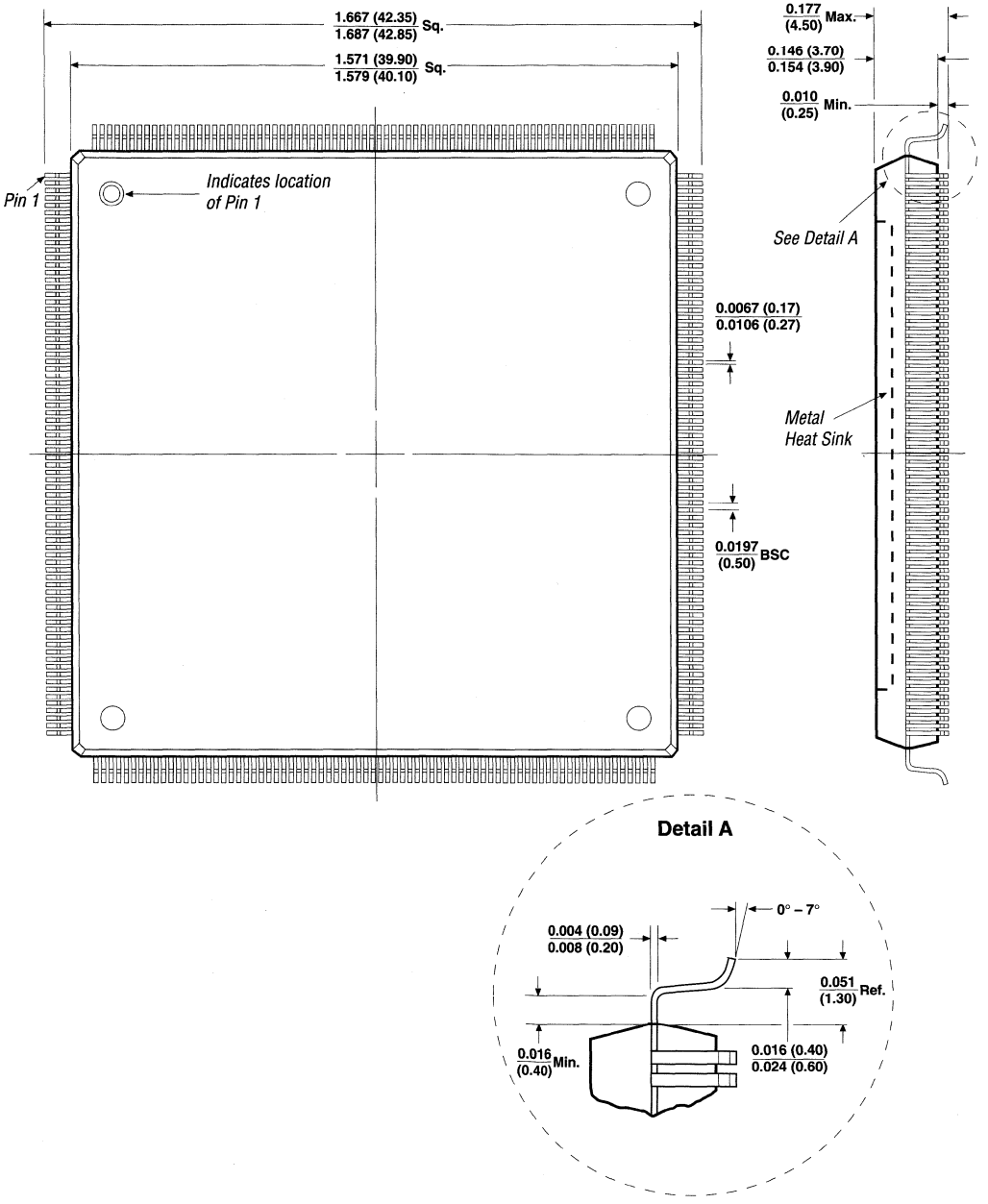
280-Pin Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



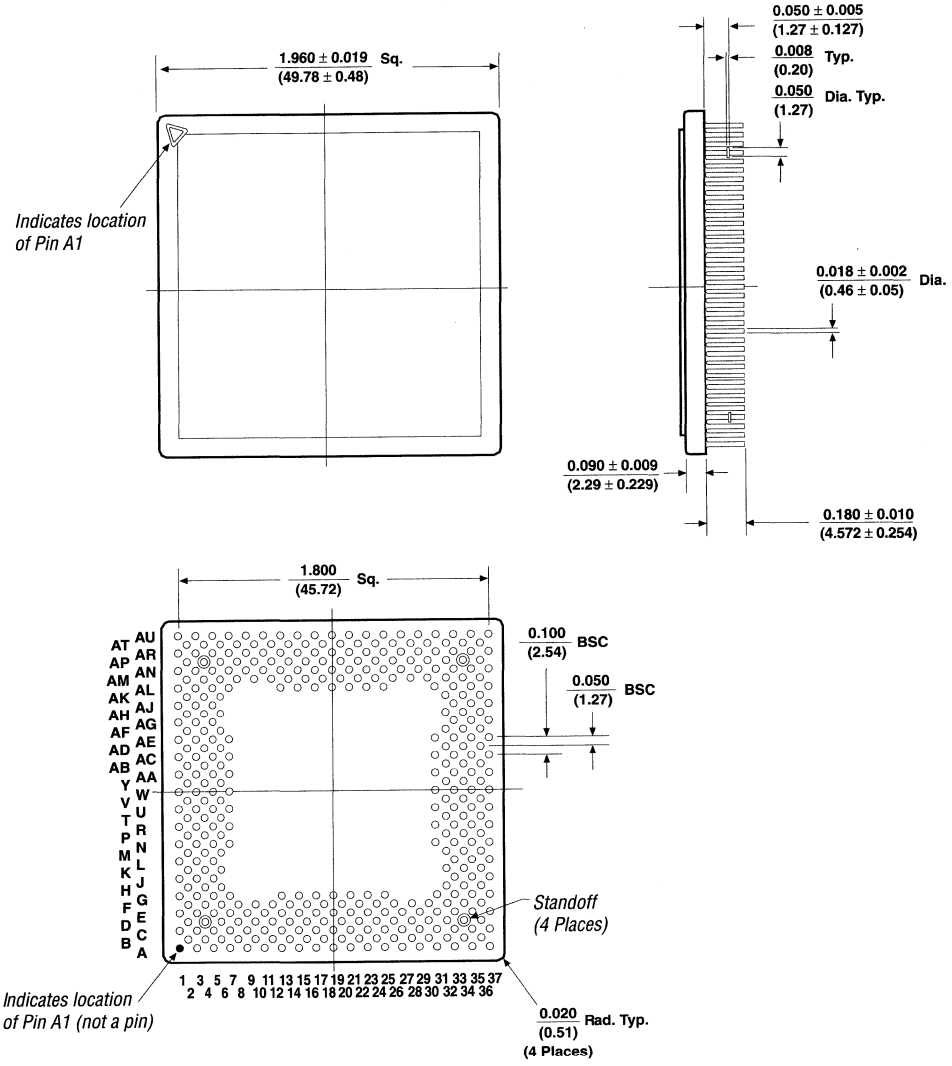
304-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



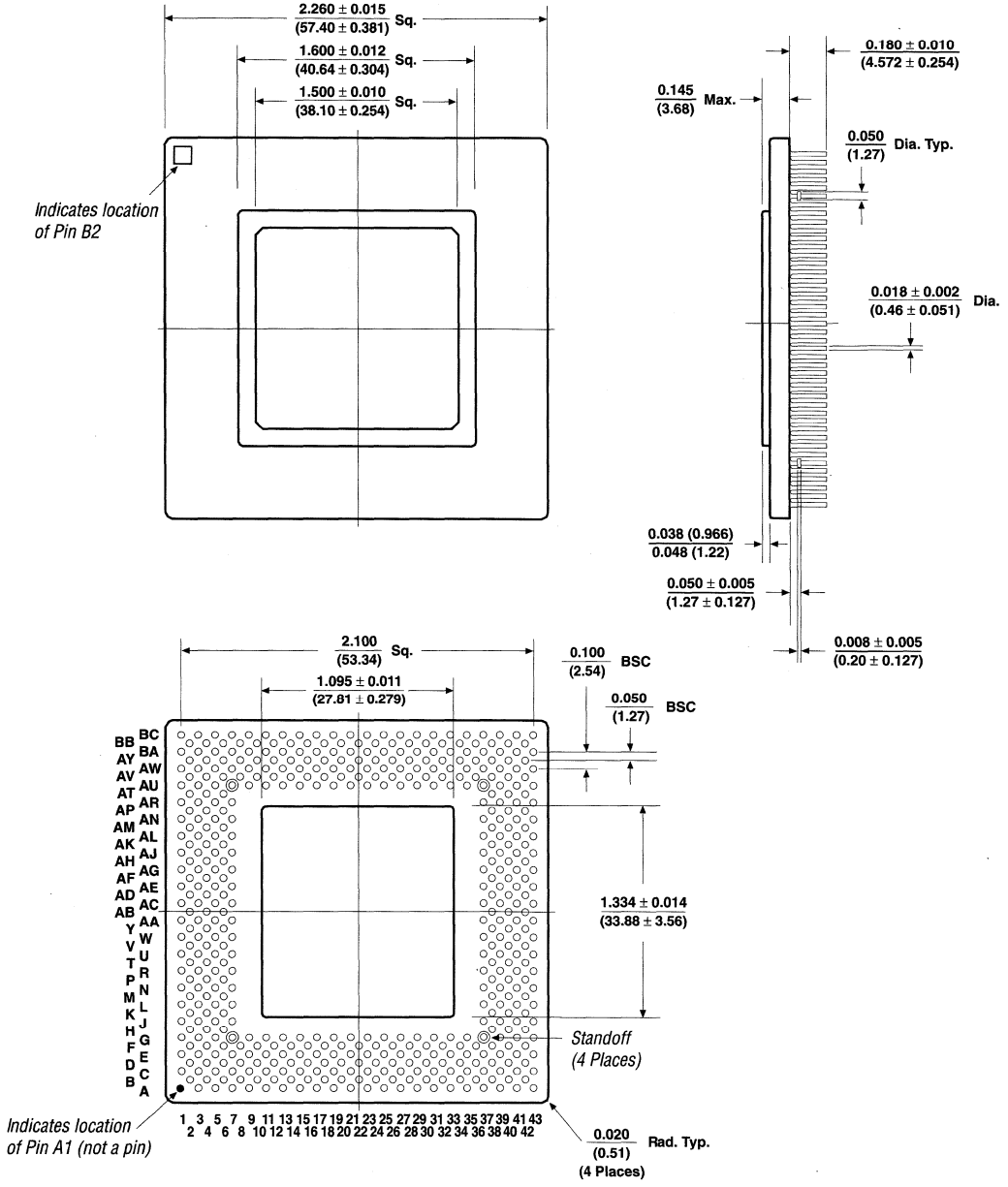
403-Pin Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parenthesis, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



503-Pin Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Package Outlines" on page 635 of this data sheet for dimension formats.



Notes:

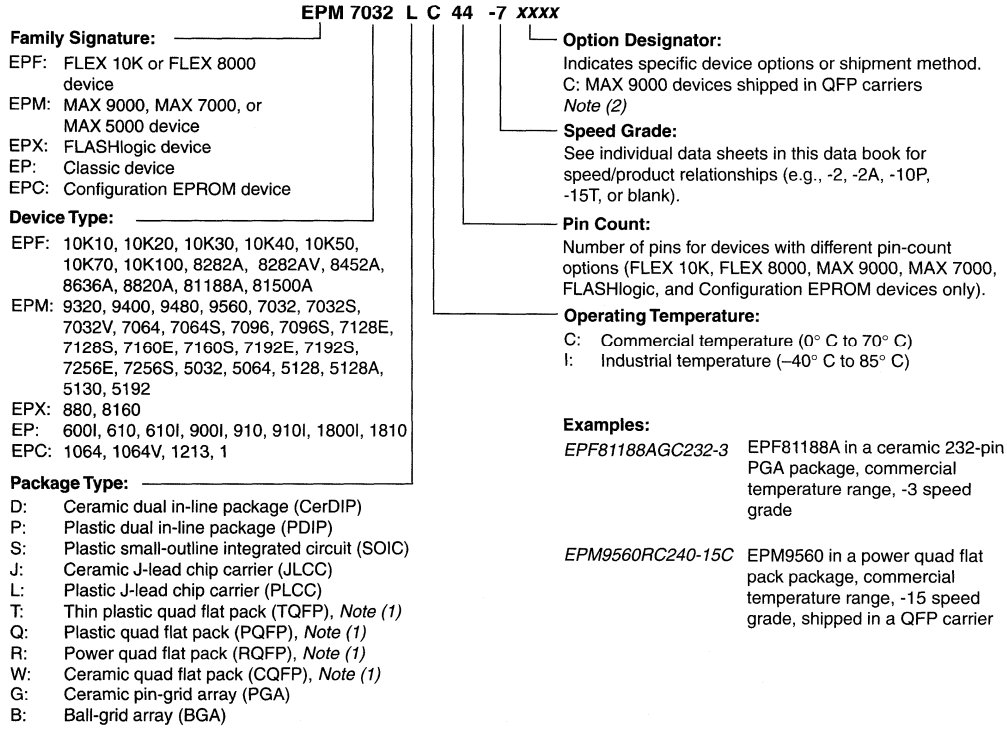
Ordering Information

June 1996, ver. 8

Altera Devices

Figure 1 explains the ordering codes for Altera devices. Devices that have multiple pin counts for the same package include the pin count in their ordering codes. Some codes use relative numbers (e.g., -1, -2) to designate speed grades; others use actual propagation delay times (e.g., -15, -20). For information on specific package, speed grade, and operating temperature combinations, refer to the device family data sheets in this data book, or contact Altera Customer Marketing at (408) 894-7104.

Figure 1. Device Package Ordering Codes



Notes:

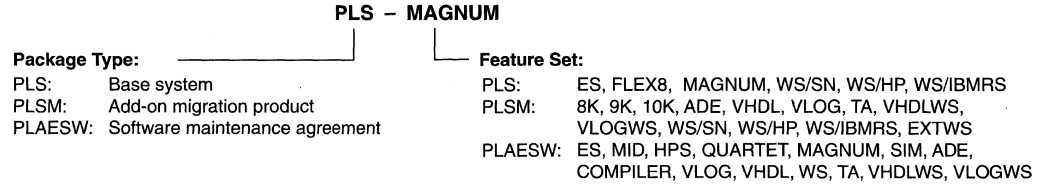
(1) MAX 9000, MAX 7000, and MAX 5000 devices in QFP packages with 100 or more pins can be ordered in QFP carriers. For more information on QFP carriers, see the *QFP Carrier & Development Socket Data Sheet* in this data book; for information on Altera shipment methods, contact Altera Customer Marketing.

(2) Contact Altera Customer Marketing for more information.

Development Tools

Figure 2 explains the ordering codes for Altera development systems. For information on specific packages, refer to the *MAX+PLUS II Programmable Logic Development System Data Sheet* in this data book, or contact Altera Customer Marketing at (408) 894-7104.

Figure 2. Development System Ordering Codes



Programming Hardware

This section provides the ordering codes for Altera programming hardware and adapters. Table 1 lists the ordering codes for the programming cards, cables, and units.

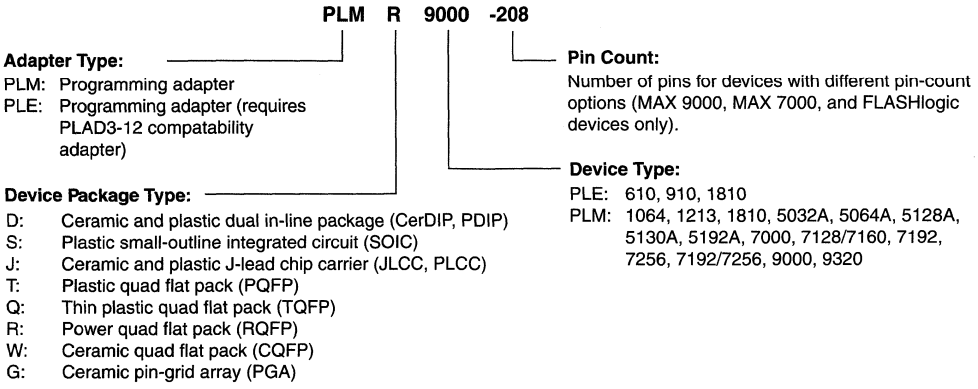
Table 1. Programming Hardware

Product	Ordering Code	Description
Altera Stand-Alone Programmer	PL-ASAP2	Includes programming software, a Logic Programmer card, and the MPU.
LP6 Logic Programmer Card	PLP6	Interfaces with IBM PC-AT and compatible computers.
Master Programming Unit (MPU)	PL-MPU	With the appropriate adapters, programs all Altera devices.
Compatibility Adapter	PLAD3-12	Interfaces PLE-prefix adapters to the MPU. Together with the MPU, directly programs 20-pin Classic devices.
BitBlaster Serial Download Cable	PL-BITBLASTER	Interfaces with IBM-compatible computers and workstations.

Figure 3 explains the ordering codes for Altera programming adapters. Two types of adapters plug directly into the Master Programming Unit (MPU): PLM-prefix and PLAD3-12 adapters. Multiple pin-compatible devices use the same device type code shown in Figure 3.

Figure 3. Programming Adapter Ordering Codes

See the Altera Programming Hardware Data Sheet for specific information on each device and package combination.



QFP Carrier & Development Sockets

Table 2 shows the ordering codes for QFP device device sockets. All MAX 9000, MAX 7000, and MAX 5000 QFP devices with 100 or more pins may be ordered in QFP carriers. QFP carriers and development sockets are rated from –65° C to 155° C and are qualified to handle commercial (C) and industrial (I) operating temperatures.

Table 2. QFP Device Sockets

Product	Ordering Code
100-pin development socket (includes removal tool)	PL-SKT/Q100
160-pin development socket (includes removal tool)	PL-SKT/Q160
208-pin development socket (includes removal tool)	PL-SKT/Q208
240-pin development socket (includes removal tool)	PL-SKT/Q240
304-pin development socket (includes removal tool)	PL-SKT/Q304

Table 3 shows the ordering codes for QFP carrier extraction tools.

Table 3. QFP Carrier Extraction Tools

Product	Ordering Code
100-pin QFP carrier extraction tool	PL-EXT1
160- and 208-pin QFP carrier extraction tool	PL-EXT2
240-pin QFP carrier extraction tool	PL-EXT4
304-pin QFP carrier extraction tool	PL-EXT5

Notes:

Guidelines for Handling J-Lead & QFP Devices

June 1996, ver. 2 Application Note 71

Introduction

Surface-mount J-lead and quad flat pack (QFP) devices are currently in high demand. All device packages require protection during transportation and storage. To prevent damage to Altera J-lead and QFP devices, follow the guidelines outlined in this application note. This application note discusses the following topics:

- Handling J-lead devices
- Handling QFP devices
- Dry-packing J-lead and QFP devices
- Shipping J-lead and QFP devices in boxes

Handling J-Lead Devices

To protect device leads and ensure proper operation, J-lead devices must be handled carefully when they are stored, shipped, and transferred.

Storing & Shipping J-Lead Devices

Store and ship J-lead devices in tubes sealed with stoppers. If necessary, also add foam to the tubes for cushioning.

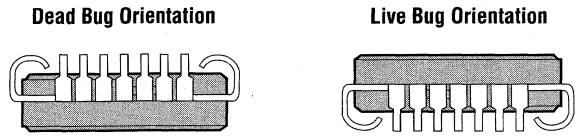
Tubes

Tubes protect J-lead devices during transportation and storage. Use clear tubes to allow easy inspection of the contents' top-side markings. The tube material should also be antistatic and stiff enough to prevent the tubes from warping, cracking, or developing burrs during normal handling. Follow these guidelines when transporting or storing devices in tubes:

- Tubes should have "antistatic" printed on them.
- Prevent devices from overlapping inside the tube.
- Keep tubes horizontal.
- Keep devices in "dead bug" orientation. See Figure 1.

☞ Use conductive tubes only when programming UV-erasable EPROM devices.

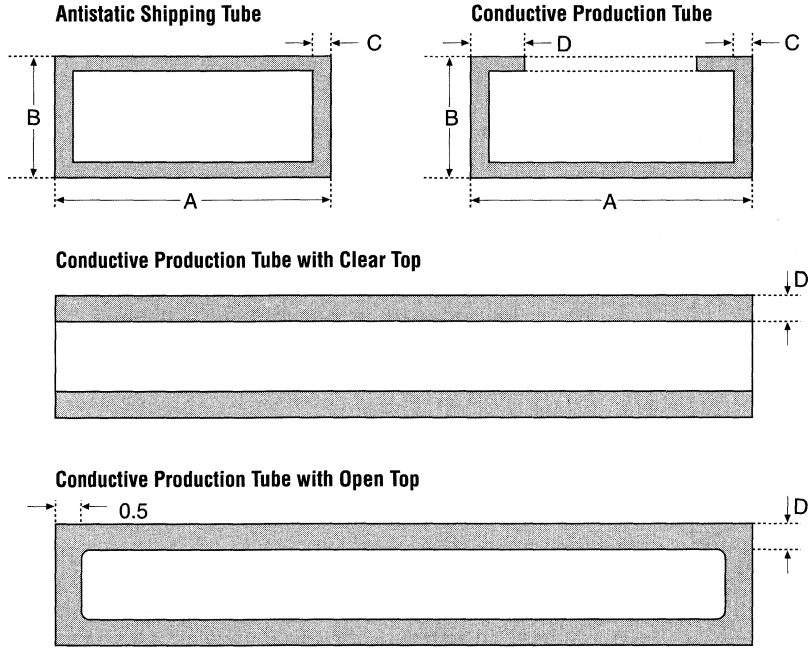
Figure 1. Dead Bug vs. Live Bug Orientation



The tubes must match the dimensions of the device. Figure 2 shows the tube dimensions required for each J-lead device.

Figure 2. Tube Dimensions for J-Lead Devices

Dimensions are shown in inches.



Pin Count	A	B	C	D	Shipping Length	Production Length
20	0.480	0.260	0.025	0.140	20.00	20.25
28	0.580	0.260	0.025	0.140	20.00	20.25
44	0.780	0.260	0.025	0.140	20.25	20.25
68	1.100	0.280	0.035	0.150	20.00	20.25
84	1.300	0.280	0.035	0.150	20.25	20.25

Table 1 lists the part numbers for Altera-approved tubes for J-lead devices.

Table 1. Tube Part Numbers for J-Lead Devices *Note (1)*

Pin Count	Altera Reference Part Number		Tube Capacity (Devices)
	Antistatic Tube	Conductive Tube	
20	E20-03708-00	P20-03784-01	49
28	E20-02078-00	P20-03780-01	39
44	E20-02079-00	P20-03694-01	26
68	E20-02080-00	P20-03693-01	18
84	E20-03710-00	P20-03781-03	15

Note:
(1) To order tubes, contact your local sales representative.

Stoppers

Stoppers seal tubes and protect devices against mechanical damage and electrostatic discharge (ESD). Altera uses black stoppers that match the tube dimensions. Follow these guidelines when inserting stoppers:

- Seat stoppers firmly into both ends of the tube when transporting or storing devices.
- Push stopper teeth fully inside the tube, with the grip extending outside for easy removal. Do not insert the stopper completely inside the tube. See Figure 3.

Figure 3. Stopper Properly Inserted into a Tube

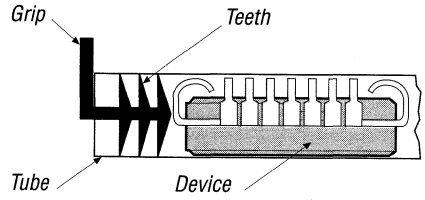


Table 2 lists the part numbers for Altera-approved black stoppers for J-lead devices.

Table 2. Black Stopper Part Numbers for J-Lead Devices *Note (1)*	
Pin Count	**Manufacturer Part Number**
20	K-VT0236-25
28	K-VT0236-12
44	K-VT0236-14
68	K-VT0236-16
84	K-VT0037B-03

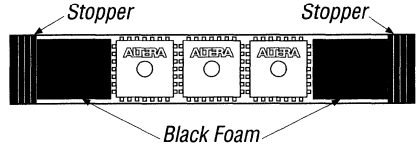
Note:
(1) To order stoppers, contact your local sales representative.

Foam

Foam provides extra cushioning and restricts movement inside the tube to prevent device pins from bending. When used, foam should be placed at each end of the tube between the stoppers and devices (see Figure 4). Foam should be antistatic, non-corrosive, and free of contaminants. Place foam in tubes containing:

- A gap inside the tube measuring 1/4-inch or greater
- Plastic J-lead chip carrier (PLCC) devices with 44 or more pins (full tubes containing PLCC devices with 28 or fewer pins do not generally need foam)
- Ceramic J-lead chip carrier (JLCC) devices

Figure 4. Stoppers, Foam & Devices in a Tube



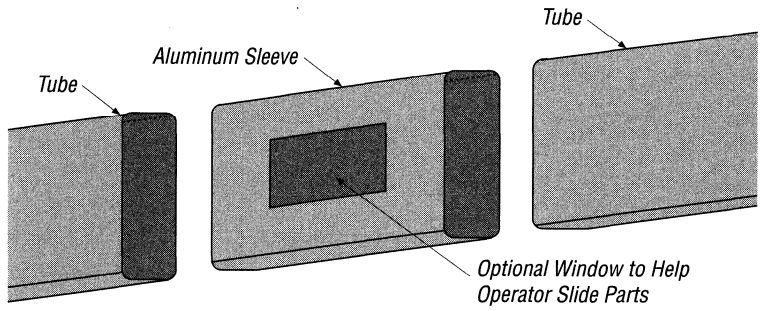
Transferring Devices between Tubes

To prevent leads from bending on tube edges, follow these steps when transferring devices from one tube to another:

1. Use a metal or plastic sleeve to line up tube ends (see Figure 5). If you do not have a sleeve, carefully line up the tube ends.

2. Tilt the tubes so that the devices slide from one tube to the other. Do not shake or vibrate the tubes.

Figure 5. Sleeve for Tube-to-Tube Transfer



Handling QFP Devices

To protect device leads, QFP devices must be handled carefully when they are stored, shipped, and transferred. QFP devices in carriers should be shipped only inside tubes sealed with stoppers and if necessary, with foam. QFP devices without carriers should be stored and shipped only in trays sealed with straps.

Handling QFP Devices in Carriers

Carriers are static-dissipative, molded plastic shells that hold QFP devices in a secure frame to prevent mechanical damage to device leads. Devices can be programmed and erased inside carriers. Follow these guidelines when handling QFP devices in carriers:

- Do not touch the QFP device; touch only the carrier using finger cots.
- Use only Altera QFP carrier extraction tools to extract QFP devices from carriers.
- Extract QFP devices directly into trays.
- Inspect the orientation and lead integrity of QFP devices after extracting them from carriers.

If you need to insert a QFP device into a carrier, contact Altera Customer Marketing at (408) 894-7104. Go to the *QFP Carrier & Development Socket Data Sheet* for more information on QFP carriers.

Tubes

Use only tubes to protect QFP devices in carriers during transportation. Clear tubes should be used to allow easy inspection of the contents' top-side markings. The tube material should also be antistatic and stiff enough to prevent tubes from warping, cracking, or developing burrs during normal handling.

Follow these guidelines when transporting QFP devices in carriers inside tubes:

- Tubes should have "antistatic" printed on them.
- Prevent devices in carriers from overlapping inside the tube.
- Keep tubes horizontal.
- Keep devices in dead bug orientation. See Figure 1 on page 684.
- Seal tubes with stoppers. If necessary, add foam to tubes.

Table 3 lists the part numbers for Altera-approved tubes for QFP devices in carriers.

Table 3. Altera-Approved Tubes for QFP Devices in Carriers *Note (1)*

Pin Count	Package Dimensions (mm)	Tube Capacity (QFP Devices in Carriers)	Altera Reference Part Number
100	14 × 20	23	E20-04726-00
160	28 × 28	14	E20-04743-00
208	28 × 28	14	E20-04743-00
240	32 × 32	12	E20-0408-00-00
304	40 × 40	10	E20-0408-01-00

Note:
(1) To order tubes, contact your local sales representative.

Go to "Transferring Devices between Tubes" on page 686 for information on how to transfer devices between tubes.

Stoppers

Stoppers seal tubes and protect devices against mechanical damage and ESD. Altera uses stoppers that match specific tube dimensions. Follow these guidelines when inserting stoppers:

- Seat stoppers firmly into both ends of a tube for both transportation and storage.
- Push stopper teeth fully inside the tube, with the grip extending outside for easy removal. Do not insert the stopper completely inside the tube. See Figure 3 on page 685.

Table 4 lists the reference part numbers for Altera-approved black stoppers for QFP devices in carriers.

Table 4. Black Stopper Part Numbers for QFP Devices in Carriers *Note (1)*	
Pin Count	**Altera Reference Part Number**
100	K-VT0236-16
160	E20-047-50-00
208	E20-047-50-00
240	*Note (2)*
304	*Note (2)*

Notes:
(1) To order stoppers, contact your local sales representative.
(2) Contact Altera Applications for the reference part number.

Foam

Foam provides extra cushioning and restricts movement inside tubes to prevent device pins from bending. When used, foam should be placed at each end of the tube between the stoppers and devices (see Figure 4 on page 686). Foam should be antistatic, non-corrosive, and free of contaminants. Add foam to tubes containing a gap inside the tube measuring 1/4-inch or greater.

Handling QFP Devices Without Carriers

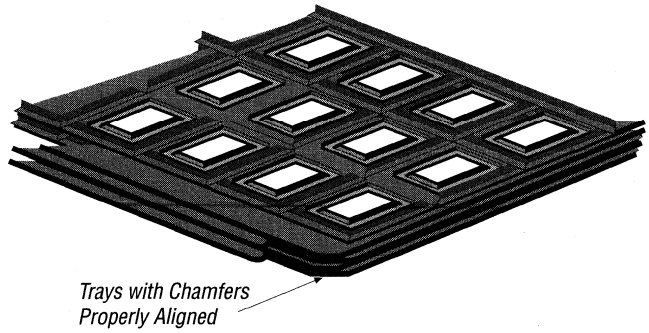
QFP devices ordered without carriers and QFP devices that have been extracted from carriers are stored only in trays sealed with straps.

Trays

To hold QFP devices not in carriers, use only Altera-approved trays—full-sized Peak Plastic Corporation trays and 1/3-sized ITW Camtex trays. Other JEDEC-approved trays are not as protective of Altera's QFP devices because they are manufactured to different nominal specifications. When stacking trays for transportation or storage, follow these guidelines:

- Seal stacks of trays with straps.
- Make sure all trays are of the same revision. The revision is indicated by the letter following "Rev."
- Align all pin-one chamfers on the trays together. See Figure 6.
- Align trays and ensure that they are seated properly before strapping them.
- Stack power quad flat pack (RQFP) trays no higher than 5 trays (4 trays containing devices and 1 cover tray).
- Stack plastic quad flat pack (PQFP) trays no higher than 7 trays (6 trays containing devices and 1 cover tray).

Figure 6. Properly Aligned Peak Trays



All of the full-size Peak Plastic Corporation trays used by Altera can withstand temperatures up to 180° C. These heat-resistant trays are rigid and can endure baking at 125° C—the recommended temperature for dehydrating moisture-sensitive devices. Table 5 lists the part numbers for Altera-approved, low-profile trays.

Table 5. Altera-Approved Trays for QFP Devices *Note (1)*

Package	Package Dimensions (mm)	Tray Capacity (Devices)	Peak Part Number *Note (2)*	Altera Reference Part Number
32-pin TQFP	7 × 7	250	ND-0707-1.0-1025-*n*	E20-03548-00
44-pin TQFP	10 × 10	160	ND-1010-1.0-0820-*n*	E20-03549-00
44-pin QFP	10 × 10	96	ND-1010-2.0-0616-*n*	E20-03550-00
100-pin TQFP	14 × 14	90	ND-1414-1.0-0615-*n*	E20-03551-00
100-pin QFP	14 × 20	66	ND-1420-2.7-0611-*n*	E20-03544-01
132-pin QFP	JEDEC	36	NX-PQFP-132-0409-*n*	E20-03355-00
160-pin QFP	28 × 28	24	ND-2828-3.5-0308-*n*	E20-04746-00
208-pin QFP	28 × 28	24	ND-2828-3.5-0308-*n*	E20-04746-00
240-pin QFP	32 × 32	24	ND-3232-3.4-0308-*n*	E20-04267-00
304-pin QFP	40 × 40	12	ND-4040-3.8-0206-*n*	E20-03552-00

Notes:

(1) To order 100 trays or less, contact EcoTech at (408) 988-2050. To order more than 100 trays, contact Peak Plastics Corporation (USA) at (415) 369-2544.

(2) For trays that can withstand 180° C, $n = 8$. For trays that can withstand 150° C, $n = 6$.

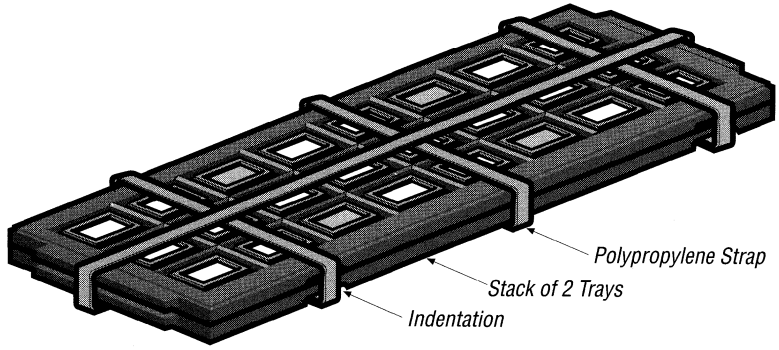
Straps

Straps secure trays and prevent devices from jostling during transportation and storage. To hold trays together during transportation, Altera recommends using at least 1/2-inch-wide polypropylene straps that can withstand temperatures up to 130° C in case you need to bake the QFP devices before mounting. When storing devices, Altera recommends using either velcro or polypropylene straps. Velcro straps that are 20 inches in length are sufficiently long to bind stacks of 2 to 7 trays for storage. Follow these guidelines when you strap trays together for shipping:

- Use only polypropylene straps. (Although velcro straps can hold trays together during storage, they lack the strength required to hold trays together during transportation.)
- Set the tension on the strapping machine high enough to prevent straps from sliding off a stack of trays.
- Secure three heat-sealed polypropylene straps across the width of the stack, placing two of the straps in the indentations on the long sides of the trays. See Figure 7.
- Secure one polypropylene strap across the length of the tray.
- Remove straps with a knife to prevent jostling devices in the trays.

Do not use rubber bands, masking tape, string, or other similar material in place of velcro or polypropylene straps.

Figure 7. Properly Secured Polypropylene Straps on a Stack of Trays

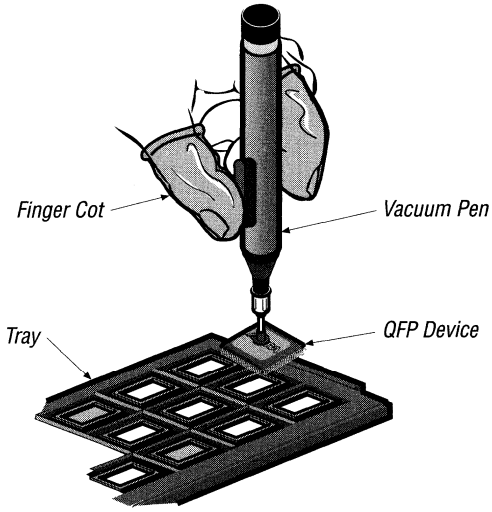


Transferring QFP Devices between Trays

Altera recommends using automated pick-and-place machines in an ESD-protected environment to transfer QFP devices between trays. If you need to transfer QFP devices manually, follow these guidelines:

- Work in an ESD-protected environment.
- Use ground straps and finger cots.
- Only use vacuum pens to manually transfer QFP devices. Vacuum pens should be able to maintain their vacuum for at least four seconds. See Figure 8.
- Transfer devices right-side-up over a table; then release the vacuum only after the device is properly oriented and seated in the tray.
- QFP device leads should never contact the tray.

Figure 8. Transferring a QFP Device Using a Vacuum Pen



Dry Packing J-Lead & QFP Devices

Dry packing is a method of packing moisture-sensitive devices for shipment. Risk to moisture-sensitive devices can occur when moisture is exposed to the high soldering temperatures of the reflow process. Although many of Altera's J-lead and QFP devices are not sensitive to moisture, Altera has adopted dry packing as a standard practice for moisture-sensitive devices to eliminate all risk of moisture to those devices. In addition, Altera can dry-pack other devices upon request. Prior to dry packing, the devices are baked to remove any existing moisture and then vacuum-sealed in moisture-barrier bags. Table 6 lists the contents of a typical dry pack.

Table 6. Dry Pack Contents

Item	Specification
Moisture-barrier bag	MIL-B-81705C, Type 1 or equivalent
Desiccant	MIL-D-3464, Type II or equivalent
Humidity-indicator card	Compliant with MIL-I-8835A
Labels	ID label and caution label

To maintain a moisture-free environment, follow these guidelines after receiving dry-packed devices from Altera:

- Open bags as close to the seal as possible to leave enough of the bag for resealing.
- Reseal bags after opening to minimize exposure to moisture.
- Inspect all dry packs for potential leaks in the seals or bags.
  - If a leak exists and the humidity-indicator card shows an unacceptable humidity level (i.e., the 30% dot has started to turn pink), rebake the devices.
  - If a leak exists but the humidity-indicator card shows an acceptable humidity level (i.e., the 30% dot is blue with no pink), reseal the devices in an undamaged bag.
- After opening dry packs, check that the humidity-indicator card shows acceptable humidity. If the card shows an unacceptable humidity level, rebake the devices.
- Rebake devices prior to mounting if the interval between opening a dry pack and mounting the devices onto a board exceeds the floor life of the devices (see Table 7).
- Rebake any devices stored for over one year.

Table 7 lists the floor life of devices currently baked and dry-packed by Altera. The floor life is the length of time a device can be exposed to a factory environment after the device has been removed from the bag and before it is mounted.

Table 7. Floor Life of Standard Dry-Packed Product at Altera

Package	Storage Conditions *(2)*	Floor Life (Hours) *(1)*		
		At OEM	At Distributor *(3)*	Total
1-mm thin quad flat pack (TQFP), all packages	< 30° C / 60% R.H.	24	24	48
PQFP, 100 or more pins, *(4)*	< 30° C / 60% R.H.	120	24	144
RQFP, all packages	< 30° C / 60% R.H.	24	6	30
PLCC, 84 pins (selected devices)	< 30° C / 60% R.H.	120	24	144
BGA, all sizes	< 30° C / 60% R.H.	24	24	48

Notes to table:

(1) These times are based on experiments simulating infrared-reflow processes with peak temperatures of 235° C.
(2) The abbreviation R.H. stands for relative humidity.
(3) These times include programming time, if applicable.
(4) FLASHlogic 132-pin devices in a PQFP package has a floor life of 48 hours (24 hours at the OEM and 24 hours at the distributor).

Altera recommends the following guidelines when dry-packing devices:

- Bake QFP devices in heat-resistant trays at 125° C for at least 12 hours.
- Bake J-lead devices in heat-resistant tubes at 125° C for at least 12 hours. If you lack heat-resistant tubes, bake J-lead devices on a cookie sheet in dead-bug orientation.
- Use heat-sealed bags that are resistant to punctures and abrasion.
- Seal bags with a bag-sealing machine that can evacuate the air inside a bag. Relax the vacuum enough to prevent the bag from contracting so tightly over the tube or tray ends that it risks puncture.
- Replace the desiccant and humidity indicator card if the dry pack is open for longer than one hour.
- Use at least one unit of desiccant per dry pack.

Shipping J-Lead & QFP Devices in Boxes

When shipping trays or tubes of devices, use only boxes that have passed the ASTM D776 test for shipping containers. To protect against ESD, Altera recommends that you use boxes with an internal, conductive finish. Filler material is added to boxes to cushion the contents and prevent trays or tubes from shifting position during shipping. Boxes should contain enough filler material to prevent stoppers from falling out of tubes when jostled. Filler material should meet the following standards:

- Filler materials should be antistatic and non-corrosive.
- Filler materials should not crumble, flake, powder, outgas, or shed.
- Filler materials should not scratch or puncture the trays, tubes, or dry-pack bags.

Selecting Sockets for Altera Devices

June 1996, ver. 1 Application Note 80

Introduction

Altera offers a number of surface-mount packages. Surface-mount assembly places unique demands on the development and manufacturing process by requiring different CAD symbols for printed circuit board (PCB) layout, different soldering processes for production (reflow vs. wave solder), and different test and reliability issues. Bonding programmable devices to a PCB also prevents designers from conveniently erasing and reprogramming the device, an important part of design development.

Socketing the surface-mount devices is a popular compromise. Conventional mounting techniques can be used on the socketed devices, either by through-hole soldering them to a PCB or by mounting them onto a socketed carrier board for wire-wrap applications.

This application note discusses the following topics:

- Mechanical considerations for J-lead sockets
- Socket evaluation for J-lead packages
- Socket evaluation for QFP packages
- Socket evaluation for BGA packages
- Packaging operations for wire-wrap applications
- Socket manufacturers

Mechanical Considerations for J-Lead Sockets

J-lead devices make contact with electrical sockets from either the bottom or the side of the leads. Depending on how the devices are held in place, the sockets can bend the leads and make the electrical contact unreliable. Accordingly, the designer must consider the type of package, the number of device insertions and removals, and the amount of lead deformation before choosing a socket.

Burn-in sockets are zero-insertion-force sockets that do not deform a device's leads. Currently, burn-in sockets have dimensions similar to those of production sockets, making them the best option for prolonging the life of a reprogrammable device during prototyping, while still allowing the use of production sockets later in the design process.

Once a design enters the production phase, cost becomes a major concern. As a result, low-cost production sockets, designed to hold a device permanently and securely, are widely available. However, these sockets must exert a reasonable force on the device leads to prevent the device from popping out of the socket. After several insertions, this force can deform the leads, causing them to short out or fail to make contact, rendering the device unusable. Therefore, Altera strongly recommends using a burn-in socket during the design and development phases of a project, and a low-cost production socket during the production phase.

Production sockets must be chosen carefully. If an erasable device must be removed more than 10 times for reprogramming, it is preferable to use non-deforming, low-insertion-force (burn-in) sockets. In high-stress environments (e.g., strong G-forces, thermal shock, high humidity), sockets with high-insertion forces and optional retention clips are needed. To reduce the possibility of damaging device pins, most manufacturers of high-quality sockets include a stand-off mechanism inside the socket that prevents a device from being forced too far into a socket.

Socket Evaluation for J-Lead Packages

Altera tested available production sockets for use with 44-, 68-, and 84-pin windowed ceramic J-lead (JLCC) packages. Although testing was performed using JLCC packages, the following information also applies to plastic J-lead chip carrier (PLCC) devices. Each socket was subjected to three tests:

- The change in the gap between the corner pins of each device was measured before and after each of the 10 insertions.
- Each pin of the socket was wired in series and tested for open or short circuits lasting longer than 10 µs. This open-and-short circuit test was performed while the socket was attached to a vibration block. The amplitude of vibration was 3.0 mm peak-to-peak at a frequency that varied from 10 Hz to 55 Hz to 10 Hz, in 1-minute cycles for 2 hours. The vibration test was performed on all three axes at a temperature of 70° C.
- The actual point of contact between the socket pin and the device lead was photographed to determine the direction of the forces and the amount of surface contact between them.

Altera tested sockets from eight manufacturers. Tables 1, 2, and 3 show the results of the 44-, 68-, and 84-pin production sockets that passed the open-and-short circuit test. Sockets are ranked by their ability to maintain the device's pin integrity after multiple device insertions.

Table 1. Summary of 44-Pin Production Socket Analysis

Vendor & Part Number	Comments
Augat, Inc. PCS-044A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
AMP, Inc. 821575-1	Moderate pin deformation. Contact force has a downward component. No retainer clip option.

Table 2. Summary of 68-Pin Production Socket Analysis

Vendor & Part Number	Comments
Augat, Inc. PCS-068A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
ITT/Cannon Corporation LCS-68-2	Low pin deformation. Contact force has a downward component. Has a retainer clip option.
AMP, Inc. 821574-1	Moderate pin deformation. Contact force has a downward component. No retainer clip option.

Table 3. Summary of 84-Pin Production Socket Analysis

Vendor & Part Number	Comments
Augat, Inc. PCS-084A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
ITT/Cannon Corporation LCS-84-2	Moderate pin deformation. Contact force has a downward component. Has a retainer clip option.
AMP, Inc. 822151-1 (for surface mount)	Moderate pin deformation. Contact force has a downward component. No retainer clip option. Designed for plastic packages.
AMP, Inc. 821573-1	Large pin deformation. Very tight fit. No retainer clip option. Due to pin deformation, Altera recommends a maximum of three insertions. Designed for ceramic packages.
Burndy Corporation QILE-84P-410T	Large pin deformation. Very tight fit. No retainer clip option. Due to pin deformation, Altera recommends a maximum of three insertions.

Vendors may provide additional information about their products, such as material selection, prevention of solder ingress during wave soldering, or lead shape. Altera recommends qualifying sockets before committing to a particular vendor.

Table 4 shows the contact distances for Altera packages. These measurements should be used to select a socket, preferably with internal stand-offs, for use with Altera devices.

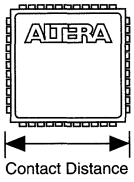


Table 4. Device Contact Distances

Package	Pins	Contact Distance (Minimum mils)	Contact Distance (Maximum mils)
PLCC	20	385	395
PLCC, JLCC	28	485	495
PLCC, JLCC	44	685	695
PLCC, JLCC	68	985	995
PLCC, JLCC	84	1,185	1,195

Socket Evaluation for QFP Packages

Because QFP packages are more susceptible to lead deformation, production sockets must be rigorously qualified. Altera recommends using a burn-in socket for QFP packages because of the sockets' reliability. While sockets should always be qualified, Table 5 suggests sockets based on the number of pins and type of QFP package.

Table 5. Socket Vendor Information

Package Type	Number of Pins	Socket Vendor	Part Number
TQFP	32	Yamaichi	IC51-0324-1498
TQFP	44	Yamaichi	IC51-0804-808
PQFP	44	Yamaichi	IC51-467-KS11258
TQFP	100	Yamaichi	IC51-1004-809
PQFP, CQFP	100	Yamaichi	IC51-1004-814-2
QFP	132	Yamaichi	IC51-1324-828
PQFP, RQFP	160	Yamaichi	IC51-1604-845-4
RQFP	208	Yamaichi	IC51-2084-1052-11
RQFP (round heat sink)	208	Yamaichi	IC51-1052KS-13804
CQFP	208	Yamaichi	IC51-1509-KS14057
PQFP (EPX8160)	208	Yamaichi	IC51-1052-KS14025
PQFP	208	Yamaichi	IC51-2084-1052-11
RQFP	240	Yamaichi	IC51-1655KS-13666
RQFP (round heat sink)	240	Yamaichi	IC51-2404-1655-2
CQFP	240	Enplas	FPQ-240-0.5-05

Socket Evaluation for BGA Packages

Lead deformation is not a concern when considering BGA packages because the leads are solder balls. Therefore, a burn-in socket can be used if a customer intends to replace the device. See Table 6.

Table 6. Socket Vendor Information

Package Type	Number of Pins	Socket Vendor	Part Number
BGA	169	Enplas	BGA-169(225)-1.5-01A

Packaging Operations for Wire-Wrap Applications

Wire-wrap applications require a through-hole mount compatible with the J-lead package. The sockets specified do not typically conform mechanically to most wire-wrap panels. Wire-wrap cards have machine receptacles in rows with 100-mil spacing between receptacles and 300-mil spacing between rows. Carrier boards provide an effective way to bridge the gap. Mounting a socket to a carrier board provides the convenience of wire wrap, and the socket occupies a relatively small area on a device. Some carrier boards have signal routing with shorter paths or 45° bends to minimize signal reflection.

Socket Manufacturers

Telephone numbers for the manufacturers mentioned in this application note are listed in Table 7. Contact the appropriate manufacturer for additional information.

Table 7. Socket Manufacturers

Product	Company	Telephone Number
Production sockets	3M/Textool Corporation	(800) 328-0411
	AMP, Inc.	(800) 522-6752
	Augat, Inc.	(508) 699-9800
	Burndy Corporation	(408) 245-2590
	ITT/Cannon Corporation	(714) 261-5300
Test and burn-in sockets	3M/Textool Corporation	(800) 328-0411
	AMP, Inc.	(800) 522-6752
	Advanced Interconnections Corporation	(401) 823-5200
	Dai-Ichi Seiko Company, Ltd. (Japan)	(81) 0482-53-3131
	Emulation Technology, Inc.	(408) 982-0660
	Yamaichi	(408) 456-0797
	Enplas	(415) 572-1682
Carrier boards and wire-wrap adapters	Advanced Interconnections Corporation	(401) 823-5200
	Emulation Technology, Inc.	(408) 982-0660

Information in this application note is based on tests performed by Altera and on information provided to Altera by various vendors. Altera assumes no liability for the use of third-party products mentioned in this document.

Reflow Soldering Guidelines

for Surface-Mount Devices

June 1996, ver. 1 Application Note 81

Introduction

Altera's surface-mount products include quad flat pack (QFP), J-lead chip carrier (JLCC and PLCC), ball-grid array (BGA), and small-outline integrated circuit (SOIC) devices, as well as QFP development sockets. Several soldering methods exist, but forced-air convection and infrared reflow soldering (or a hybrid) are the most common ways to secure surface-mount devices to printed circuit boards (PCBs). These reflow processes consist of applying a eutectic solder paste to a circuit board, placing devices onto the paste, drying the paste, and then conveying the board through an oven with successive heating elements of varying temperatures. In the oven, each board typically passes through a gradual, preheating stage followed by a brief duration at the higher soldering temperature. This maximum temperature, the rate of heating, and the time a device spends at each temperature are the most critical parameters for effective soldering.

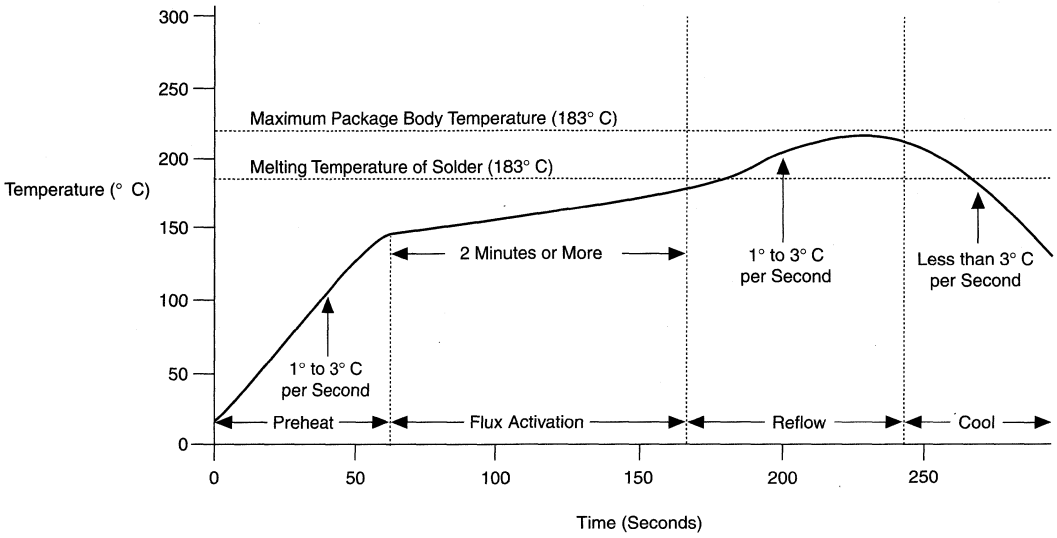
Customers' experiences have shown that Altera's surface-mount products can be successfully mounted on boards over a wide range of temperatures. Any plastic package, especially if it is sensitive to moisture, can be damaged by an inappropriate reflow process. Although Altera is not in the business of performing board assembly, guidelines for reflow processes have been developed. These guidelines are based on extensive experiments that subject Altera devices to the controlled introduction of moisture, simulation of infrared and vapor-phase reflow, and temperature cycling. Altera cannot specify a universally optimal temperature profile without knowing each customer's board design, application, and available equipment. However, the following recommendations do provide adequate guidelines and limits to ensure that devices are not unduly stressed.

Temperature Profiles

Because different board designs use different solder paste, circuit boards, number of devices, and types of devices, no single temperature profile will work for all PCBs. However, Figure 1 shows a sample temperature profile based on successful profiles used by Altera. The graph illustrates the four basic stages of a reflow oven:

- Preheat
- Flux Activation
- Reflow
- Cool

Figure 1. Temperature Profile for Infrared or Convection Reflow



Reflow

In the preheat stage, the solder paste dries while its more volatile ingredients evaporate. After preheating, the leads should be kept at about 150° C for a minimum of two minutes so the flux in the paste can clean the bonding surfaces properly. During the flux activation stage, the solder on all areas of the board should be roughly the same temperature. The devices enter the reflow stage when the temperature increases at a rate of 1° to 3° C per second. To prevent warping, bridging, and cold solder joints, keep the leads above the solder's melting point (about 183° C) for at least 60 seconds. Ideally, the leads should only be subjected to the peak temperature (220° C) for approximately 10 seconds to reduce the risk of damage to the solder and devices. In addition, the device body temperature—which may vary from the temperature of the leads by as much as 15° C—should not exceed 220° C.

Post-Reflow Cooling

The reflow stage is complete when the molten solder connections cool and solidify to form strong solder joint fillets. A fast cooling rate reduces the grain size of the intermetallic compounds and strengthens the solder joints. However, due to the risk of thermal shock, cooling should be less than 3° C per second.

Post-Reflow Cleaning

After the soldering process, a simple wash with deionized water sufficiently removes most residues from the board assembly. Most board-assembly manufacturers use either water-soluble fluxes with a tap water wash, or "no-clean" fluxes that do not require cleaning after reflow.

Reflow Tips

The following tips provide information on how to optimize the reflow process:

- For more uniform heating, use convection and hybrid ovens rather than plain, infrared ovens. Some boards (especially those with large devices or sockets) require these fine-tuned ovens that provide uniform temperatures to all devices on the board.
- Use an oven with more heating elements on both its floor and ceiling to minimize temperature variations, deliver precise temperature, and provide the necessary heat to board areas that might be shielded. Simply having fewer heating elements in an oven may not permit enough temperature control.
- Place thermocouples on the leads and bodies of the devices. Monitor the lead temperatures to ensure good solder joints, and monitor the device body temperatures to protect the devices. The difference between the lead and device body temperatures can be as high as 15° C. Therefore, it is risky to rely on temperature measurements at only one location.
- Adjust the reflow duration to create good solder joints without raising the device body temperature beyond the allowed maximum of 220° C.

Moisture-Sensitivity of Devices

Semiconductor sensitivity to moisture becomes an important issue as board assemblers switch to hotter and faster reflow processes. Any non-hermetic package can absorb moisture. Like popcorn, the moisture in some plastic packages can vaporize and expand rapidly due to high temperature. Cracks or delamination (a slight separation of the plastic from the die or leadframe inside a device) may then occur. Delamination sometimes, but not always, degrades devices.

Altera is dedicated to improving package materials to reduce the risk of moisture-induced damage. Nevertheless, as a precaution, Altera currently bakes and dry-packs devices in the following packages: thin quad flat pack (TQFP), power quad flat pack (RQFP), plastic quad flat pack (PQFP) devices with 100 leads or more, and some 84-lead PLCC devices. Based on the sensitivity of each device to moisture, Altera has specified the floor life of each package, which is

the maximum recommended time between removing devices from a dry pack and soldering them onto a PCB. To determine the floor life for each potentially moisture-sensitive device, Altera forced moisture into sample packages, then subjected them to typical reflow temperatures and temperature cycling. The devices were subsequently tested electrically and analyzed physically with x-ray and acoustic microscopy to gauge their sensitivity to moisture. Altera performs moisture sensitivity tests according to *Procedures for Characterizing and Handling of Moisture-/Reflow-Sensitive ICs* (IPC-SM-786A), the standard from the Institute for Interconnecting and Packaging Electronic Circuits. Further reliability and solder tests demonstrated that 220° C is both a satisfactory and safe maximum body temperature for Altera's devices during reflow (i.e., 220° C is adequate for soldering devices onto PCBs ***and*** 220° C is the maximum safe temperature).

Reflow of Moisture-Sensitive Devices

Once the moisture-sensitive devices are removed from their dry packs or other controlled environments, the devices should be soldered onto the PCB within the floor life specified on the dry pack's label. Devices can be stored indefinitely in a desiccant cabinet, a controlled environment kept at less than 30° C and 20% relative humidity. If a device is exposed to too much moisture, bake it for 12 hours at 125° C to revitalize it, then mount the device within the specified floor life.

For more information about storing and handling moisture-sensitive devices, see *Application Note 71 (Guidelines for Handling J-Lead & QFP Devices)* in this data book.

During reflow, the device's body temperature should be kept below 220° C, and the rate of temperature change should be kept between 1° to 3° C per second. Based on Altera's testing, the devices can operate safely at any humidity level after reflow.

References

Institute for Interconnecting and Packaging Electronic Circuits, Inc. *Component Packaging and Interconnecting with Emphasis on Surface Mounting* (ANSI/IPC-SM-780). New York: Institute for Interconnecting and Packaging Electronic Circuits, Inc., 1988.

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Institute for Interconnecting and Packaging Electronic Circuits, Inc. *Test Methods Manual* (IPC-TM-650). New York: Institute for Interconnecting and Packaging Electronic Circuits, Inc., 1991.

JEDEC/Electronic Industries Association, Inc. *Moisture-Induced Stress Sensitivity for Plastic, Surface-Mount Devices* (JESD22-A112). New York: JEDEC/Electronic Industries Association, 1994.

Notes:

Technical Support
from Altera Applications

June 1996, ver. 3

Introduction

Altera's technical support team includes over 80 Applications Engineers dedicated to promptly resolving customers' technical issues. Altera responds to customers' questions promptly and efficiently via e-mail, telephone, or fax. Applications Engineers are located at Altera headquarters in San Jose, California, and at Altera offices around the world.

Altera Applications offers the following services:

- Technical support hotline
- Electronic mail
- Technical publications
- Altera Express
- World-wide web site
- Altera FTP site
- Bulletin board service
- CompuServe
- Training courses
- Design evaluations
- On-site support

13 General Information

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(408) 954-0348

Customers in the United States and Canada can receive direct technical support for Altera devices and software by calling Altera Applications at (800) 800-EPLD between the hours of 7:30 a.m. and 5:00 p.m. Pacific time. Customers outside the United States and Canada can receive technical assistance by calling an Applications Engineer at (408) 894-7000 between the hours of 7:30 a.m. and 5:00 p.m. Pacific Time, or by contacting their local Altera distributor or sales office. Customers can also fax technical support questions to (408) 954-0348.

Electronic Mail

sos@altera.com

Customers can use electronic mail (e-mail) to send technical questions about devices and software to Altera Applications at **sos@altera.com**. Altera e-mail is checked regularly throughout the day and is given the same priority as telephone calls. However, because e-mail delivery through the Internet can be delayed, either the technical support hotline or fax should be used for urgent issues.

Technical Publications

(408) 894-7144

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Altera produces a variety of technical literature to help customers select and design with programmable logic, including application notes and data sheets. Altera also provides *News & Views*, a quarterly newsletter that includes the latest information on Altera products, technical articles written by Altera Applications Engineers, and a question and answer section that addresses many commonly asked questions. All registered users of Altera products receive a free subscription to *News & Views*. Customers who wish to request Altera technical publications, or add their name to the *News & Views* mailing list, can contact Altera Literature Services at (408) 894-7144 or e-mail their requests to **lit_req@altera.com**. Technical literature is also available via Altera Express, the Altera world-wide web site, and the Altera FTP site.

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The Altera Express automated fax system allows customers to receive the latest Altera literature 24 hours a day, 7 days a week. Customers who wish to order documents or a catalog should simply dial one of the following numbers and follow the instructions. Customers in the United States or Canada can dial (800) 5-ALTERA; international customers can call (408) 894-7850 from a fax phone.

World-Wide Web Site

http://
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Altera provides a world-wide web (WWW) site for instant on-line access to the latest Altera product information. The site allows customers to browse through Altera product information and literature, press releases, a corporate profile, and employment opportunities. Access the Altera web site at **http://www.altera.com**, or contact the Altera Applications Department at (800) 800-EPLD for more information.

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Altera provides a 24-hour file transfer protocol (FTP) site for instant Internet access to the latest Altera product information. On-line versions of Altera application notes, application briefs, data sheets, and software utilities are available at **ftp.altera.com**. Customers can also use the FTP site to transfer design files to and from the Altera Applications Department for technical support and review.

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To access the Altera BBS, call (408) 954-0104. To connect to the BBS via modem, the following equipment and configuration is required:

- Bell Standard 212A, CCITT standard, or compatible modem
- Up to 14,400 baud rate
- 8 data bits, 1 stop bit, no parity

The following file transfer protocols are supported:

- ASCII (Non-Binary)
- Xmodem (Checksum)
- Xmodem (CRC)
- 1K-Xmodem
- Ymodem (Batch U/L and D/L)
- Zmodem (Batch U/L and D/L)
- Kermit

CompuServe

go altera

Altera provides CompuServe support through the "Altera Forum." Customers can use the Altera Forum library to upload and download files, leave messages for other users or for the Altera Applications department, or hold real-time interactive conferences. CompuServe provides a free introductory membership to each Altera customer. To access the Altera Forum, type `go altera` ↵ at the CompuServe command prompt.

Training Courses

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Altera provides a variety of training courses that teach innovative and efficient design techniques. With these courses, customers can discover the time-saving features of Altera's comprehensive MAX+PLUS II development system, explore the design features of Altera's device families, or simply learn more about Altera products.

Altera training courses are taught by Altera Applications Engineers. Small class sizes ensure that every student receives individual attention. Hands-on exercises with Altera devices and the MAX+PLUS II software reinforce lecture topics to maximize learning.

Altera's training program is divided into multiple courses that focus on various aspects of the Altera design environment. Course topics range from introductory programmable logic design to advanced architecture and design labs. Training courses are offered on a regular basis at locations throughout the world. On-site training is also available. For more information about Altera's training courses, customers can contact their local Sales Representative or the Altera Training Administrator at (408) 894-7000. A schedule of training courses is available from Altera's world-wide web site at **http://www.altera.com**.

Design Evaluations

Altera Applications Engineers and Field Applications Engineers can evaluate customer designs and recommend the most efficient design methods and the device(s) that will best fit customer needs. Altera will also estimate device performance. For more information, customers can contact their local Altera sales office.

On-Site Support

Altera Field Applications Engineers are located around the world to provide on-site technical support. They are available to evaluate customer designs, demonstrate the MAX+PLUS II software, and provide on-site training. Customers can contact their local Field Applications Engineer by calling their local Altera sales office.

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Notes:

Abbreviations

June 1996

The *1996 Data Book* uses the following abbreviations:

ACCESS	Altera Commitment to Cooperative Engineering Solutions
AHDL	Altera Hardware Description Language
AMPP	Altera Megafunction Partners Program
AN	Application note
APD	Active parallel down
APU	Active parallel up
AS	Active serial
ASCII	American Standard Code for Information Interchange
ASIC	Application-specific integrated circuit
ASSP	Application-specific standard product
ATM	Asynchronous Transfer Mode
BBS	Electronic bulletin board service
BGA	Ball-grid array
BNF	Backus-Naur form
BPR	Bypass register
BSC	Boundary-scan cell
BSDL	Boundary-Scan Description Language
BST	Boundary scan testing
CAE	Computer-aided engineering
CAS	Column-address strobe
CCD	Charge-coupled device
CerDIP	Ceramic dual in-line package
CMD	Command File
CMOS	Complementary metal-oxide semiconductor
CPLD	Complex programmable logic device
CPU	Central processing unit
CQFP	Ceramic quad flat pack
CRC	Cyclic redundancy check
DIP	Dual in-line package
DRAM	Dynamic random access memory
DS	Data sheet
DSP	Digital signal processing
DUT	Device under test
EAB	Embedded array block
EAU	Electronic Application Utility
EDA	Electronic Design Automation

EDF	EDIF Input File
EDIF	Electronic Design Interchange Format
EEPROM	Electrically erasable programmable read-only memory
EPLD	Erasable Programmable Logic Device
EPROM	Erasable programmable read-only memory
ESD	Electrostatic discharge
FFT	Fast Fourier transform
FIFO	First-in-first-out
FIN	Fitter Input File
FIR	Finite impulse response filter
FIT	Fit File
FLEX	Flexible Logic Element MatriX
FPGA	Field-programmable gate array
FTP	File transfer protocol
GAL	Gate array logic
GDF	Graphic Design File
HDL	Hardware description language
HEX	Hexadecimal File
IC	Integrated circuit
ICR	In-circuit reconfigurability
IEEE	Institute of Electrical and Electronic Engineers
IIR	Infinite impulse response
INC	Include File
INI	Initialization File
I/O	Input/output
IOC	Input/output cell
IOE	Input/output element
IR	Instruction register
ISA	Industry-standard architecture
ISP	In-system programmability
JCF	JTAG Chain File
JED	JEDEC File
JLCC	Ceramic J-lead chip carrier
JTAG	Joint Test Action Group
LAB	Logic array block
LCA	Logic cell array
LE	Logic element
LED	Light-emitting diode
LMF	Library Mapping File
LOG	Log File
LPM	Library of parameterized modules
LSB	Least significant bit
LSI	Large-scale integration
LUT	Look-up table
MAC	Multiplier-accumulater

MAX	Multiple Array MatriX
MD-SAS	Multi-device sequential active serial
MMF	MAX+PLUS II Message File
MPLD	Mask-Programmed Logic Device
MPU	Master programming unit
MSB	Most significant bit
MSI	Medium-scale integration
MSPS	Million samples per second
MTBF	Mean time between failures
MTF	Message Text File
NRE	Non-recurring engineering
OEM	Original equipment manufacturer
OTP	One-time-programmable
PAL	Programmable array logic
PC	Personal computer
PCB	Printed circuit board
PCI	Peripheral component interconnect
PDIP	Plastic dual in-line packages
PGA	Pin-grid array
PIA	Programmable interconnect array
PIB	Product information bulletin
PLCC	Plastic J-lead chip carrier
PLD	Programmable logic device
PLL	Phase-locked loop
POF	Programming Object File
POR	Power-On Reset
PPA	Passive parallel asynchronous
PPS	Passive parallel synchronous
PQFP	Plastic quad flat pack
PROM	Programmable read-only memory
PS	Passive serial
QFP	Quad flat pack
RAM	Random access memory
RBF	Raw Binary File
RH	Relative Humidity
ROM	Read-only memory
RPT	Report File
RQFP	Power quad flat pack
RTL	Register transfer level
SBF	Serial Bitsteam Files
SNF	Simulator Netlist File
SOF	SRAM Object File
SOIC	Small-outline integrated circuit
SRAM	Static random access memory
SSG	Synchronous signal generator
SSI	Small-scale integration

SVF	Serial vector format file
SYM	Symbol File
TAP	Test access port
TDF	Text Design File
TDO	Text Design Output File
TDX	Text Design Export File
TQFP	Thin quad flat pack
TTF	Tabular Text File
TTL	Transistor-to-transistor logic
UES	User electronic signature
UV	Ultraviolet
VEC	Vector File
VHD	VHDL Design File
VHDL	VHSIC Hardware Description Language
VHSIC	Very high speed integrated circuit
VHO	VHDL Output File
VLSI	Very large-scale integration
VO	Verilog Output File
WDF	Waveform Design File
WWW	World-wide web
WYSIWYG	What-you-see-is-what-you-get
XNF	Xilinx Netlist Format File
ZIF	Zero -insertion -force

Glossary

June 1996

A

Altera Hardware Description Language (AHDL) Altera's design entry language. AHDL is a high-level, modular language that is completely integrated into MAX+PLUS II. You can create AHDL Text Design Files (**.tdf**) with the MAX+PLUS II Text Editor or any standard text editor, then compile, simulate, and program your projects within MAX+PLUS II. AHDL supports Boolean equations, state machines, conditional, and decode logic. AHDL also allows you to create and use parameterized functions, and includes full support for functions in the library of parameterized modules (LPM).

Altera Megafunction Partners Program (AMPP) An alliance between Altera and developers of synthesizable megafunctions, created to encourage and increase the use of megafunctions in programmable logic device (PLD) designs.

array clock A clock signal that passes through the logic array of a device before arriving at the clock input of a register.

Assembler The Compiler module that creates one or more Programmer Object Files (**.pof**), SRAM Object Files (**.sof**), and optional JEDEC Files (**.jed**) for programming Altera devices.

Assignment & Configuration File (.acf) An ASCII file that stores information about probe, resource, and device assignments for a hierarchy tree, as well as configuration information for the Compiler, Simulator, Timing Analyzer, and Programmer. All information that can affect output files containing design information for the current hierarchy tree is controlled by the ACF.

B

BBS Bulletin board service. An Altera Applications Department bulletin board service that provides continuous, round-the-clock access to up-to-date device and development tool information, electronic application notes and briefs, customer newsletters, and software utility programs. The telephone number for the Altera BBS is (408) 954-0104.

BGA Ball-grid array. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

BitBlaster A serial download cable that allows both PC and workstation users to program and configure devices in-system or in-circuit. The BitBlaster provides programming support to MAX 9000, MAX 7000S, and FLASHlogic devices, and configuration support for FLEX 10K, FLEX 8000, and FLASHlogic devices. Multi-device JTAG chain configuration is also available for FLEX 10K, FLEX 8000, and FLASHlogic devices. Multi-device JTAG chain programming is available for MAX 9000, MAX 7000S, and FLASHlogic devices.

C

carry chain A dedicated architectural feature of the FLEX 10K and FLEX 8000 device families that provides a high-performance carry-forward function between logic elements. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry

chain, and feeds into both the LUT and the next portion of the carry chain. This carry-forward function is ideal for adders, counters, and comparators.

cascade chain A dedicated architectural feature of the FLEX 10K and FLEX 8000 families that allows implementation of high-performance, wide fan-in functions. Adjacent LUTs can be used to compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain is available only in FLEX 10K and FLEX 8000 devices.

CerDIP Ceramic dual in-line package. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

Classic An Altera device family based on Altera's original EPROM-based EPLD architecture. The Classic device family includes the EP600I, EP610, EP610I, EP900I, EP910, EP910I, EP1800I, and EP1810 devices.

Compiler Netlist Extractor The MAX+PLUS II Compiler module that converts each design file in a project to a single database format. The Compiler Netlist Extractor also checks each design file in a project for problems such as duplicate node names, missing inputs and outputs, and outputs that are tied together.

Configuration EPROM Altera's family of serial EPROMs, which are designed to configure FLEX 10K and FLEX 8000 devices. This device family includes the EPC1064, EPC1064V, EPC1213, and EPC1.

configuration scheme The method used to load data into a FLEX devices.

Four configuration schemes are available for FLEX 10K devices: passive serial (PS), passive parallel asynchronous (PPA), passive parallel synchronous (PPS), and JTAG. For complete information on FLEX 10K configuration schemes, see *Application Note 59 (Configuring FLEX 10K Devices)*.

Six configuration schemes are available for FLEX 8000 devices: active serial (AS), active parallel up (APU), active parallel down (APD), passive parallel asynchronous (PPA), passive parallel synchronous (PPS), and passive serial (PS). For complete information on FLEX 8000 configuration schemes, see *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*.

continuity checking A test for open circuits between device pins and programming adapter sockets. This test verifies that a device is properly seated in the socket of the adapter.

CQFP Ceramic quad flat pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

D

Database Builder The MAX+PLUS II Compiler module that builds a single, fully flattened database which integrates all files in a project hierarchy. It also examines the logical completeness and consistency of the project and checks for boundary connectivity and syntactical errors.

dedicated input pin A pin that can only be used as an input to the device.

Design Doctor The Compiler utility that checks each design file in a project for logic that could cause reliability problems when the project is implemented in one or more devices. The Design Doctor runs in conjunction with the Logic Synthesizer module and analyzes the project with a predefined or customized set of design rules.

development socket A prototyping socket for high-pin-count QFP packages.

device Refers to an Altera programmable logic device, including FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices. Altera also offers Configuration EPROM devices that are used to configure FLEX 10K and FLEX 8000 devices.

device family A group of Altera programmable logic devices with the same fundamental architecture. Altera device families are the FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic device families. Altera also offers a Configuration EPROM device family that includes devices used for configuring FLEX 10K and FLEX 8000 devices.

DIP Dual in-line package. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information. Ceramic (CerDIP) and plastic (PDIP) versions are available.

E

EDIF Electronic Design Interchange Format. An industry-standard format for the transmission of design data. You can generate an EDIF 2 0 0 or 3 0 0 netlist file from a schematic design or from a VHDL or Verilog HDL design that has been processed with an appropriate industry-standard synthesis tool and you can then import the file into MAX+PLUS II as an EDIF Input File (**.edf**). MAX+PLUS II supports EDIF Input Files that contain functions from the library of parameterized modules (LPM). The MAX+PLUS II Compiler can also generate one or more EDIF Output Files (**.edo**) in either EDIF 2 0 0 or 3 0 0 format that contain functional and timing information for simulation with a standard EDIF simulator.

EDIF Input File (.edf) An EDIF version 2 0 0 or 3 0 0 netlist file generated by any industry-standard EDIF netlist writer. EDIF Input Files can be compiled by the MAX+PLUS II Compiler. MAX+PLUS II supports EDIF Input Files that contain functions from the library of parameterized modules (LPM).

EDIF Output File (.edo) An EDIF version 2 0 0 or 3 0 0 netlist file generated by the EDIF Netlist Writer module of the MAX+PLUS II Compiler. This file can be exported to an industry-standard workstation or PC environment for simulation.

EEPROM Electrically Erasable Programmable Read-Only Memory. A form of reprogrammable semiconductor memory in which the contents can be erased by subjecting the device to appropriate electrical signals. See *Operating Requirements for Altera Devices* and *Configuration Elements & Reliability* in this data book for more information.

embedded array A series of embedded array blocks (EABs) that is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide data-path manipulation, and data transformation functions.

embedded array block (EAB) The building block of embedded arrays. Each EAB provides 2,048 bits of configurable RAM, ROM, FIFO, or dual-port RAM. When implementing logic, each EAB can contribute 100 to 300 gates towards complex logic functions.

EPLD Erasable programmable logic device. Altera EPLD device families include MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic.

EPROM Erasable Programmable Read-Only Memory. A form of reprogrammable semiconductor memory in which the contents

can be erased by subjecting the device to the proper wavelength of ultraviolet light. See *Operating Requirements for Altera Devices* and *Configuration Elements & Reliability* in this data book for more information.

expander product term A single product term with an inverted output that feeds back into the logic array block (LAB) of a MAX 9000, MAX 7000, or MAX 5000 device. An uncommitted expander product term that can be shared with other logic cells in the same LAB is called a shareable expander; a product term that has been shared in this manner is called a shared expander. In MAX 9000 and MAX 7000 devices only, an expander product term that is "borrowed" from an adjacent logic cell in the same LAB is called a parallel expander.

external timing parameters Factory-tested, worst-case values specified by Altera. In this data book, external timing parameters are shown in bold type. In the *FLEX 8000 Programmable Logic Device Family Data Sheet*, external timing parameters are listed under "External Timing Characteristics."

extraction tool A tool to extract QFP devices from QFP carriers. Extraction tools are available from Altera for 100-pin, 160-pin, 208-pin, 240-pin, and 304-pin QFP packages. See the *QFP Carrier & Development Socket Data Sheet* in this data book for information.

F

family-specific macrofunction A macrofunction provided by Altera that contains logic optimized for the architecture of a specific device family. The functionality of a family-specific macrofunction is always the same, regardless of the device family for which it is designed. However, primitives and nodes used within the macrofunction file can vary among families to take advantage of different device architectures, providing higher performance and more efficient implementation.

FastTrack Interconnect Dedicated connection paths that span the entire width and height of a FLEX 10K, FLEX 8000, or MAX 9000 device. These connection paths allow signals to travel between all logic array blocks (LABs) in a device.

Fit File (.fit) An ASCII text file generated by the Compiler that documents pin, logic cell, I/O cell, embedded cell, chip, and device assignments made during the last compilation.

Fitter The MAX+PLUS II Compiler module that fits a project into one or more devices. The Fitter selects appropriate interconnection paths as well as the pin and logic cell assignments. It also generates part of the Report File (**.rpt**) and Fit File (**.fit**) for the project.

FLASH A type of reprogrammable semiconductor memory, whose contents of which can be erased by subjecting the device to appropriate electrical signals. See *Configuration Elements & Reliability* in this data book for more information.

FLASHlogic An Altera device family consisting of SRAM-based devices with shadow EPROM or shadow FLASH memory. The high performance FLASHlogic device family includes the EPX880 and EPX8160 devices.

FLEX Download Cable A cable used to download SRAM Object File (**.sof**) data in a passive serial (PS) configuration scheme to a FLEX 10K or FLEX 8000 device in-circuit. You can configure FLEX 10K and FLEX 8000 devices with the FLEX Download Cable to allow in-circuit testing and prototyping on the printed circuit board (PCB).

FLEX 8000 An Altera device family based on the Flexible Logic Element MatriX (FLEX) architecture. This SRAM-based family offers high-performance, register-intensive, high-gate-count devices. The FLEX 8000 device family includes the EPF8282A, EPF8282AV,

EPF8452A, EPF8636A, EPF8820A, EPF81188A, and EPF81500A devices.

FLEX 10K The most recent Altera device family based on the Flexible Logic Element MatriX (FLEX) architecture. This SRAM-based family offers high-performance, register-intensive, high-gate-count devices with embedded arrays. The embedded arrays are used to efficiently implement memory or complex logic functions. The FLEX 10K device family includes the EPF10K10, EPF10K20, EPF10K30, EPF10K40, EPF10K50, EPF10K70, and EPF10K100 devices.

flipflop An edge-triggered, clocked storage unit that stores a single bit of data. A low-to-high transition on the clock signal changes the output of the flipflop based on the value of the data input(s). This value is maintained until the next low-to-high transition of the clock, or until the flipflop is preset or cleared. Depending on the architecture of the device family, a register can be programmed as a level-sensitive flow-through latch or as an edge-triggered D, T, JK, or SR flipflop.

functional simulation A MAX+PLUS II Simulator mode that uses a functional Simulator Netlist File (**.snf**) to simulate the logical performance of a project without timing information.

Functional SNF Extractor The MAX+PLUS II Compiler module that creates the functional Simulator Netlist File (**.snf**) required for functional simulation.

G

Graphic Design File (.gdf) A schematic design file created with the MAX+PLUS II Graphic Editor.

global clear A signal from a dedicated input pin that does not pass through the logic array before arriving at the clear input of a register. In FLEX 8000 devices, a global clear can come from any of the dedicated inputs. MAX 9000 and MAX 7000 devices have input pins that can be used either as global clear sources or dedicated inputs to the device.

global clock A signal from a dedicated input pin that does not pass through the logic array before arriving at the clock input of a register. In FLEX 8000 devices, a global clock can come from any of the four dedicated input pins. MAX 9000, MAX 7000, MAX 5000, and EP1810 devices have input pins that can be used as either global clock sources or dedicated inputs to the device. EP910 and EP610 devices have dedicated clock input pins.

H

Hexadecimal (Intel-Format) File (.hex) A hexadecimal file in the Intel Hex format. The MAX+PLUS II Compiler and Simulator can use Hex Files as inputs to specify the initial memory contents. After compilation, you can also create Hex Files that support other configuration schemes for FLEX 10K and FLEX 8000 devices.

I

Include File (.inc) An ASCII text file that can be imported into a Text Design File (**.tdf**) with an AHDL Include Statement. The contents of the Include File replace the Include Statement that calls the file. Include Files can contain Function Prototype, Constant, Delete, and Parameters Statements.

interconnect timing parameters Internal timing parameters for the interconnect in FLEX 8000 devices.

internal timing parameters Worst-case delays based on external timing parameters. Internal timing parameters cannot be measured explicitly, and should be used only for estimating device performance. Post-compilation timing simulation or timing

analysis is required to determine actual worst-case performance. In this data book, internal timing parameters are shown in italics.

I/O cell Also known as an I/O element. A register that exists on the periphery of a FLEX 10K, FLEX 8000, or MAX 9000 device, or a fast input-type logic cell that is associated with an I/O pin in a MAX 7000E device. I/O cells permit short setup time.

I/O cell register A logic option with which you specify that you wish to implement a register in an I/O cell on a FLEX 10K, FLEX 8000, MAX 9000, MAX 7000S, or MAX 7000E device. This logic option can be applied to individual logic functions. However, it cannot be incorporated into a logic synthesis style or applied to an entire project. The MAX+PLUS II **Global Project Logic Synthesis** command specifies the default logic synthesis style and other synthesis settings for the current project. The command also allows you to specify which global signals the Compiler should create automatically, and whether to set multi-level synthesis or standard synthesis for the current project. You can also specify global default settings for logic options, such as automatic one-hot encoding, register packing, and open-drain pins.

J

JEDEC File (.jed) An ASCII file that contains programming information. JEDEC Files provide an industry-standard format for transferring information between a data preparation system and a logic device programmer. The MAX+PLUS II Compiler automatically generates JEDEC Files for the following devices during compilation: EP610, EP610I, EP910, EP910I, and EP1810 devices (Classic family) as well as EPM5032 devices (MAX 5000 family). The MAX+PLUS II Programmer can use a JEDEC File created with MAX+PLUS II (DOS), A+PLUS, or PLDshell Plus to program the Altera devices listed above, in addition to FLASHlogic devices. The Programmer can also optionally save programming data plus functional test vector in JEDEC File format.

JED2JTAG A software utility used in conjunction with PLDshell Plus. JED2JTAG is used to download JEDEC Files to one or more FLASHlogic devices via the FLASHlogic Download Cable.

JLCC Ceramic J-lead chip carrier. A device package offered by Altera. Both ceramic J-lead chip carrier (JLCC) and plastic J-lead chip carrier (PLCC) packages are available. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

JTAG Joint Test Action Group. A set of specifications that enables a designer to perform board- and device-level functional verification of a board during production.

JTAG boundary-scan testing Testing that isolates a device's internal circuitry from its I/O circuitry. This testing is made possible by the Joint Test Action Group (JTAG) boundary-scan test (BST) architecture that is available in all FLEX 10K devices, all FLEX 8000 devices except the EPF8452A and EPF81188A, all MAX 9000 devices, and all FLASHlogic devices. Serial data is shifted into boundary-scan cells in the device; observed data is shifted out and externally compared to expected results. Boundary-scan testing offers efficient PC board testing, providing an electronic substitute for the traditional "bed of nails" test fixtures.

L

Library Mapping File (.lmf) An ASCII text file used to map cells in EDIF Input Files (**.edf**) or symbols in OrCAD Schematic Files (**.sch**) to corresponding MAX+PLUS II primitives, megafunctions, or macrofunctions.

library of parameterized modules (LPM) An architecture-independent library of logic functions that are parameterized to achieve scalability and adaptability. Altera has implemented parameterized modules from LPM version 2.0.1 to 2.1.0 which offer architecture-independent design entry for all MAX+PLUS II-supported devices. The MAX+PLUS II Compiler includes built-in compilation support for LPM functions used in schematics, AHDL files, and EDIF Input Files.

linked simulation A MAX+PLUS II Simulator mode that uses a linked Simulator Netlist File (**.snf**) to simulate the logical performance of a super-project that consists of multiple, linked individual projects. A linked simulation uses the timing and/or functional netlist information from the combined SNFs of the individual linked sub-projects.

LPM *See* library of parameterized modules (LPM).

logic array A series of logic array blocks (LABs) that is used to implement general logic, such as counters, adders, state machines, and multiplexers. The logic array performs the same function as the sea-of-gates in gate arrays.

logic array block (LAB) A physically grouped set of logic resources in an Altera device. The LAB consists of a logic cell array and, in some device families, an expander product term array. Any signal that is available to any one logic cell in the LAB is available to the entire LAB. In FLEX 10K, FLEX 8000 and MAX 9000 devices, the LAB is fed by row interconnect paths and a dedicated input bus. In MAX 7000, FLASHlogic, and MAX 5000 devices, the LAB is fed by a programmable interconnect array (PIA) and a dedicated input bus. In Classic devices, the logic in the LAB shares a global clock signal. The LAB is fed by a global bus and a dedicated input bus. In the EP1810, LABs are called quadrants.

logic cell The generic term for the basic building block of an Altera device. In FLEX 10K and FLEX 8000 devices, logic cells are called logic elements. In MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices, logic cells are called macrocells.

logic element (LE) A basic building block of an Altera FLEX 10K or FLEX 8000 device. A logic element consists of a look-up table (LUT)—i.e., a function generator that quickly computes any function of four variables—and a programmable register to support sequential functions. The register can be programmed as a flow-through latch, as a D, T, JK, or SR flipflop, or bypassed entirely for pure combinatorial logic. The register can feed other logic cells or feed back to the logic cell itself. Some logic elements feed output or bidirectional I/O pins on the device.

logic element timing parameters Internal timing parameters for the logic elements in FLEX 8000 devices.

Logic Programmer card The LP6 expansion card required to run the MAX+PLUS II Programmer and program Altera devices. MAX+PLUS II software currently supports the LP6 Programmer card for use with PC-AT and compatible computers.

Logic Synthesizer The Compiler module that uses several algorithms to minimize gate count, remove redundant logic, and utilize the device architecture as efficiently as possible. Processing can be customized with logic option and logic synthesis style assignments. This module also applies logic synthesis techniques to help implement timing requirements for a project.

look-up table (LUT) A function that generates outputs based on inputs and a set of stored data. The logic element of FLEX 10K and FLEX 8000 devices includes a four-input LUT

that can be configured to emulate any logical function of four inputs.

M

macrocell The basic building block in Altera MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices. A macrocell consists of two parts: combinatorial logic and a configurable register. The combinatorial logic allows a wide variety of logic functions. Depending on the architecture of the device family, the register can be programmed as a flow-through latch, as a D, T, JK, or SR flipflop, or bypassed entirely for pure combinatorial logic. The register can feed other macrocells or feed back to the macrocell itself. Some macrocells feed output or bidirectional I/O pins on the device. Macrocells in FLEX 10K and FLEX 8000 devices are called logic elements.

macrofunction A high-level building block that can be used together with gate and flipflop primitives in MAX+PLUS II design files. In general, a macrofunction is a lower-level design file in a MAX+PLUS II hierarchical project.

Master Programming Unit (MPU) A logic device programming box. The MPU works with zero-insertion-force sockets and individual adapters to program and test Altera devices. The PL-MPU base unit and PLM-prefix adapters support both device programming and device testing. The PLE3-12 base unit, as well as adapters with other prefixes, support device programming only.

MAX 5000 An Altera device family based on the first generation of Multiple Array MatriX (MAX) architecture. This EPROM-based device family includes EPM5032, EPM5064, EPM5128, EPM5130, and EPM5192 devices.

MAX 7000 An Altera device family based on the second generation of Multiple Array MatriX (MAX) architecture. MAX 7000S and MAX 7000E devices are enhanced versions of MAX 7000 devices and are function-, pin-, and programming file-compatible with MAX 7000 devices. MAX 7000E and MAX 7000S devices offer up to six pin- or logic-driven output enable signals, fast input setup times to logic cells, and multiple global clocks with optional inversion. In addition, MAX 7000S devices feature ISP and JTAG boundary-scan test circuitry. These EEPROM-based devices include EPM7032, EPM7032S, EPM7032V, EPM7064, EPM7064S, EPM7096, EPM7096S, EPM7128E, EPM7128S, EPM7128SV, EPM7160E, EPM7160S, EPM7192E, EPM7192S, EPM7256E, and EPM7256S devices.

MAX 9000 An Altera device family based on the third generation of Multiple Array MatriX (MAX) architecture, with a higher density than the MAX 7000 device family. These EEPROM-based devices include EPM9320, EPM9400, EPM9480, and EPM9560 devices.

MAX+PLUS II Altera's Multiple Array MatriX Programmable Logic User System. MAX+PLUS II is a set of computer programs and hardware support products that allow design and implementation of custom logic with FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices.

MegaCore function Megafunctions that are created by Altera and are optimized for use with Altera devices.

megafunction Off-the-shelf building blocks that implement useful functions such as processors, digital signal processing (DSP) functions, bus controllers, and interfaces. Both MegaCore and AMPP megafunctions are available.

MPLD Mask-Programmed Logic Device. A custom Altera device created by converting a design originally created for an Altera programmable logic device. Altera offers a program for converting customer designs into

MPLDs, which are cost-effective alternatives for high-volume production.

O

OrCAD Library File (.lib) A binary file containing information that describes how symbols are displayed in OrCAD Schematic Files (.**sch**).

OrCAD Schematic File (.sch) A schematic design file created with the OrCAD Draft schematic editor. You can open and edit an OrCAD Schematic File in MAX+PLUS II and save it as both a Graphic Design File (.**gdf**) and an OrCAD Schematic File (.**sch**). An OrCAD Schematic File can also be compiled directly by the MAX+PLUS II Compiler.

P

parallel expander An expander product term that is "borrowed" from an adjacent logic cell in the same MAX 9000 or MAX 7000 logic array block (LAB). A parallel expanders is also a logic option that you can apply to a logic function to allow it to borrow such parallel expanders. This option can reduce the number of shared expander product terms required in your project and increase the speed of your project. However, the project may use additional logic cells, and may be more difficult to fit.

Partitioner The MAX+PLUS II Compiler module that divides a project into multiple devices, minimizing the number of connections between devices.

passive parallel asynchronous (PPA) A configuration scheme in which an external controller (e.g., a CPU) loads the design data into a FLEX 10K or FLEX 8000 device via a common data bus.

PCI *See* peripheral component interconnect (PCI).

PDIP Plastic dual in-line package. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

PENGN A utility used in conjunction with PLDshell Plus. PENGN is used to download logic designs to FLASHlogic devices via the FLASHlogic Download Cable.

peripheral component interconnect (PCI) An industry-established, high-speed bus standard for 32- and 64-bit applications.

peripheral register A register on the periphery of a FLEX 8000 device. A peripheral register is also a logic option that specifies that a register should be implemented in a peripheral register.

PGA Pin-grid array device package. A ceramic device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

PIA *See* programmable interconnect array.

PLAD3-12 An adapter that plugs into the Master Programming Unit (MPU). This adapter allows you to use PLE-prefix adapters originally designed for use with the PLE3-12A programming unit.

PLCC A device package option offered by Altera. Both ceramic J-lead chip carrier (JLCC) and plastic J-lead chip carrier (PLCC) packages are available.

PLDshell Plus Altera's Programmable Logic Shell. PLDshell Plus is a set of computer programs for designing and implementing custom logic circuits with Altera FLASHlogic and Classic devices. The MAX+PLUS II Programmer can program FLASHlogic and Classic devices with JEDEC Files (.**jed**) created by PLDshell Plus.

programmable interconnect array (PIA) The portion of a MAX 7000, FLASHlogic, or MAX 5000 device that routes signals between different logic array blocks (LABs).

Programmer Object File (.pof) A binary file generated by the MAX+PLUS II Compiler's Assembler module. This file contains the data used by the MAX+PLUS II Programmer to program an Altera device. The MAX+PLUS II Programmer can optionally save functional text vectors in a POF.

PQFP Plastic quad flat pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

product term Two or more factors in a Boolean expression combined with an AND operator constitute a product term, where "product" means "logic product."

programmable logic devices (PLDs) Digital, user-configurable integrated circuits used to implement custom logic functions. PLDs can implement any Boolean expression or registered function with built-in logic structures.

programming file A file containing data for programming Altera devices. Both the MAX+PLUS II Compiler and Programmer can generate programming files. The following programming file formats are available in MAX+PLUS II: Hexadecimal (Intel-Format) File (**.hex**), JEDEC File (**.jed**), JTAG Chain File (**.jcf**), Programmer Object File (**.pof**), Raw Binary File (**.rbf**), Serial Bitstream File (**.sbf**), SRAM Object File (**.sof**), Tabular Text File (**.ttf**).

POF, SOF, and JEDEC Files are used to program devices with the MAX+PLUS II Programmer. Test vector for functional testing can be saved in POFs and JEDEC Files, Hex Files, TTFs, RBFs, and SBFs are used to configure FLEX 10K and FLEX 8000 devices by other means. JCFs are used to program or configure one or more FLEX 10K, MAX 9000, or FLASHlogic devices in a multi-device JTAG chain. JEDEC Files generated by A+PLUS and PLDshell Plus software can also be used to program Classic devices. The Programmer can save data read from an examined device in POF or JEDEC File format.

project A project consists of all files associated with a particular design, including all subdesign files and related ancillary files created by the user or by the MAX+PLUS II software. The project name is the same as the name of the top-level design file in the project, without the filename extension. MAX+PLUS II performs compilation, simulation, timing analysis, and programming one project at a time.

Q

QFP Quad flat pack. A device package offered by Altera. Windowed ceramic QFP (CQFP), plastic QFP (PQFP), power QFP (RQFP) and plastic thin QFP (TQFP) packages are available. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

R

register *See* flipflop.

removal tool *See* extraction tool.

Report File (.rpt) An ASCII test file, generated by the MAX+PLUS II Compiler's Fitter module, that shows how device resources are used by the project. If a module preceding the Partitioner generates an error, this file is not generated. If the Partitioner generates an error, the Report File is generated in most cases.

RQFP Power quad flat pack. A device package offered by Altera. See *Altera Device Package*

Outlines and *Ordering Information* in this data book for more information.

S

Security Bit A bit that prevents an Altera device from being interrogated. This bit also prevents EPROM-based Altera devices from being inadvertently reprogrammed. The security bit can be turned on or off for each device in a project, or for the entire project.

shared expanders and **shareable expanders** A feature of MAX 9000, MAX 7000, and MAX 5000 device architecture that allows logic cells to use uncommitted product terms within the same logic array block (LAB). A product term that is eligible to be shared in this manner is called a sharable expander; a product term that has been shared in this manner is called a shared expander. The MAX+PLUS II Compiler automatically allocates shareable expanders when a project is compiled. A shared expander also can be allocated with an EXP primitive.

Simulator Netlist File (.snf) A binary file containing the data for functional simulation, timing simulation or timing analysis, or linked multi-device simulation. These optional Compiler modules create the different types of SNFs that contain the information required for different simulation modes and/or timing analysis.

SOIC Small-outline integrated circuit. A plastic device package option. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

SRAM Static random access memory. A read-write memory that stores data in integrated flipflops. See *Configuration Elements & Reliability* in this data book for more information.

SRAM Object File (.sof) A binary file generated by the MAX+PLUS II Compiler's Assembler module that contains the data for configuring an Altera FLEX 10K or FLEX 8000 device.

Symbol File (.sym) A graphic file created by the Symbol Editor or the Compiler Netlist Extractor module of the Compiler. This file represents a design file (a megafunction or macrofunction) or MAX+PLUS II primitive with the same name and can be used in Graphic Design Files (**.gdf**).

T

Tabular Text File (.ttf) An ASCII text file in tabular format containing configuration data for the sequential passive parallel synchronous (PPS), passive parallel asynchronous (PPA), and passive serial (PS) configuration schemes for FLEX 8000 devices, and the PS configuration scheme for FLEX 10K devices.

Text Design File (.tdf) An ASCII text file written in the Altera Hardware Description Language (AHDL). Text Design Export Files (**.tdx**) and Text Design Output Files (**.tdo**) can be saved as TDFs and compiled with MAX+PLUS II.

Text Design Export File (.tdx) An ASCII text file in the Altera Hardware Description Language (AHDL) that is optionally generated when you compile a Xilinx Netlist Format File (**.xnf**). It contains the same logic as the SNF File. A Text Design Export File can be saved as a Text Design File (**.tdf**) and used to replace the corresponding XNF File in the hierarchy of a project.

timing simulation A MAX+PLUS II Simulator mode that uses a timing Simulator Netlist File (**.snf**) to simulate the logical and timing performance of a project. Because the timing SNF is generated after logic synthesis, partitioning and fitting are performed; timing simulation allows you to simulate only the nodes in a project that have not been removed by logic optimization.

TQFP Thin quad flat pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

Turbo Bit A control bit for choosing the speed and power characteristics of an Altera device. If the Turbo Bit is on, the speed increases; if it is off, the power consumption decreases. The Turbo Bit can be turned on or off in a design file or in the Compiler.

U

user I/O The total number of I/O pins and dedicated inputs on a device.

V

Verilog HDL A hardware description language from Cadence. You can create a Verilog HDL description with the MAX+PLUS II Text Editor or any standard text editor and compile it directly with MAX+PLUS II. You can also generate an EDIF 2 0 0 or 3 0 0 netlist file from a Verilog HDL design that has been processed with a Verilog HDL synthesis tool. The netlist file can then be imported into MAX+PLUS II as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate a Verilog Output File (**.vo**).

Verilog Output File (.vo) A Verilog Hardware Description Language (HDL) standard netlist file generated by the Verilog Netlist Writer module of the Compiler. A Verilog Output File contains functional and timing information for simulation with a standard Verilog simulator.

VHDL Very High Speed Integrated Circuit (VHSIC) Hardware Description Language. You can create a VHDL Design File (**.vhd**) with the MAX+PLUS II Text Editor or any standard text editor and compile it directly with MAX+PLUS II. You can also generate an EDIF 2 0 0 or 3 0 0 netlist file from a VHDL design that has been processed with a VHDL synthesis tool. The netlist file can then be imported into MAX+PLUS II as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate a VHDL Output File (**.vho**).

VHDL Design File (.vhd) An ASCII text file created with the MAX+PLUS II Text Editor or another standard text editor. The VHDL Design File contains design logic that is defined with VHDL.

VHDL Output File (.vho) A VHDL standard netlist file that is generated by the VHDL Netlist Writer module of the Compiler. A VHDL Output File contains functional and timing information for simulation with a standard VHDL simulator.

W

Waveform Design File (.wdf) A binary file created with the Waveform Editor, which contains design logic that is defined by a combination of waveforms.

X

Xilinx Netlist Format (.xnf) A netlist format generated by Xilinx software. XNF Files generated by running the Xilinx LCAXNF utility can be compiled directly by the MAX+PLUS II Compiler. An XNF File can define all logic in a project, or be incorporated at the bottom level in a hierarchical project.

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Numerics

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